

Oregon Department of Transportation

Standard Specification

for

Microcomputer Signal Controller

July 1, 2014



OREGON DEPARTMENT OF TRANSPORTATION
TRAFFIC-ROADWAY SECTION

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CHAPTER 1: GLOSSARY

Wherever the following terms or abbreviations are used, the intent and meaning shall be interpreted as follows:

A – Ampere

AC – Alternating Current

AC+ - 120 volts AC, 60 hertz ungrounded power source

AC- - 120 volts AC, 60 hertz grounded return to the power source

AGTS - Automatic Generator Transfer Switch

amp(s) – Ampere(s)

AWG – American Wire Gage

BBS – Battery Backup System

C – Celsius

Cabinet – An outdoor enclosure for housing the controller unit and associated equipment

Certificate of Compliance – A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications

Component – A component shall be defined as any electrical or electronic device

Contractor – The person or persons, manufacturer, firm, partnership, corporation, vendor, or combination thereof, who have entered into a contract with the STATE, as party or parties of the second part or their legal representative

Controller Unit – That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly

CPU – Central Processing Unit

DC – Direct Current

DIN – Deutsche Industry Norm

EG – Equipment Ground

EIA – Electronic Industries Association

EMI – Electro Magnetic Interference

Engineer – The Chief Engineer of the Department of Transportation, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them

Equal – Interpretation shall be in the judgment of the Engineer:

- Connectors: Having identical physical dimensions, contact/pin material, plating, and method of connection.
- Devices: conforming to function, pin out, electrical and operating parameter requirements, access times, and interface parameters of the specified device.

ETL – Electrical Testing Laboratories, Inc.

Firmware – A computer program or software stored permanently in PROM, EPROM or ROM, or semi-permanently in EEPROM

FLASH – A +5 VDC powered IC memory device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features

FPA – Front Panel Assembly

Hz – Hertz

IC – Integrated Circuit

IEEE – Institute of Electrical and Electronics Engineers

ISO – International Standards Organization

Jumper – A means of connecting/disconnecting two or more conductive points by soldering or de-soldering a conductive wire or by PCB post connection or disconnection.

KB – Kilobytes

KBps - Kilobytes per second

kHz – kilohertz

Laboratory – The established laboratory of the Department of Transportation or other laboratories authorized by the Department to test materials involved in the contract

LED – Light Emitting Diode

LOGIC – Negative Logic Convention (Ground True) State

lx – Lux

m – Meter

mA – Milliampere

MB – Megabyte

Module – A functional unit that plugs into an assembly

MOS - Metal Oxide Semiconductor

MOV – Metal Oxide Varistor

MPU – Microprocessor Unit

ms – Millisecond(s)

mV – Millivolt(s)

mW – Milliwatt(s)

N – Newton (SI unit of force)

NA – Presently not assigned - cannot be used by the contractor for other purposes

NEMA – National Electrical Manufacturer’s Association

N.C. – Normally closed contact

N.O. – Normally open contact

ns – Nanosecond

PCB – Printed Circuit Board

PDA – Power Distribution Assembly

pF – Picofarad

PWM – Pulse Width Modulation

RBF – Random Block File

RDR – ACIA Receiver Data Register

RF – Radio Frequency

RMS – Root Mean Square

ROM – Read Only Memory

RTCA – Real Time Clock Adjuster Circuitry

s – Second

Second Sourced – Produced by more than one manufacturer

SI – International System of Units

SMC – Serial Management Controller

SP – Serial Port

SR – ACIA Status Register

SRAM – Static Random Access Memory

STATE – State of Oregon

SW – Switch

TBK – Terminal Block

TDR – ACIA Transmit Data Register

TOD – Time of Day Clock

Triac – Silicon controller rectifier which controls power bilaterally in an AC switching circuit

Thumb Screw Device (TSD) – A retractable screw fastener with projecting stainless steel screw, spring, and natural aluminum knob finish

TTL – Transistor-Transistor Logic

UL – Underwriter’s Laboratories, Inc.

VAC – Voltage Alternating Current

VDC – Voltage Direct Current

VME – Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2

Watchdog Timer (WDT) – A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts

x – Number Value

XX – Manufacturer's Option

μA – Microampere

μF – Microfarad

μH – Microhenry

μS – Microsecond

CHAPTER 2: GENERAL SPECIFICATIONS

2.1.1 Specifications

2.1.1.1 All devices must meet the general specifications in the following specifications, as well as the ODOT Standard Specification for Microcomputer Signal Controller dated September 4, 2001, the Caltrans TEES Specifications as published March 12, 2009 and Errata 1 dated January 21, 2010.

2.1.1.2 In case of conflict, the Engineer will resolve any discrepancies between these documents in the following order or precedence:

- ODOT Standard Specification for Microcomputer Signal Controller dated July 1, 2014
- ODOT Standard Specification for Microcomputer Signal Controller dated September 4, 2001
- Caltrans TEES Specifications dated March 12, 2009 and Errata 1 dated January 21, 2010

2.1.2 Documentation

2.1.2.1 Each controller cabinet assembly shall include two copies of the latest manual for each item of equipment that is furnished with the cabinet. The STATE, at our option, may reduce the number of manuals required on a project.

2.1.2.2 Manuals shall be printed in font of Helvetica Bold 12 (or equal) on 8.5 in by 11.5 in paper. Schematics, layouts, parts lists, and plan details shall have a minimum font of Gothic Legal 18 (or larger) and may be on 11 in by 17 in sheets, but the sheets must be neatly folded to 8.5 in by 11 in size. The manual shall be bound in durable covers.

2.1.2.3 Each manual shall include the following:

- Table of Contents
- Glossary
- General Description
- General Characteristics
- Installation
- Adjustments
- Theory of Operation
 - Systems Description (Include block diagram)
 - Detailed Description of Circuit operation
- Maintenance
 - Preventive Maintenance

- Trouble Analysis
- Troubleshooting Sequence Chart
- Wave Forms
- Voltage Measurements
- Alignment Procedures
- Parts List (To include circuit and board designation, part type and class, power rating and component manufacturer, original manufacturer's part number and data specification sheets for special design components)
- Electrical Interconnection Drawing
- Schematic and Logic Diagram
- Assembly Drawings and Pictorial Diagram Showing Physical Locations and Identification of Each Component

CHAPTER 3: SPECIFICATIONS FOR CABINET MODELS 332S, 332, 334, AND 336

SECTION 1- CABINET COMPOSITION

3.1.1 Requirements

3.1.1.1 Unless otherwise specified, the Cabinet shall be furnished, ready for operation, with the following composition:

3.1.1.2 The Model 332S Cabinet shall consist of the components shown on the cabinet print in Appendix A.

3.1.1.3 Terminal blocks (TB1 – TB9) shall be DIN rail mounted and labeled by mechanical means. All terminal blocks shall be one piece or factory assembled, sectional, color coded, double terminal, barrier type, with binder screw terminals. All wiring shall be terminated with insulated wire ferrules. Terminal blocks shall not interfere with the access or opening up to 60 degrees of back panels on devices mounted in the front of the cabinet. The terminal blocks shall meet the following minimum specifications:

- Listing: UL1059
- Voltage Rating: 600V
- Current Rating: 30A
- Wire Range: 10AWG to 22AWG

3.1.1.4 The Model 332 Cabinet shall consist of the components shown/specified in Appendix C

3.1.1.5 The Model 334 Cabinet shall consist of the components shown/specified in Appendix C

3.1.1.6 The Model 336 Cabinet shall consist of the components shown/specified in Appendix C

3.1.1.7 Cabinets shall have all input and output files installed and wired complete. However, only those input and output devices, such as detector sensor units, isolator units, and switch packs necessary to provide the operation required by the plans or specifications shall be furnished.

3.1.1.8 All assemblies and files included in cabinets shall be mounted on the cage mounting rails. Cabinet model interface wiring shall be per the cabinet print, detailed wiring lists, and cabinet wiring diagram.

3.1.2 Cabinet Shipping Requirements

3.1.2.1 The cabinet shall be delivered mounted on a plyboard shipping pallet. The pallet shall be bolted to the cabinet base. The housing doors shall be blocked to prevent movement during transportation.

SECTION 2- HOUSING REQUIREMENTS

3.2.1 Requirements

3.2.1.1 Except as herein modified, the cabinet housing shall conform to the CALTRANS TEES Specifications in Chapter 6.

3.2.2 Locks

3.2.2.1 The locks shall be a Best Company 5L7RD Series (or an approved equal) with a red construction core. Two keys shall be supplied with each cabinet. The keys shall be removable in the locked position only.

3.2.3 332S Cabinet Light Fixture

3.2.3.1 Two LED cabinet light fixtures shall be installed in each controller cabinet. The light fixture shall be mounted to the cabinet exhaust area cover plate by screw and self-locking nut. The mounting hardware shall not penetrate the exterior of the cabinet shell. The light fixture shall not interfere with access to any cabinet component or terminal blocks.

3.2.3.2 The light fixture shall be protected by an “in-line” type fuse holder (1 Amp fuse) and controlled from a normally closed door-operated switch located at each door. The fixture power shall be switched “ON” when the each door is opened.

3.2.3.3 The LED fixture shall meet the following minimum specifications:

- Input voltage: 120VAC
- Lumens: 200 Lumens or greater
- Color temperature: 2700°K to 5500°K
- Total wattage: 15 Watts or less
- Lumen maintenance (L70): 50,000 Hours or More
- Operating Temperature: -40° F to 140° F

3.2.4 Circuit Breaker Panel

3.2.4.1 Circuit breakers shall be UL 489 approved. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the Amperes rating shall be marked and visible from the front of the breaker. Contacts shall

be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from 0.4 °F to 122 °F. The minimum Interrupting Capacity shall be 10,000 Amperes. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carling switch Time Delay Curve #24 or equal).

SECTION 3- CABINET CAGE REQUIREMENTS

3.3.1 Requirements

3.3.1.1 The cabinet cage shall conform to the CALTRANS TEES Specifications in Chapter 6 – Section 3.

SECTION 4- CABINET ASSEMBLIES

3.4.1 Requirements

3.4.1.1 Except as herein modified, the cabinet assemblies shall conform to the CALTRANS TEES Specifications in Chapter 6 – Section 4.

3.4.2 332S Power Distribution Assembly (PDA)

3.4.2.1 PDA #2L for 332S Cabinet

- 1 – Duplex NEMA 5-15R Controller Receptacle
- 2 – Duplex NEMA 5-15R Equipment Receptacle
- 1 – 1-Pole, 15 amp, 120 VAC Signal Bus Circuit Breaker
- 1 – 1-Pole, 15 amp, 120 VAC Controller Circuit Breaker
- 5 – 1-Pole, 10 amp, 120VAC Signal Bus Circuit Breaker with Auxiliary Switch
- 1 – 2 Pole Ganged, 10 amp, 120 VAC Flash Bus Circuit Breaker
- 1 – Solid State Relay (Normally Closed) – Rated Minimum 50 Amperes, 120VAC (Crydom A2450-B or Equal)
- 2 – Model 204 Flasher Unit and Socket
- 1 – Model 206L Power Supply Module and Socket
- 1 – Model 430 Heavy Duty Relay & Socket (Transfer Relay)
- 1 – AUTO/FLASH Control Switch
- 1 – FLASH On Indicator Light
- 3 – 10 Position TBK T1, T2 & T4
- 1 – 4 Position TBK T3
- 1 – SSR Fault Indicator Light

3.4.3 Circuit Breaker with Auxiliary Switch

3.4.3.1 Five, single pole, 10 amp circuit breakers with auxiliary switch feature and medium trip delay characteristic shall be provided.

3.4.3.2 The five breakers shall be wired and routed per the Circuit Breaker Line Diagram. The breaker auxiliary switch circuit shall be open when the breaker is in the ON position. The auxiliary circuits shall be wired in parallel so that any tripped breaker shall energize the solid state relay input, flash transfer relay coils, and the “FLASH ON” indicator. The auxiliary contacts shall be rated at 5 amps, 120 VAC, minimum (fast-on type connection).

3.4.4 Power Strip for 332S

3.4.4.1 A power strip shall be installed in the cabinet cage. The power strip shall provide AC surge suppression with EMI noise filtering. The minimum performance specifications for the power strip are:

- Listing: UL 1449 Third Edition Type 3
- Peak surge current: 40kA
- Operating voltage: 120 VAC nominal
- Operating frequency: 60Hz nominal
- Clamping voltage: 330V
- AC suppression energy: 3840 Joules
- Number of Outlets 12 Total (2 Front/ 10 Rear)
- Operating temperature: -40°F to 165°F
- Maximum dimensions: 1.75” H x 19” W x 6” D
- Mounting: 19” rack mountable (1U rack space)

SECTION 5- CABINET WIRING

3.5.1 Requirements

3.5.1.1 Except as herein modified, the cabinet wiring shall conform to the CALTRANS TEES Specifications in Chapter 6 – Section 5.

3.5.2 Cabinet Wiring Diagram

3.5.2.1 The cabinet print shall be furnished on current ODOT drawings for the appropriate cabinet model. The drawings are available from the Traffic Standards Unit. A minimum of four (4) copies of wiring diagrams printed on all-weather 11” by 17” paper (Rite in the Rain or approved equal) is required.

3.5.2.2 The Contractor shall add to the drawing all information and details required giving an accurate description of the wiring and operation of each individual cabinet. The information required includes the following:

- Software program number and C1 & C11 connector pin program assigned functions
- Input panel phase and loop number references

- Input and output file phase references
- Location and phase reference for all input/output devices furnished
- Modifications made to standard cabinet wiring
- Intersection layout
- Phase sequence diagram
- Preemption sequence diagram (if applicable)

3.5.2.3 The intersection layout shall include all vehicle signals, pedestrian signals, vehicle detectors, push buttons, lane usage arrows, and special devices located and identified as shown on the plans. A north arrow shall also be included and the intersecting streets shall be identified.

3.5.2.4 The phase and preemption sequence diagrams shall refer to the phase designations and sequence shown on the plans for both normal phase rotation and preemption.

3.5.3 Conductors

3.5.3.1 AC Wiring shall be routed and bundled separately or shielded separately from all logic voltage control circuits.

3.5.3.2 Cabling and wiring shall be routed to prevent conductors from being in contact with metal edges. Cabling and wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

3.5.3.3 Each detector lead-in pair, from the field terminals to the input file terminals, shall be a cable of UL Type 2092 or better. The stranded, tinned, copper drain wire shall be connected to the "L" terminal on the input file TBKs. This input terminal shall be connected to the equipment grounding bus through a single conductor. Each connection to the input file shall be made by using a crimp connector that is soldered after the connector is crimped to the wire. Each connection to the field terminals shall be made by using a crimp ferrule connector. These cables shall be heat shrunk protected - both the drain wire and the foil shield, to prevent shorting against the contacts on the back of the input file.

3.5.4 Detector Test Buttons (Model 332S Cabinets)

3.5.4.1 A detector test panel containing 18 normally open pushbuttons shall be furnished and installed between the PDA & the output file.

3.5.4.2 There shall be a pushbutton for each input in a Model 332S Cabinet associated with each of the eight vehicle, four pedestrian phases, four EV

preempts and two Railroad preempts, whether or not such phases are used at a particular location.

3.5.4.3 The panel shall have a connector for disconnecting all panel wiring from the input file.

3.5.4.4 All pushbuttons shall be labeled by function.

SECTION 6- CABINET TRANSIENT SURGE SUPPRESSION REQUIREMENTS

3.6.1 Power Line Requirements (Model 332S Cabinets)

3.6.1.1 A surge protection device (SPD) shall be installed at the service feeder entrance of the traffic signal cabinet. The minimum performance specifications for the SPD are:

- Listing: UL 1449 Third Edition Type 1 or Type 2 SPD
- Peak surge current: 40kA per mode
- Operating voltage: 120 VAC
- Operating frequency: 60Hz nominal
- UL 1449 Voltage Protection Rating (VPR): 600V
- SPD technology: Metal Oxide Varistors (MOVs)
- Fault Indicator: Light Status
- Operating temperature: -40°F to 165°F
- Relative Humidity: 0-95% Non-Condensing
- Maximum dimensions: 6" H x 4" W x 6" D

3.6.2 Twisted Pair Copper Communications Surge Protection Requirements

3.6.2.1 A surge protection device (SPD) shall be furnished to provide protection from electrical transients over twisted pair communications. The minimum performance specifications for the SPD are:

- Listing: UL 497B
- Peak surge current: 10kA (8x20us)
- Clamping voltage: 50 to 200 Volts
- Insertion loss: 0.1 dB @ 10 MHz
- Operating temperature: -40°F to 165° F

CHAPTER 4: SPECIFICATIONS FOR TRAFFIC SIGNAL CONTROLLERS

SECTION 1- GENERAL REQUIREMENTS

4.1.1 Requirements

4.1.1.1 The traffic signal controller shall be listed on the Agency's QPL (Green Sheets).

SECTION 2- MODEL 2070 CONTROLLER

4.2.1 Requirements

4.2.1.1 Except as herein modified, the model 2070 controller shall conform to the CALTRANS TEES Specifications in Chapter 9.

4.2.2 Assembly

4.2.2.1 The model 2070E controller shall be composed of the following assembly:

- 2070 Lite Unit Chassis
- 2070-1E CPU Module
- 2070-2A Field I/O Module
- 2070-4 Power Supply Module
- 2070-3B Front Panel

4.2.2.2 The 2070-6A 1200 Baud Modem Module may be supplied as a separate item as an option to the Agency if specified in the special provisions

4.2.3 Software

4.2.3.1 The model 2070E controller shall be fully compatible with current versions of software used by the Agency.

4.2.4 Accessories

4.2.4.1 Two 2 Mb Data keys

CHAPTER 5: SPECIFICATIONS FOR INPUT DEVICES

SECTION 1- MODEL 222 TWO-CHANNEL LOOP DETECTOR SENSOR

5.1.1 Requirements

5.1.1.1 Model 222 Two-Channel Loop Detector Sensors shall conform to the CALTRANS TEES Specifications in Chapter 5.

5.1.1.2 Model 222 Two-Channel Loop Detector Sensors shall be listed on the Agency's QPL (Green Sheets).

SECTION 2- MODEL 242 TWO-CHANNEL DC ISOLATOR

5.2.1 Requirements

5.2.1.1 Model 242 Two-Channel DC Isolators shall conform to the CALTRANS TEES Specifications in Chapter 5.

5.2.1.2 Model 242 Two-Channel DC Isolators shall be listed on the Agency's QPL (Green Sheets).

SECTION 3- MODEL 252 TWO-CHANNEL AC ISOLATOR

5.3.1 Requirements

5.3.1.1 Model 252 Two-Channel AC Isolators shall conform to the CALTRANS TEES Specifications in Chapter 5.

5.3.1.2 Model 252 Two-Channel AC Isolators shall be listed on the Agency's QPL (Green Sheets).

SECTION 4- MODEL 255 TWO-CHANNEL AC ISOLATOR

5.4.1 Requirements

5.4.1.1 Model 255 Two-Channel AC Isolators shall conform to the CALTRANS TEES Specifications in Chapter 5 as an inverting Model 252 and labeled Model 255.

5.4.1.2 Model 255 Two-Channel AC Isolators shall be listed on the Agency's QPL (Green Sheets).

SECTION 5- EMERGENCY VEHICLE PREEMPTION SYSTEM

5.5.1 Requirements

5.5.1.1 Emergency Vehicle Preemption Systems shall be listed on the Agency's QPL (Green Sheets).

SECTION 6- GPS CLOCK ASSEMBLY

5.6.1 Requirements

5.6.1.1 GPS Clock Assemblies shall be listed on the Agency's QPL (Green Sheets).

SECTION 7- VIDEO DETECTION SYSTEM

5.7.1 Requirements

5.7.1.1 Video Detection Systems shall be listed on the Agency's QPL (Green Sheets).

SECTION 8- RADAR DETECTION SYSTEM

5.8.1 Requirements

5.8.1.1 Radar Detection Systems shall be listed on the Agency's QPL (Green Sheets).

SECTION 9- BATTERY BACKUP SYSTEM

5.9.1 Requirements

5.9.1.1 Battery Backup Systems shall be listed on the Agency's QPL (Green Sheets).

CHAPTER 6: SPECIFICATIONS FOR OUTPUT DEVICES

SECTION 1- MODEL 200 SWITCH PACK

6.1.1 Requirements

6.1.1.1 Model 200 Switch Packs shall conform to the CALTRANS TEES Specifications in Chapter 3.

6.1.1.2 Model 200 Switch Packs shall be listed on the Agency's QPL (Green Sheets).

SECTION 2- MODEL 204 FLASHER UNIT

6.2.1 Requirements

6.2.1.1 Model 204 Flasher Units shall conform to the CALTRANS TEES Specifications in Chapter 3.

6.2.1.2 Model 204 Flasher Units shall be listed on the Agency's QPL (Green Sheets).

SECTION 3- MODEL 430 FLASH TRANSFER RELAY

6.3.1 Requirements

6.3.1.1 Model 430 Flash Transfer Relays shall conform to the CALTRANS TEES Specifications in Chapter 6.

6.3.1.2 Model 430 Flash Transfer Relays shall be listed on the Agency's QPL (Green Sheets).

CHAPTER 7: SPECIFICATIONS FOR POWER SUPPLY AND MONITOR UNITS

SECTION 1- MODEL 206L POWER UNIT

7.1.1 Requirements

7.1.1.1 Model 206L Power Supplies shall conform to the CALTRANS TEES Specifications in Chapter 3.

7.1.1.2 Model 206L Power Supplies shall be listed on the Agency's QPL (Green Sheets).

SECTION 2- MODEL 210 MONITOR UNIT

7.2.1 Requirements

7.2.1.1 Model 210 Monitor Units shall conform to the CALTRANS TEES Specifications in Chapter 3 – Section 6.

7.2.1.2 Model 210 Monitor Units shall be listed on the Agency's QPL (Green Sheets).

7.2.2 Wiring Diagram Assignments

7.2.2.1 See Appendix

CHAPTER 8: TESTING AND EQUIPMENT ACCEPTANCE

SECTION 1- SUBMITTALS AND TESTING CRITERIA

8.1.1 Submittals

8.1.1.1 The Contractor is required to deliver all traffic signal control equipment, including cabinet prints and operation manuals, in one shipment. A minimum of four (4) copies of wiring diagrams printed on all-weather 11" by 17" paper (Rite in the Rain or approved equal) is required.

8.1.1.2 The testing of control equipment will be done at the expense of the Agency, requesting the testing. The Contractor shall allow six (6) weeks for testing. Incomplete shipments will not be accepted and will be returned to the Contractor at the Contractor's cost.

- The following information shall be included with equipment shipments:
- Contractor
- Supplier
- Manufacturer
- Location
- Contract number
- Agency for which the equipment is to be tested.
- Include a complete set of plans and specifications to which the equipment is to be tested

All traffic signal control equipment shall be delivered mounted on a plywood shipping pallet. The pallet shall be bolted to the cabinet base. The housing doors shall be blocked to prevent movement during transportation. The equipment shall be delivered to:

Oregon Department of Transportation
Traffic Systems Services Unit
2445 Liberty Street NE
Salem, Oregon 97303-6738

8.1.2 Testing Criteria

8.1.2.1 The following traffic signal control equipment will be tested by the Agency prior to being installed:

- Controller unit
- Controller cabinet
- 24VDC Power supply
- Input devices

- Preemption devices
- Loop amplifiers
- AC isolators
- DC isolators
- Video
- Radar
- Output devices
 - Flasher units
 - Relays
 - Switch packs
- Conflict monitor
- Auxiliary equipment in the cabinet
- Other equipment as noted in the special provisions required for the operation of an installation

8.1.2.2 All traffic signal control equipment will be tested as an assembly in three (3) categories: physical, operational, and environmental.

SECTION 2- PHYSICAL TESTING

8.2.1 Requirements

8.2.1.1 The physical testing of the traffic signal control equipment will consist of a visual and physical inspection of all specified equipment including wiring diagrams, operation manuals and documentation supplied. The following procedures for Physical Testing will verify the quality of the traffic signal equipment and conformance to plans and specifications.

8.2.2 Procedures

8.2.2.1 Verify quantity and alignment of the following items as applicable. Remove and reinsert each device from the assembly. Each device shall slide smoothly on its tracks while being inserted or removed from the assembly where applicable.

- 24VDC Power supply
- Input devices
 - Preemption devices
 - Loop amplifiers
 - Video Detection
 - Microwave Detection
 - Radar Detection
 - AC isolators
 - DC isolators

- Output devices
 - Flasher units
 - Relays
 - Switch packs
- Conflict monitor
- Other equipment as noted in the special provisions required for the operation of an installation

8.2.2.2 Visually inspect solder connections on the back of the flash relays and output file. Solder connections shall be free of apparent defects such as shorts or cold joints.

8.2.2.3 Visually inspect cabinet construction, size, and wire harnessing for workmanship, and conformance to specifications.

8.2.2.4 Verify all screw fastener connections and attachments are properly secured to the assembly.

SECTION 3- OPERATIONAL TESTING

8.3.1 Requirements

8.3.1.1 The operational testing of traffic signal control equipment shall be performed at ambient temperature and nominal voltage of 120VAC. Testing includes specified control and non-control devices, such as, controller units, conflict monitors, switches, circuit breakers, and ground fault interrupts (GFIs). The devices will be visually observed during the test for proper input, output and control operation.

8.3.1.2 All equipment shall be unaffected by transient voltages normally experienced on a typical 120V electrical service. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in an Agency accepted cabinet.

8.3.2 Procedures

8.3.2.1 Wire the traffic signal control equipment to a test panel as identified in the plans and specifications of the traffic signal installation to model the traffic signal intersection.

8.3.2.2 Cut out proper diodes on the conflict monitor diode card as identified in plans and specifications of the traffic signal installation.

8.3.2.3 Apply configuration to the traffic signal controller, such as signal timing (supplied by signal timer), as identified in the plans and specifications of the traffic signal installation.

8.3.2.4 Inspect each of the following devices for proper operation.

- Switch packs
 1. Place a call into each phase by placing inputs from the cabinet's detector test panel.
 2. The outputs of the switch packs shall correspond with the indications shown on the controller.
- I & J Files
 1. Inspect each slot for proper DC and AC Voltage.
 2. DC Voltage output shall be 24 ± 0.5 VDC
 3. AC Voltage output shall be 120 ± 5 VAC
 4. Insert a DC isolator into a slot in the I & J File.
 - Toggle the upper channel switch on the DC isolator to place a call into the traffic signal controller. The traffic signal controller shall indicate the corresponding input.
 - Toggle the lower channel switch on the DC isolator to place a call into the traffic signal controller. The traffic signal controller shall indicate the corresponding input.
 - Repeat step 4 until all slots in the I & J file are tested.
 5. Place a call into each applicable phase of the traffic signal controller from the detector test panel. The outputs of the switch packs and conflict monitor shall correspond to the indications on the traffic signal controller.
- Flash switch (police panel/ cabinet) & flasher units
 1. Toggle the flash switch to the FLASH position. The signal shall go into flash and the controller shall go into STOPTIME.
 2. Inspect the flasher output for the proper flash sequence.
 3. Toggle the flash switch to the AUTO position. The controller shall restart in its startup phases.
- Signal power switch (police panel)
 1. Toggle the signal power switch to OFF. The signal indications on the switch packs shall turn OFF.
 2. Toggle the signal power switch to ON. The signal shall turn on to the current controller phase.
- DC power supply
 1. Check power supply voltage output with a multi-meter. The voltage output of the power supply shall be 24 ± 0.5 VDC.

2. Remove the AC fuse. The control equipment shall detect a VDC failure, signal shall go into flash.
 3. Verify the AC fuse is properly sized. Reinstall the AC fuse.
 4. Remove the DC fuse. The control equipment shall detect a VDC failure, signal shall go into flash.
 5. Verify the DC fuse is properly sized. Reinstall the DC fuse.
- Circuit breakers
 1. Toggle a single Signal Bus circuit breaker from ON to OFF, then back to ON. The signal shall go into flash.
 2. With the signal in flash, turn the flash bus breaker OFF. The signal shall turn OFF.
 3. Repeat steps 1 & 2 with each Signal Bus circuit breaker.
 - Power outlets
 1. Verify operation of Ground Fault Interrupt (GFI) outlets with a circuit tester. Press the test button. The Ground Fault Interrupt (GFI) outlet shall not have power.
 2. Verify operation of Non GFI outlets with a circuit tester. The Non GFI outlets shall have power with the GFI outlets tripped.
 3. Press the reset button. The Ground Fault Interrupt (GFI) shall be powered.
 - Fans
 1. Verify fan operation. Lower fan thermostat to a temperature lower than the ambient temperature. The fans shall turn on.
 2. Set fan thermostat to 90°. The fans shall turn off.
 - Front & Rear door switch and cabinet lighting fixture
 1. Open the cabinet door. The cabinet light fixture shall turn on.
 2. With the cabinet door open, push the cabinet door switch. The cabinet light fixture shall turn off.
 3. Remove and verify cabinet door switch fuse. The fuse shall have a current rating of 1 amp.

8.3.2.5 Verify the conflict monitor for proper operation.

- Auto conflict monitor test.
 1. Remove conflict monitor from the cabinet and place into a conflict monitor tester.
 2. Configure conflict monitor test to show permitted movements.
 3. Inspect test results for valid operations such as voltage monitoring, watchdog timer and permitted movements.
- Verify door switch trigger.
 1. Remove the conflict monitor.

2. Close the front cabinet door or push the front door switch. The signal shall go into flash.
 3. Reinstall and reset the conflict monitor.
- Conflicting field outputs.
 1. Reinstall conflict monitor into the cabinet.
 2. Jumper a field output that is active to a conflicting field output. The conflict monitor shall trip.
 3. Reset the conflict monitor.
 - Remove power supply.
 1. Remove the 24 VDC power supply from the cabinet. The conflict monitor shall trip.
 2. Reinstall the 24 VDC power supply and reset the conflict monitor.

8.3.2.6 Verify timing accuracy. Connect a timing device to monitor and record the accuracy of controller timing functions, such as minimum green, maximum green, walk, and yellow. Timing function accuracy shall be within ± 100 milliseconds of the programmed interval.

8.3.2.7 Verify proper simulated operation. Simulate inputs into the traffic control equipment by placing calls in the test panel. The equipment shall not exhibit non-specified or abnormal operations throughout testing.

SECTION 4- ENVIRONMENTAL TESTING

8.4.1 Requirements

8.4.1.1 The environmental testing of traffic signal control equipment consists of checking the ability of devices to operate as specified, under conditions of variable temperature and power supply.

8.4.1.2 All components shall be tested to operate within the following limits unless otherwise noted:

- Applied Line Voltage: 50 to 130 VAC
- Ambient Temperature: -30°F to +165°F

8.4.1.3 All components shall operate under the following environmental conditions and may be subjected to testing at the Agency's discretion:

- Line Voltage Spikes: +/- 300VAC
- Frequency: 60 (+/-3.0) Hertz
- Relative Humidity: 5 to 95 percent

8.4.2 Procedures

- 8.4.2.1** The control equipment will be set up in an environmental chamber. Testing, monitoring and simulation equipment will be connected to the control equipment and configured according to the plans and specifications of the installation. Apply configuration to the traffic signal controller and cut out proper diodes in the conflict monitor if it has not been done previously in the Operational Test.
- 8.4.2.2** All plug-in devices other than loop amplifiers such as preemption devices, switch packs and DC isolators shall be installed in the cabinet assembly for testing. Install and configure emergency vehicle preemption devices per manufacturer's instructions and place calls into each emergency vehicle preemption device with an Agency approved transmitter on a random basis throughout testing to verify proper operation. Loop amplifiers are to be removed from the cabinet assembly and tested in the designated loop amplifier tester inside the environmental chamber. The loop amplifiers will be inspected on a random basis during testing to verify proper operation. The control equipment will be allowed to stabilize in the environmental chamber for at least 30 minutes before testing.
- 8.4.2.3** The control equipment will be subjected to a variable voltage test. An external power supply will be connected to the input power of the control equipment. The voltage will be adjusted from 120 VAC down to 0 VAC at a maximum rate of 20V per second. The equipment shall operate normally, with the exception of the watchdog monitor, down to 90 VAC or below. The watchdog monitor shall operate normally down to 98 ± 2 VAC. The equipment must shut off and shall not exhibit non-specified or abnormal operations below the unit's minimum operating voltage. The power supply voltage will then be adjusted from 0 VAC back up to 120 VAC at a maximum rate of 20V per second. The control equipment shall, with the exception of the watchdog monitor, resume normal operation at or below 95VAC. The watchdog monitor shall resume normal operation at 103 ± 2 VAC.
- 8.4.2.4** The control equipment will be subjected to a variable temperature test. The control equipment will be cycled through temperatures from a range of -30°F to 165°F with a supply voltage of 90VAC in an environmental chamber. The rate of temperature change shall not exceed 30°F per hour. The control equipment shall operate for a maximum of 12 hours at both the high and low temperature limits. The test will be repeated with a supply voltage of 135VAC. During operations at the high and low temperature limits, the operation of the control equipment unit and timing functions shall be monitored for proper operation.

8.4.2.5 A voltage spike test will be performed at the agency's discretion. The test will synchronously add ± 300 V voltage spikes into the supply power of the control equipment. The equipment is observed for any disruption to normal operation.

SECTION 5- EQUIPMENT ACCEPTANCE PROCEDURES

8.5.1 Failures

8.5.1.1 A failure shall be defined as any occurrence that results in non-specified operation of the equipment.

8.5.1.2 If a failure occurs at any step in the test – physical, environmental, or operational – the Contractor, and/or Representative will be permitted to make on-site repairs within five (5) days after notification of the malfunction. The test will then be resumed at the beginning of the category in which the malfunction occurred.

8.5.1.3 Failure to make repairs within five (5) days after notification shall result in rejection at the Agency's discretion.

8.5.1.4 If the traffic signal control equipment fails twice in the same category, the equipment shall be rejected.

8.5.2 Control Equipment Rejection

8.5.2.1 When traffic signal control equipment is rejected, items shall be picked up by the Contractor within 10 days after notification. If the rejected equipment is not picked up after 10 days, the items shall be returned, freight collect, to the Contractor.

8.5.2.2 New equipment, having a different serial number, must then be submitted for testing. Rejected equipment shall not be accepted for subsequent testing or installations within the State of Oregon.

8.5.3 Control Equipment Acceptance

8.5.3.1 The traffic signal control equipment which successfully passes the testing procedure will be certified by the Agency as acceptable for installation only.

8.5.3.2 The Contractor will be notified when the testing has been completed and shall pick up the cabinet assembly excluding plug-in devices such as controller units, input devices, switch packs at the test facility.

8.5.3.3 The successful completion of the testing does not relieve the Contractor of equipment warranty obligations and the responsibility to furnish a complete working signal installation at the time the equipment is placed in operation.

8.5.4 Testing Results

8.5.4.1 A copy of the chamber approval letter will be sent to the Contractor and Project Manager.

8.5.4.2 A copy of the Green Sheets will be sent to the Contractor and Project Manager.

8.5.5 Control Equipment Installation

8.5.5.1 The Contractor shall pick-up, deliver and install the controller cabinet.

8.5.5.2 The Agency will be responsible for delivery and installation of the control equipment, such as controller units, input devices, switch packs, monitor units, miscellaneous plug-in devices and auxiliary devices not physically wired to the controller cabinet.

8.5.5.3 Control equipment and other miscellaneous equipment that the Agency is to install will be stored at the test facility until the signal installation is ready to be turned on

SECTION 6- AGENCIES OTHER THAN ODOT

8.6.1 Requirements

8.6.1.1 The testing will be done at the expense of the agency requesting the testing.

8.6.1.2 The following information shall be included with equipment shipments:

- Contractor
- Supplier
- Manufacturer
- Location
- Agency for which the equipment is to be tested.
- A complete set of plans and specifications to which the equipment is to be tested (List items to be tested along with testing procedures if not on ODOTs QPL)

8.6.1.3 Wire the traffic signal control equipment to a test panel as identified in the plans and specifications of the traffic signal installation to model the traffic signal intersection.

- 8.6.1.4** Cut out proper diodes on the conflict monitor diode card as identified in plans and specifications of the traffic signal installation. Guidance shall be given upon request for non-standard intersection phasing.
- 8.6.1.5** Apply configuration to the traffic signal controller, such as signal timing, as identified in the plans and specifications of the traffic signal installation. (Signal timing shall be supplied by signal timer)
- 8.6.1.6** Upon request, other agencies shall verify proper simulated operation.
- 8.6.1.7** ODOT will return all tested control equipment to the local agency. The local agency will be responsible for delivery and installation of the control equipment, within the controller cabinet.

SECTION 7- TRAFFIC SIGNAL FIELD INSPECTION AND TURN ON

8.7.1 Field Inspection

- 8.7.1.1** A field inspection of traffic signal installations will be performed by Agency electrical crews. The contractor shall notify the Engineer one week in advance of the anticipated signal completion date. The Engineer will notify the Agency's Traffic Systems Services Unit and the Agency's electrical crew of the anticipated completion date. Field inspections will be performed within one week following the date of completion. The Engineer will notify the Contractor of the inspection results and identify necessary corrections.

8.7.2 Roles and Responsibilities

- 8.7.2.1** The Engineer will coordinate with the Agency's Traffic Systems Services Unit and region electrical crew to establish the date and time the installation is to be turned on and inspected in accordance with the Inspection Checklist below. The Agency will turn on the signal within one week after completion of corrections identified in the field inspection.
- 8.7.2.2** The Contractor shall be present at the project site during turn-on to assist and make additional corrections as necessary.
- 8.7.2.3** After traffic signals are turned on and operating as designed, the Agency ultimately responsible for maintenance will assume operation and maintenance of the signal. Turn-on does not constitute final approval. The contractor is still obligated to finish any incomplete portion of the installation and correct problems with workmanship or replace material that does not meet the plans and specifications of the installation. After turn-on, damage to the traffic signal

installation caused by conditions beyond the Contractor's control will be the responsibility of the maintaining agency.

8.7.3 Inspection Procedures

8.7.3.1 Perform the following tasks prior to energizing the cabinet:

- Inspect the service cabinet for secured terminal screws and proper bonding.
- Verify cabinet grounding by measuring and recording the resistance between earth ground and the isolated and system grounds of the cabinet.
- Verify the cabinet is mounted securely with caulking and gaskets installed.
- Inspect the interior terminal screws and solder connections of the Power Distribution Assembly.
- Verify the breakers in the Power Distribution Assembly are in the OFF position.
- Inspect all cabinet terminal screws and field wiring. All field wiring shall be neat and secure.
- Inspect the output file for secure terminals and proper flash plugs.
- Verify the fan thermostat is set at 90°.
- Check pedestrian buttons for proper phasing.
- Verify the loop bleed wires are grounded.
- Verify lead-in wires are soldered and shielded within 6" of terminations.

8.7.3.2 Perform the following tasks after the cabinet is energized.

- Verify the cabinet supply voltage and then turn on the main breaker.
- Check ground buses with a 1000W lamp.
- Verify loop placement against cabinet print with a loop finder.
- Check signal circuits with a 1000W lamp and verify proper phasing.
- Install cabinet equipment in accordance with cabinet print.
- Check controller for proper start up.

8.7.3.3 Manual conflict monitor test.

- Remove conflict monitor from the cabinet and place into a manual tester.
- Turn on all yellow switches on the manual tester. Yellow lights shall not be lit unless otherwise specified in the plans and specifications.
- Verify DC Voltage. The voltage shall be between 15VDC and 25VDC.
- Turn on the Watchdog disable switch. The conflict monitor shall not trip.
- Turn off the Watchdog disable switch and the Watchdog timer switch. The conflict monitor shall trip.
- Turn on the Watchdog disable switch.

- Decrease the AC voltage to 96.5V.
- Turn the Watchdog timer off.
- Increase the AC voltage until the conflict monitor trips. The conflict monitor shall trip at 103 ± 2 VAC.
- Reinstall the conflict monitor.

8.7.3.4 Verify door switch trigger.

- Remove the conflict monitor.
- Close the front cabinet door. The signal shall go into flash.
- Reinstall and reset the conflict monitor.

8.7.3.5 Conflicting field outputs.

- Reinstall conflict monitor into the cabinet.
- Jumper a field output that is active to a conflicting field output. The conflict monitor shall trip.
- Reset the conflict monitor.

8.7.3.6 Remove power supply.

- Remove the 24 VDC power supply from the cabinet. The conflict monitor shall trip.
- Reinstall the 24 VDC power supply and reset the conflict monitor.

8.7.3.7 Verify flash switch (police panel/ cabinet) & flasher units.

- Toggle the flash switch to the FLASH position. The signal shall go into flash and the controller shall go into STOPTIME.
- Inspect the flasher output for the proper flash sequence.
- Toggle the flash switch to the AUTO position. The controller shall restart in its startup phases.

8.7.3.8 Verify signal power switch (police panel).

- Toggle the signal power switch OFF. The signal shall be dark.
- Toggle the signal power switch ON. The signal shall turn on to the current controller phase.

8.7.3.9 Verify and adjust emergency preemption.

- Place a preemption call into each channel of the preemption device with an Agency approved preemption transmitter.

- Observe the preemption calls into the traffic signal controller. The preemption calls shall correspond with the indications shown on the controller.

8.7.3.10 Verify railroad preemption where applicable.

- Remove the AC isolator from the cabinet. A railroad preemption call shall be indicated on the traffic signal controller.
- Verify proper clearout and controller phasing.
- Verify proper operation of part time restriction signs where applicable.
- Reconnect incoming power to the AC isolator. The railroad preemption call shall terminate when the AC isolator is reconnected and normal traffic controller operation shall resume.

8.7.3.11 Inspect the following general items.

- Inspect the bond wires from spans to poles where applicable.
- Verify the signal cable is secured to a messenger where applicable.
- Verify the tether wires are tight where applicable.
- Verify proper connections to signal heads and poles.
- Visually inspect mast arms.
- Verify and record cabinet AC voltage.
- Verify and record cabinet DC voltage at the 24VDC power supply.
- Verify and record cabinet current draw.
- Verify a TS1/ TS2 key core is installed.
- Verify the controller timing corresponds to the plans and specifications of the traffic signal installation.

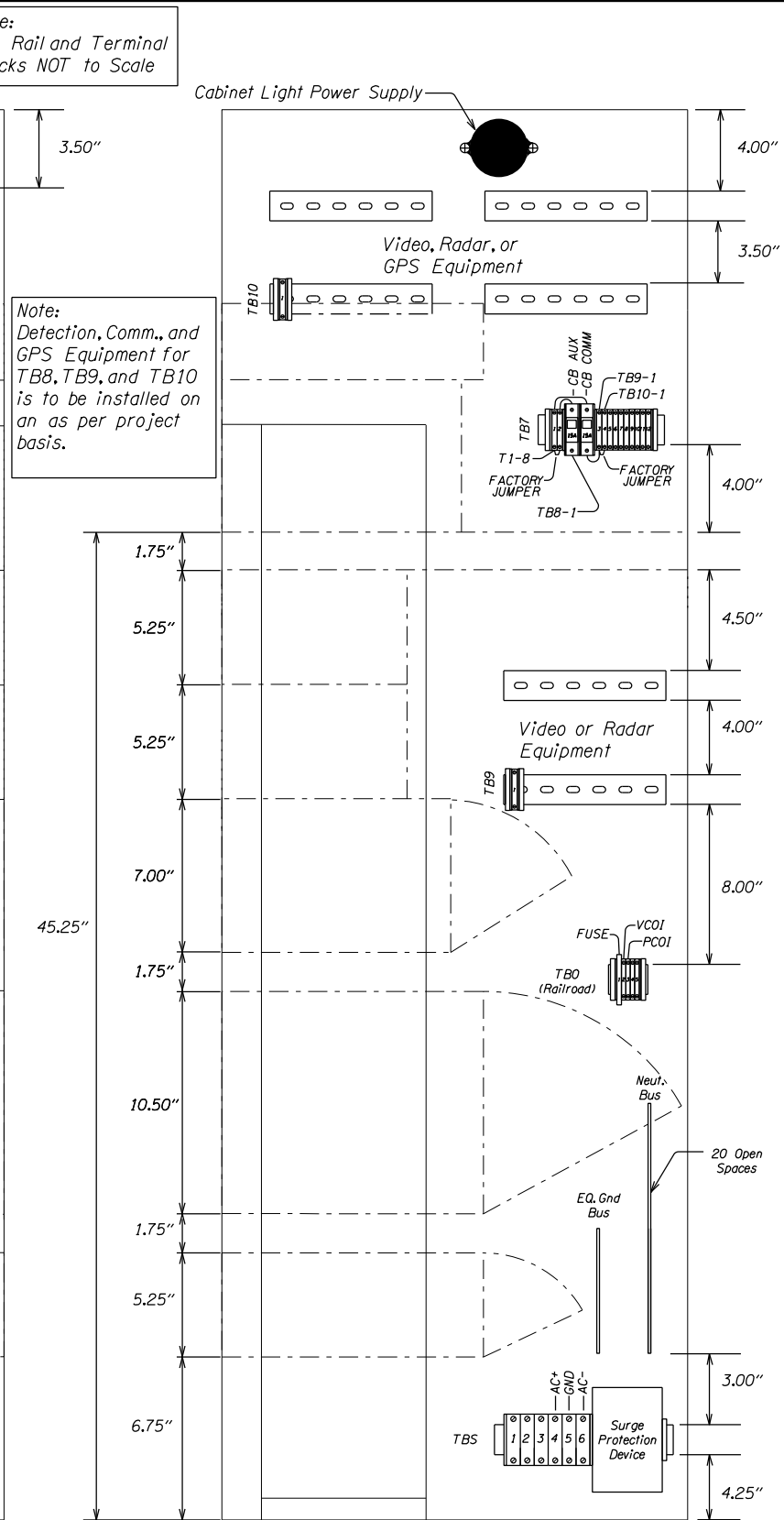
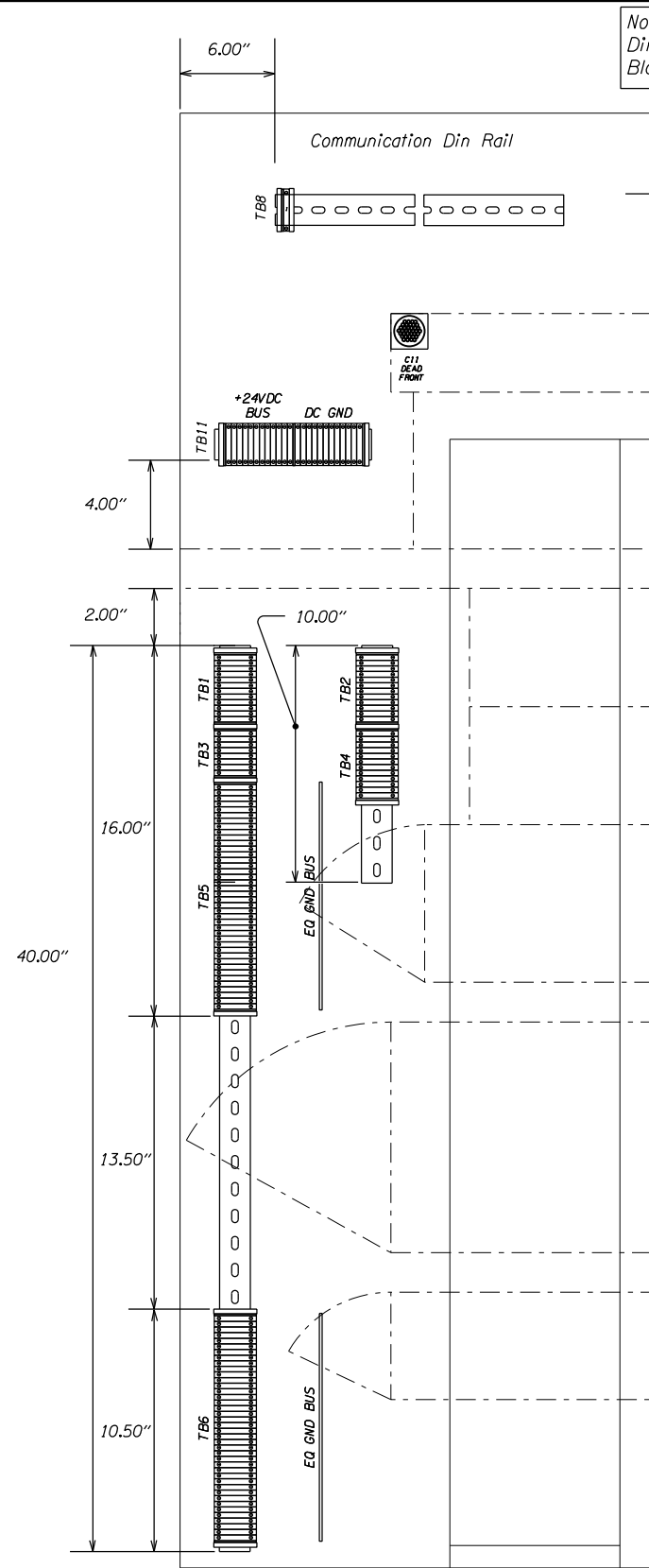
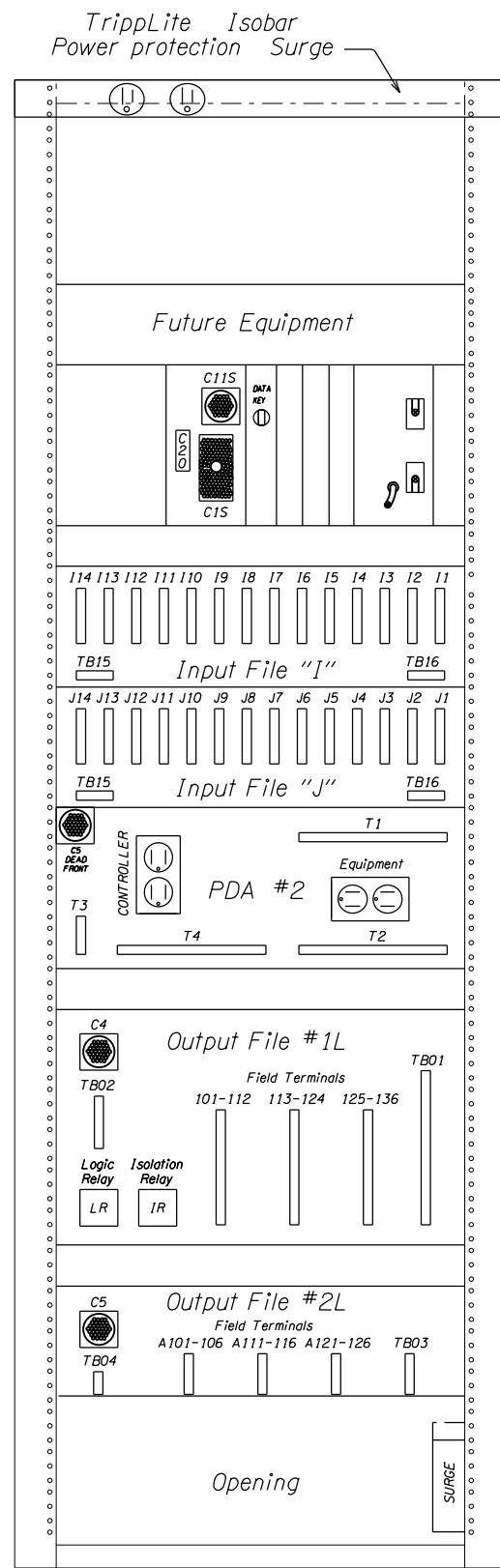
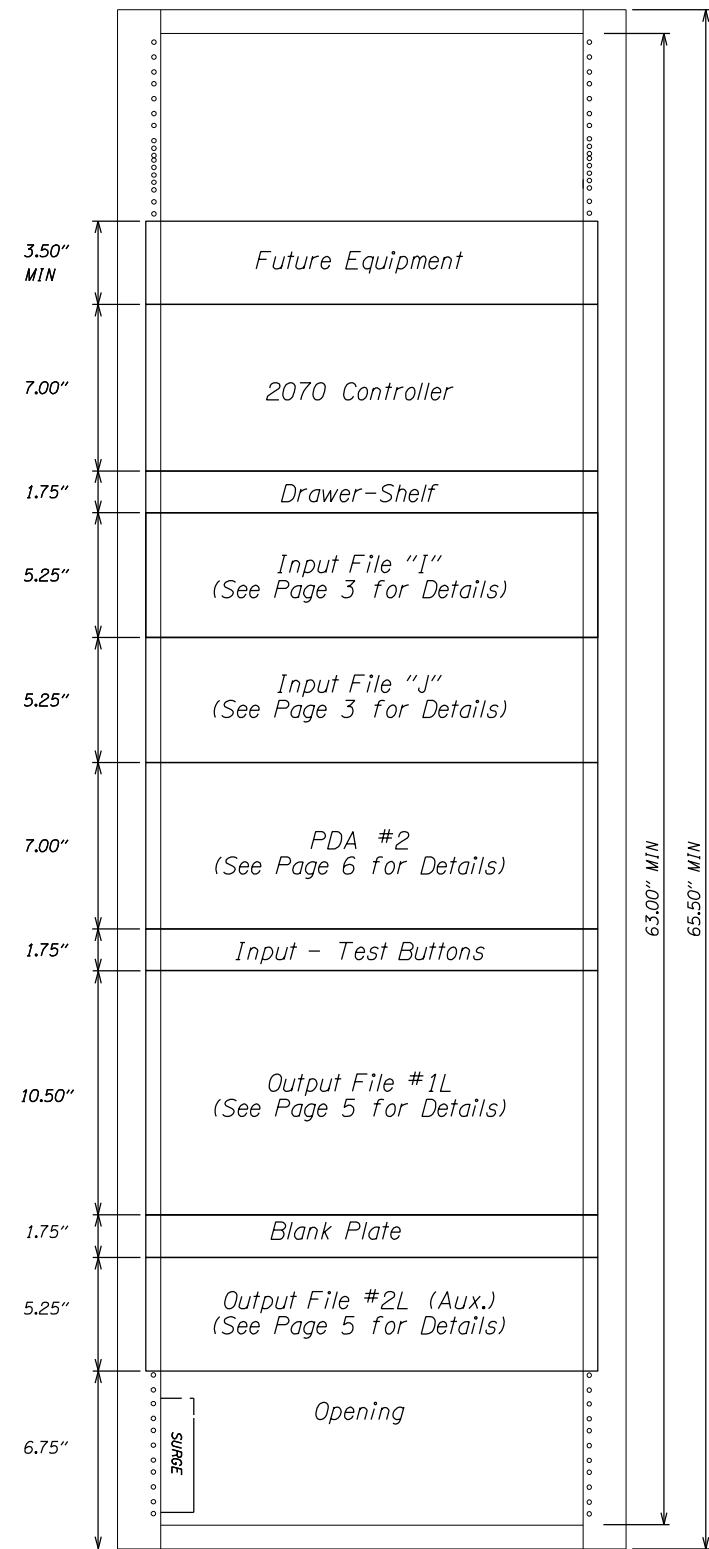
APPENDIX A: 332S CABINET PRINT

APPENDIX B: COMMUNICATIONS BRACKET

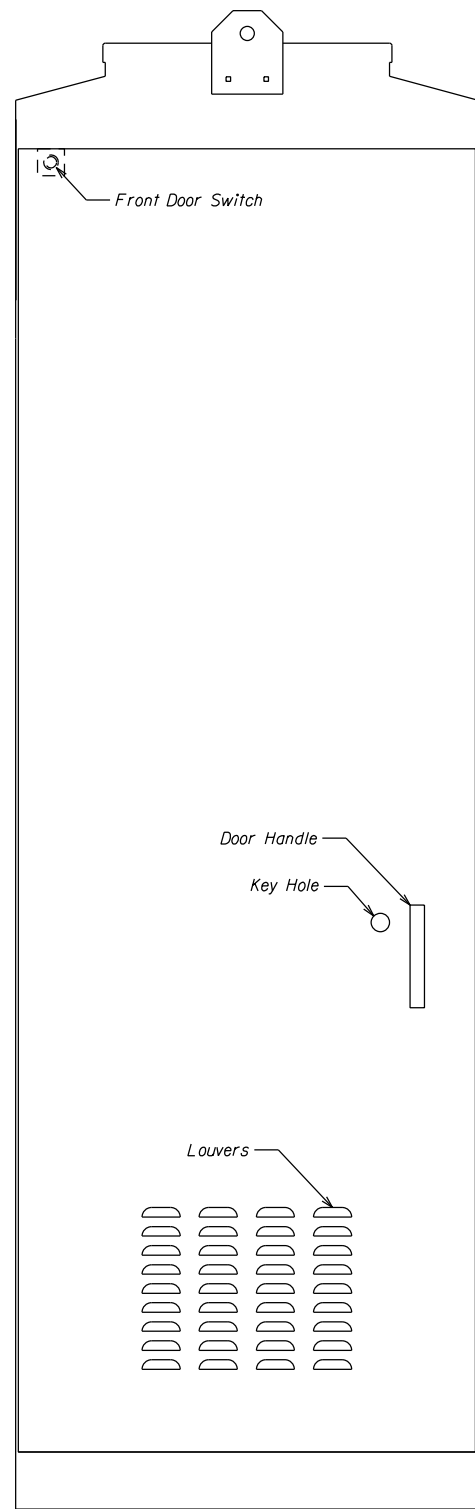
**APPENDIX C: ODOT STANDARD SPECIFICATION FOR MICROCOMPUTER
SIGNAL CONTROLLER, SEPTEMBER 4, 2001 AMENDED**

APPENDIX D: CAL TRANS TEES

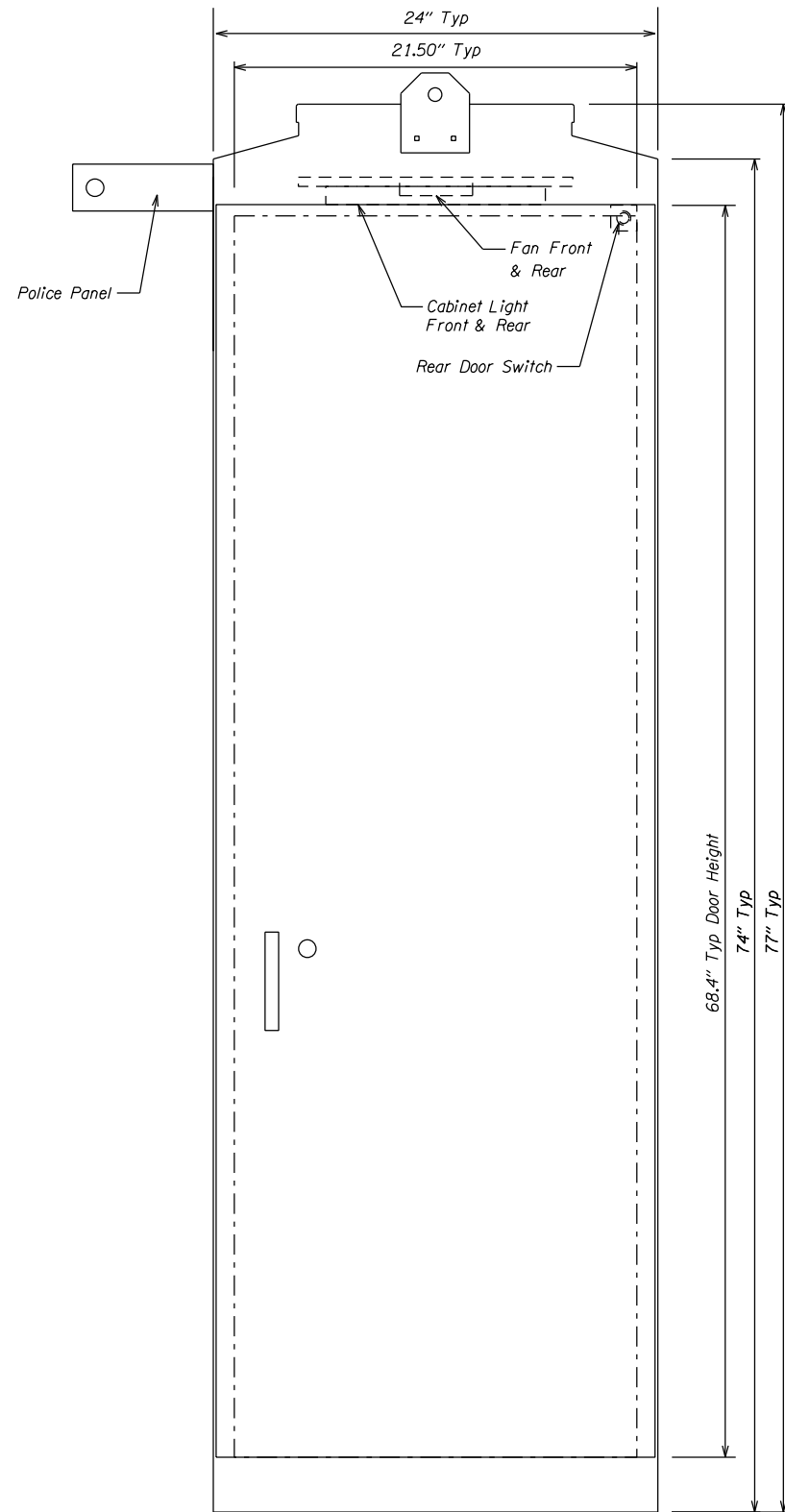
Appendix A



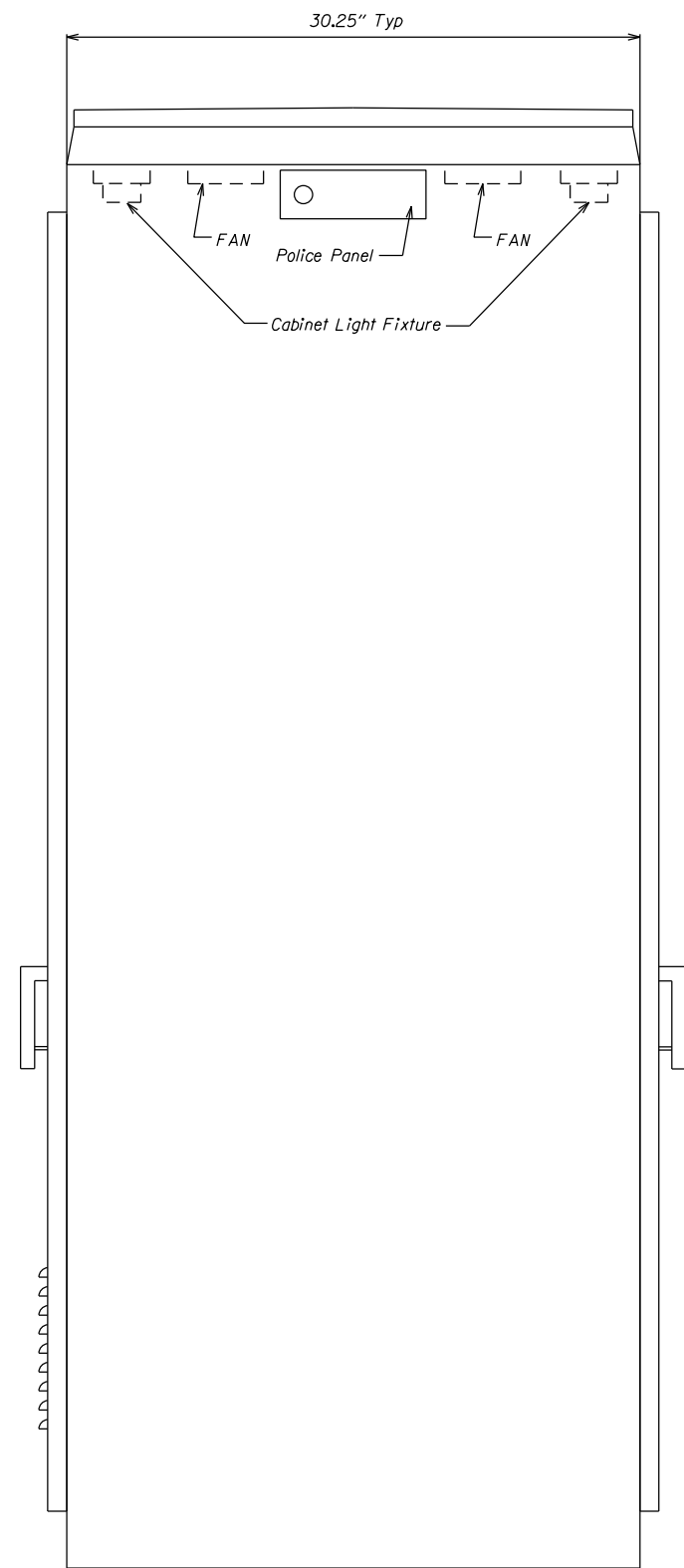
PAGE 1 of 6	332S ODOT STRETCH CABINET HOUSING	REV. NO.	DATE	INITIAL	REMARKS	INTERSECTION: _____	OREGON DEPARTMENT OF TRANSPORTATION TRAFFIC - ROADWAY SECTION 332S ODOT CABINET PRINT 07/01/2014 V-1.9
						HWY*: _____ M.P.*: _____ TSSU ID*: _____	



332S ODOT STRETCH CABINET
(FRONT VIEW)

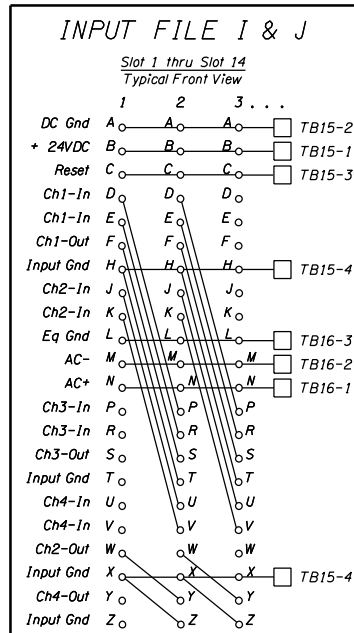


332S ODOT STRETCH CABINET
(REAR VIEW)



332S ODOT STRETCH CABINET
(RIGHT SIDE VIEW)

REV. NO.	DATE	INITIAL	REMARKS

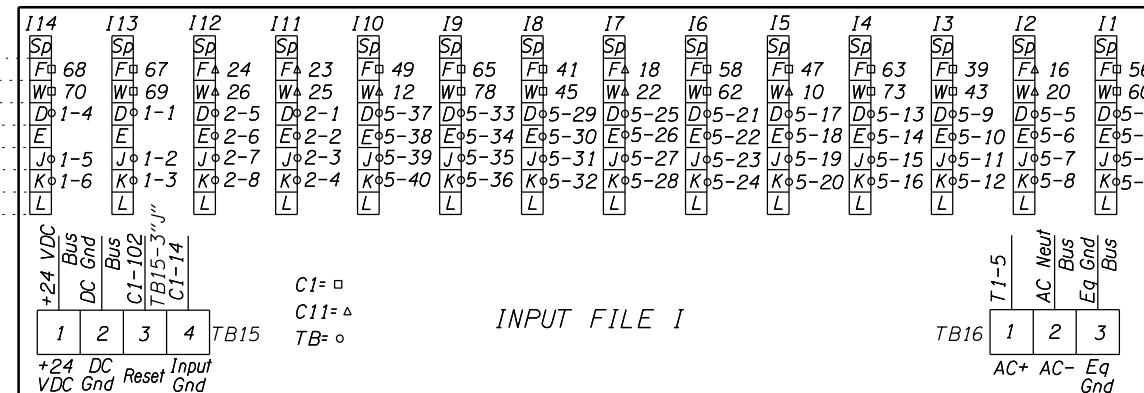


INPUT FILE - WIRING
TYPICAL WIRING DETAILS

11	12	13	14	15	16	17	18	19	110	111	112	113	114
φ 1 C1-56	φ 1 C11-16	φ 2 C1-39	φ 2 C1-63	φ 2 C1-47	φ 3 C1-58	φ 3 C11-18	φ 4 C1-41	φ 4 C1-65	φ 4 C1-49	SPARE C11-23	SPARE C11-24	2 PED C1-67	6 PED C1-68
φ 1 C1-60	φ 1 C11-20	φ 2 C1-43	φ 2 C1-76	φ 2 C11-10	φ 3 C1-62	φ 3 C11-22	φ 4 C1-45	φ 4 C1-78	φ 4 C11-12	SPARE C11-25	SPARE C11-26	4 PED C1-69	8 PED C1-70
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14
φ 5 C1-55	φ 5 C11-15	φ 6 C1-40	φ 6 C1-64	φ 6 C1-48	φ 7 C1-57	φ 7 C11-17	φ 8 C1-42	φ 8 C1-66	φ 8 C1-50	SPARE C1-54	PCOI C1-51	EVA C1-71	EVB C1-72
φ 5 C1-59	φ 5 C11-19	φ 6 C1-44	φ 6 C1-77	φ 6 C11-11	φ 7 C1-61	φ 7 C11-21	φ 8 C1-46	φ 8 C1-79	φ 8 C11-13	GPS C1-75	VCOI C1-52	EVC C1-73	EVD C1-74

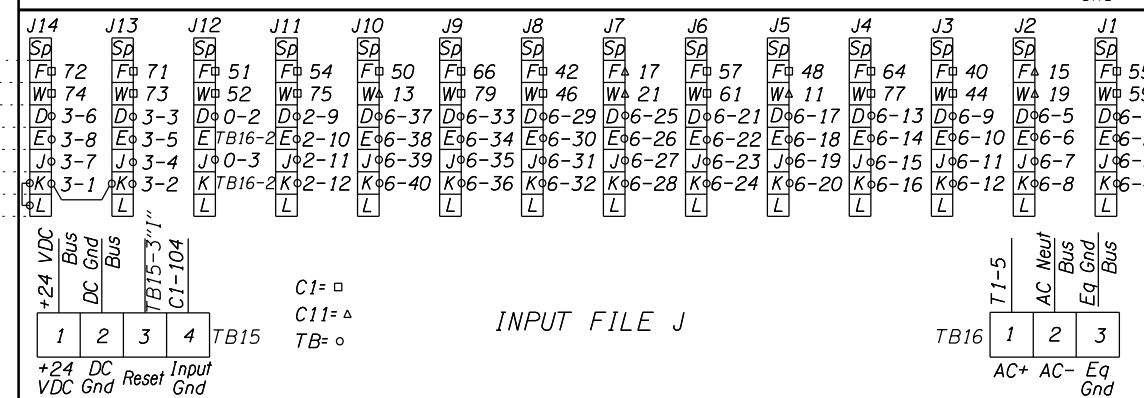
INPUT FILE I & J (FRONT VIEW)
(NOT TO SCALE)

TYPICAL TERMINALS
Spare
Ch1-Output
Ch2-Output
Ch1-Input
Ch1-Input
Ch2-Input
Ch2-Input
Equip Gnd



INPUT FILE I

TYPICAL TERMINALS
Spare
Ch1-Output
Ch2-Output
Ch1-Input
Ch1-Input
Ch2-Input
Ch2-Input
Equip Gnd



INPUT FILE J

INPUT FILE I & J (REAR VIEW)
(NOT TO SCALE)

Ph	TB1
Ph	1
Ph	2
PB Common	3
Ph	4
Ph	5
PB Common	6
Flash Sense	7
Stop Time	8
Monitor Reset	9
Advance	10
Adv. Enable	11
NC	12

Spare	TB2
Spare	1
Spare	2
Spare	3
Spare	4
Spare	5
Spare	6
Spare	7
Spare	8
Spare	9
Spare	10
Spare	11
Spare	12

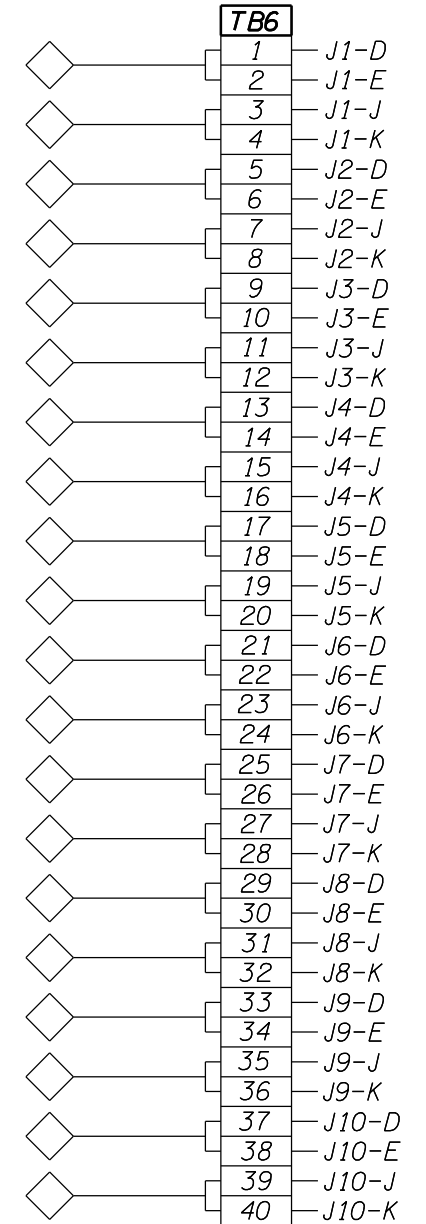
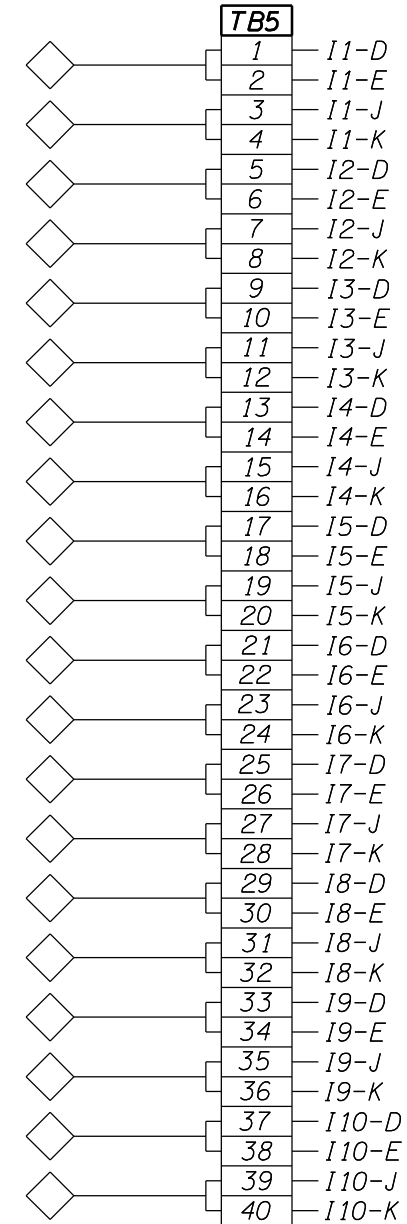
Det DC GND	TB3
Det DC GND	1
Det DC GND	2
EVA	3
EVC	4
Det+24VDC	5
EVB	6
EVD	7
Det+24VDC	8

Det DC Gnd	TB4
Det DC Gnd	1
Det+24VDC	2
2nd Det	3
3rd Det	4
2nd Det	5
3rd Det	6
Det DC Gnd	7
Det+24VDC	8
2nd Det	9
3rd Det	10
2nd Det	11
3rd Det	12

RR AC+	TB0*
RR AC+	1
PCOI	2
VCOI	3

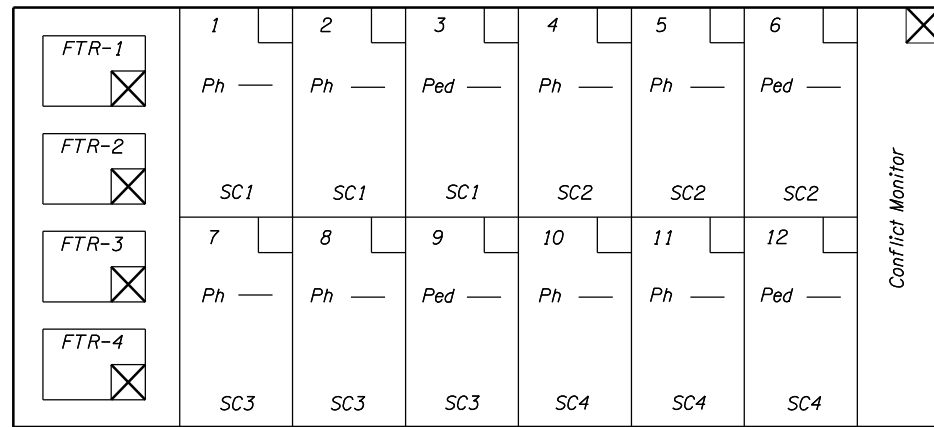
*NOTE - See Page 6 For
Railroad Interconnect
Wiring Details

TERMINAL BLOCK DEFINITIONS	
TB0	- Railroad
TB1	- PEDS & Controller
TB2	- Spares
TB3	- EV Preemption
TB4	- AUX EV Preemption
TB5	- I File Loop Feeders
TB6	- J File Loop Feeders

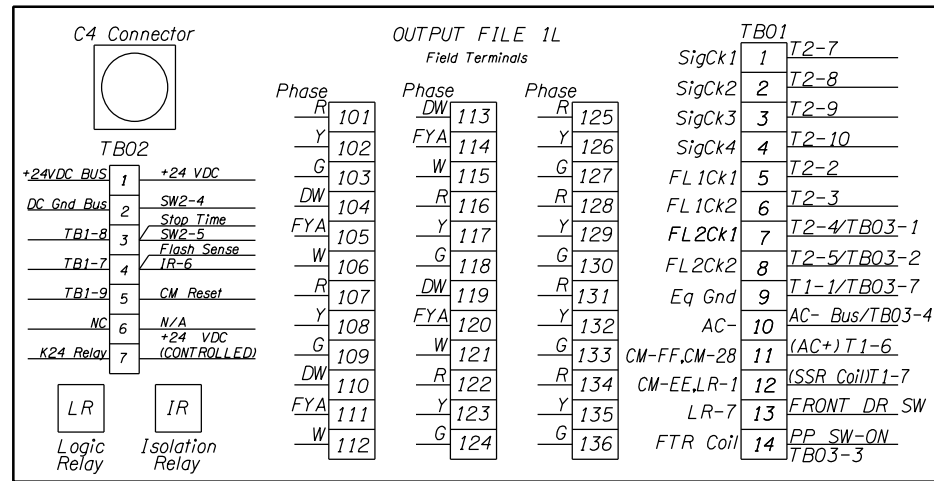


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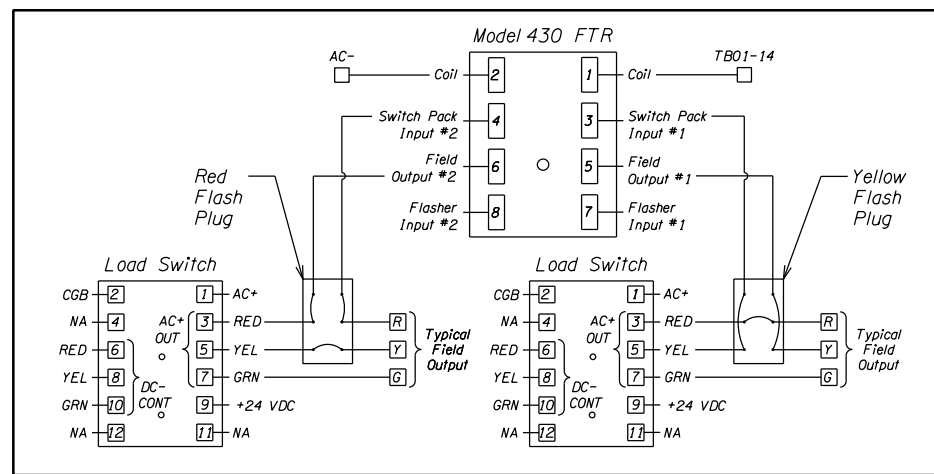
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OUTPUT FILE 1L (FRONT VIEW)
(NOT TO SCALE)



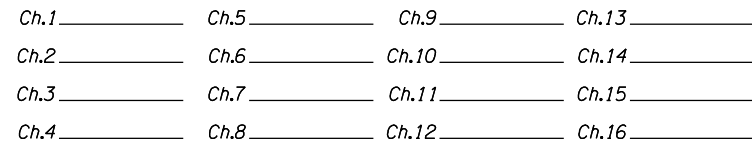
OUTPUT FILE 1L (REAR VIEW)
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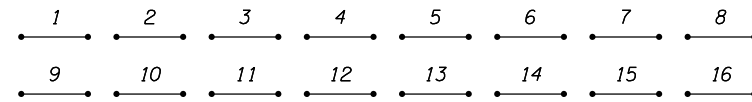
FIELD OUTPUTS - TYPICAL WIRING

CONFLICT MONITOR DIODE CARD

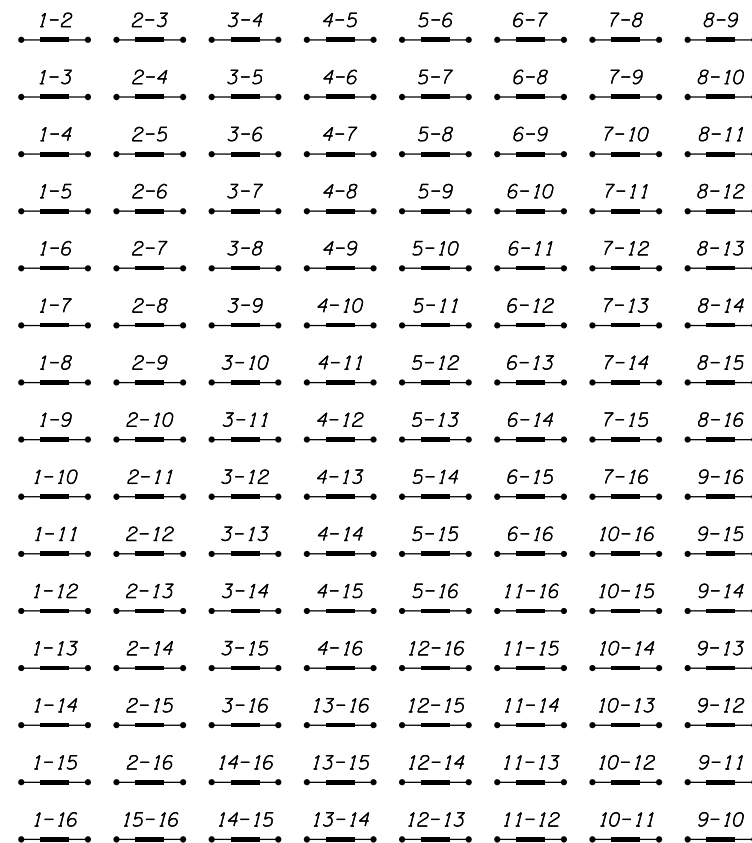
CHANNEL ASSIGNMENT



YELLOW INHIBIT JUMPERS



DIODES - Diode Removed Makes Movement Allowable (Diode IN4148)

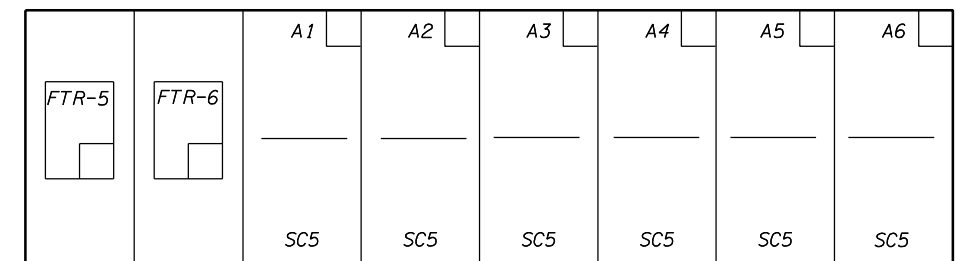


CONFLICT MONITOR DIODE CARD CUTOUT
(NOT TO SCALE)

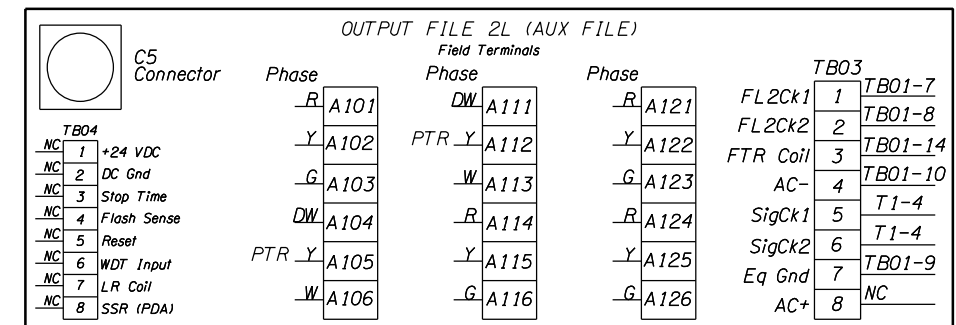
CONFLICT MONITOR - TYPICAL CONNECTOR PIN ASSIGNMENTS

Term	Function	Pin	Ch	PH	Pin	Function	Term		
130	SP2-G	1			A	SP2-Y	129		
115	SP3-W	2			B	SP8-G	136		
135	SP8-Y	3			C	SP9-W	121		
103	SP5-G	4			D	SP5-Y	102		
106	SP6-W	5			E	SP11-G	109		
108	SP-11Y	6			F	SP12-W	112		
133	SP7-G	7			H	SP7-Y	132		
114	SP3-Y (FLTYA)	8			J	SP1-G	127		
126	SP1-Y	9			K	SP9-Y (FLTYA)	120		
124	SP10-G	10			L	SP10-Y	123		
105	SP6-Y (FLTYA)	11			M	SP4-G	118		
117	SP4-Y	12			N	SP12-Y (FLTYA)	111		
A123	ASP1-G	13			P	NC	-		
-	NC	14			8	8	R	ASP2-G	A126
-	T&B	15			9	OLA	S	ASP4-G	A116
-	T&B	16			10	OLB	T	NC	-
-	NC	17			11	OLC	U	T&B	-
-	T&B	18			12	OLD	V	ASP5-G	A103
-	NC	19			13	2PED	W	NC	-
TB01-9	EQ Gnd	20			13	φ1 FLTYA	X	NC	-
TB01-10	AC-	21			14	4PED	Y	DC Gnd	TB02-2
C4-37	Watch Dog	22			14	φ3 FLTYA	Z	Ext. Reset	TB02-5
TB02-1	+24VDC	23			15	6PED	AA	T&B	-
LRCoIL	Interlock	24			15	φ5 FLTYA	BB	Stop Time	TB02-3
TB02-2	Interlock	25			16	8PED	CC	NC	-
-	NC	26				φ7 FLTYA	DD	NC	-
-	NC	27					EE	Clapper	TB01-12
TB01-11	Norm. Closed	28					FF	AC+	TB01-11

CONFLICT MONITOR - TYPICAL WIRING
(NOT TO SCALE)

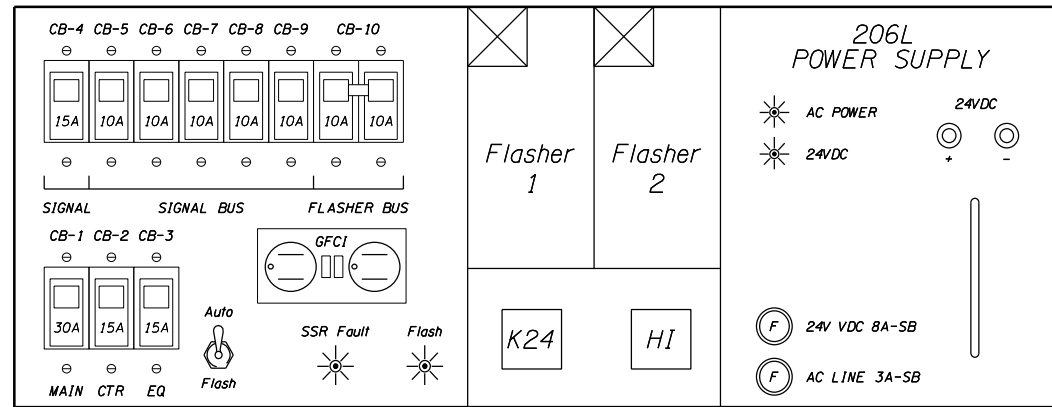


OUTPUT FILE 2L (AUX FILE)
FRONT VIEW - (NOT TO SCALE)

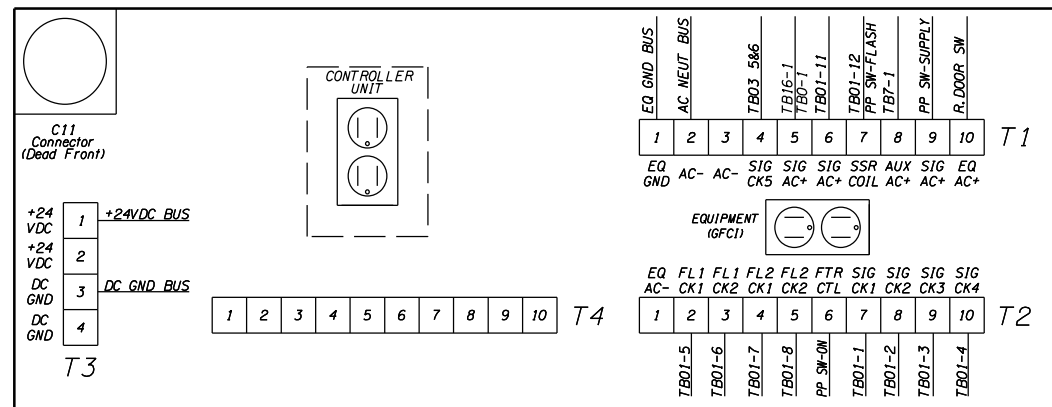


OUTPUT FILE 2L (AUX FILE)
REAR VIEW - (NOT TO SCALE)

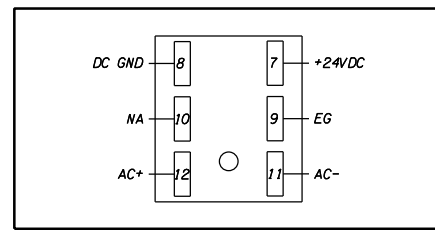
REV. NO.	DATE	INITIAL	REMARKS



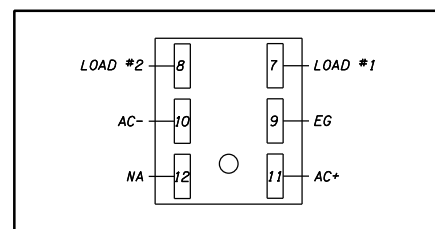
ODOT PDA 2 LAYOUT (FRONT VIEW)
(NOT TO SCALE)



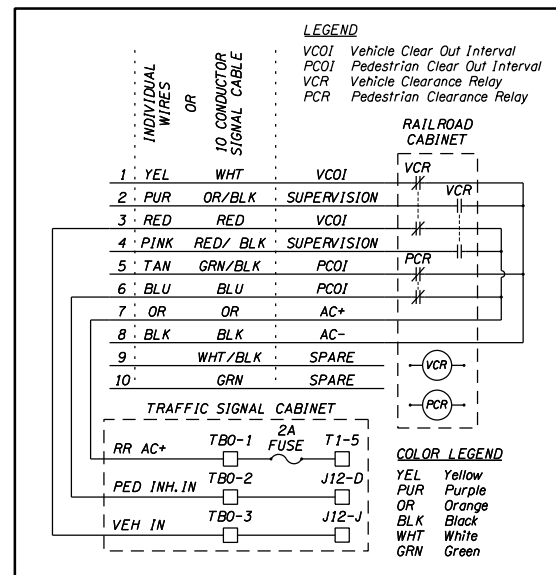
ODOT PDA 2 LAYOUT (REAR VIEW)
(NOT TO SCALE)



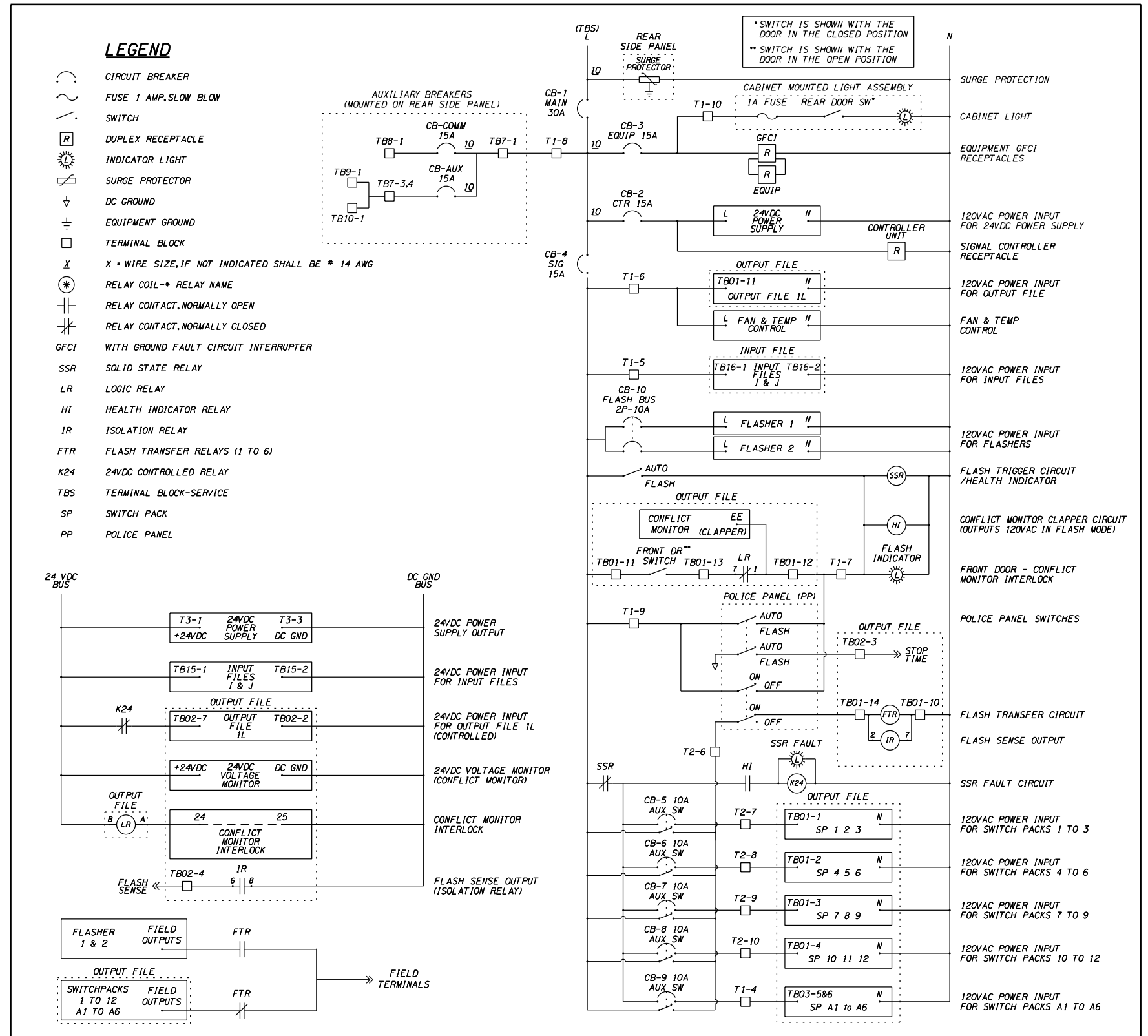
MODEL 206L POWER SUPPLY
TYPICAL CONNECTOR DETAIL



MODEL 204 FLASHER
TYPICAL CONNECTOR DETAIL

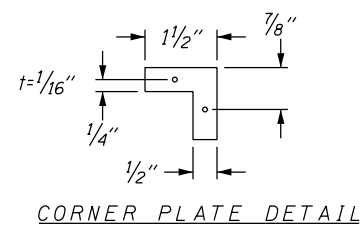
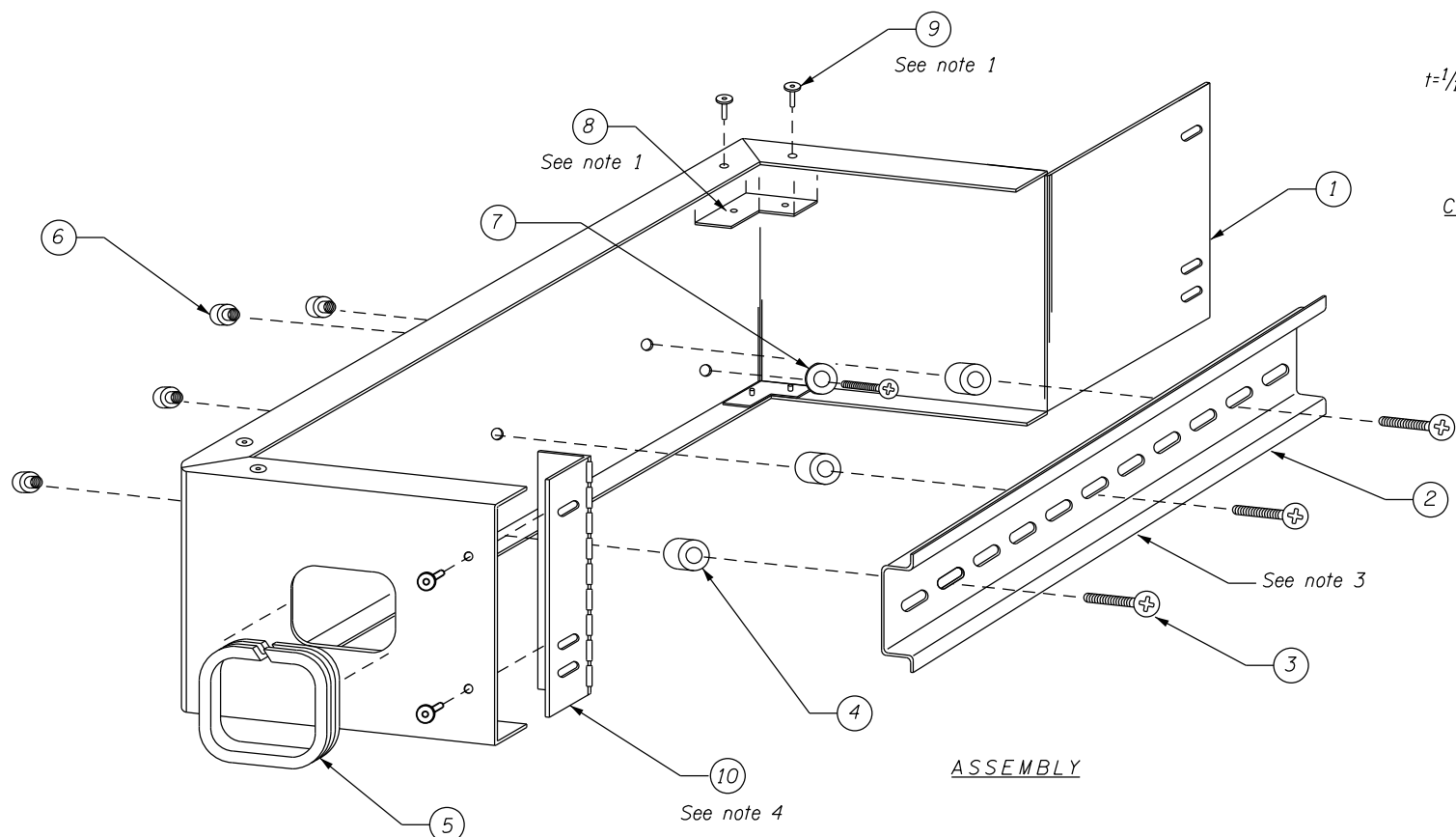


RAILROAD INTERCONNECT
TYPICAL WIRING DETAILS



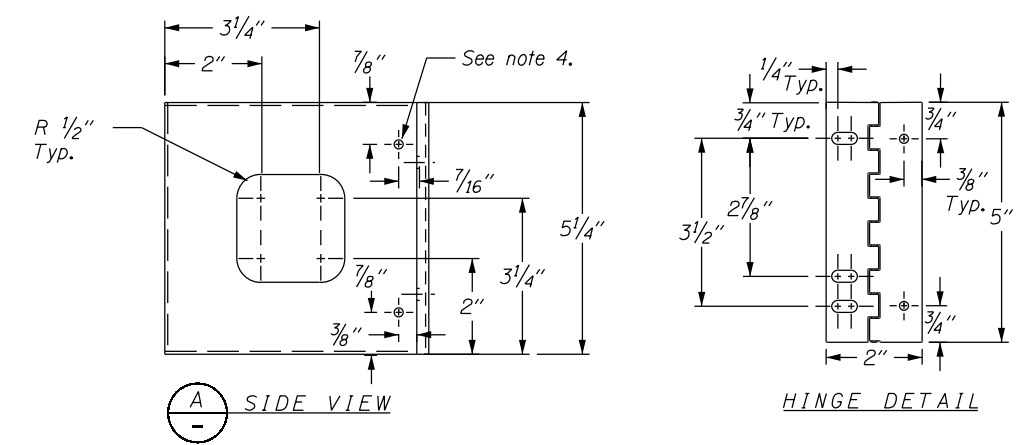
PDA #2 ELEMENTARY DIAGRAM
TYPICAL WIRING DETAILS

Appendix B



Item No.	Part	Material	Qty.
1	Rack frame	Alum. plate 5052 H-32, 1/16"	1
2	"35mm x 15mm" DIN Rail, pre-punched, 13" long	Electrolytically plated steel	1
3	10-32 x 3/4" Pan head machine screw	Type 304 Stainless	3
4	Spacer, 5/8" deep x 1/4" I.D. x 5/8" O.D.	Aluminum or HDPE	3
5	Polyethylene adhesive lined grommet edging	Polyethylene	2
6	10-32 Self clinching sheet metal nut	Type 304 Stainless	4
7	10-32 x 1/2" Green bonding screw w/ washer	Type 304 Stainless	1
8	Corner plate	Alum. plate 5052 H-32, 1/16"	4
9	3/32" dia. blind rivet, button head	Aluminum	10
10	2" W x 5" L x 1/16" Th Piano Hinge, 1/8" Pin	Type 304 Stainless	1

ASSEMBLY

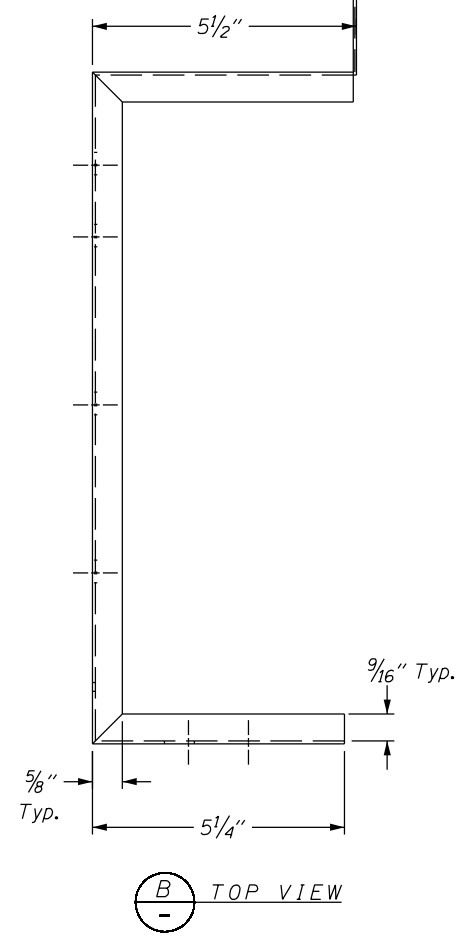


General notes:

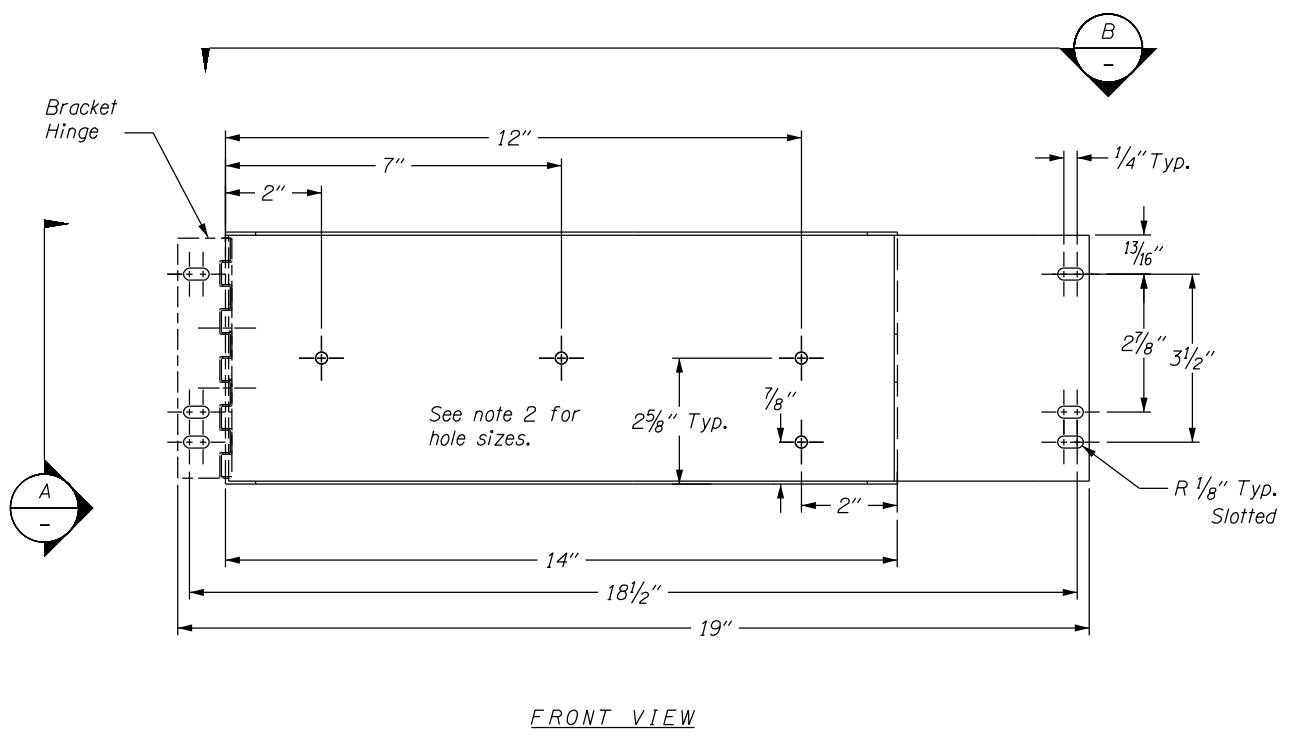
1. Fabricate rack frame using bends of single aluminum sheet.
2. Inside minimum bend radii are 1/32".
3. Remove all sharp corners.
4. All dimensional tolerances are +/- 1/32".
5. See other sheet for component assembly.

Notes:

1. Drill/punch and blind rivet corner plates on each inside corner.
2. Drill/punch holes as required to secure self clinching metal nuts.
3. Pre-punched DIN rail may be substituted with solid DIN rail. Drill thru holes as necessary for 10-32 screws.
4. Drill/punch and blind rivet stainless steel piano hinge to rack frame such that hinge opens in the clockwise direction as seen from top. Use 3/32" diameter blind rivet button head as shown.



TOP VIEW



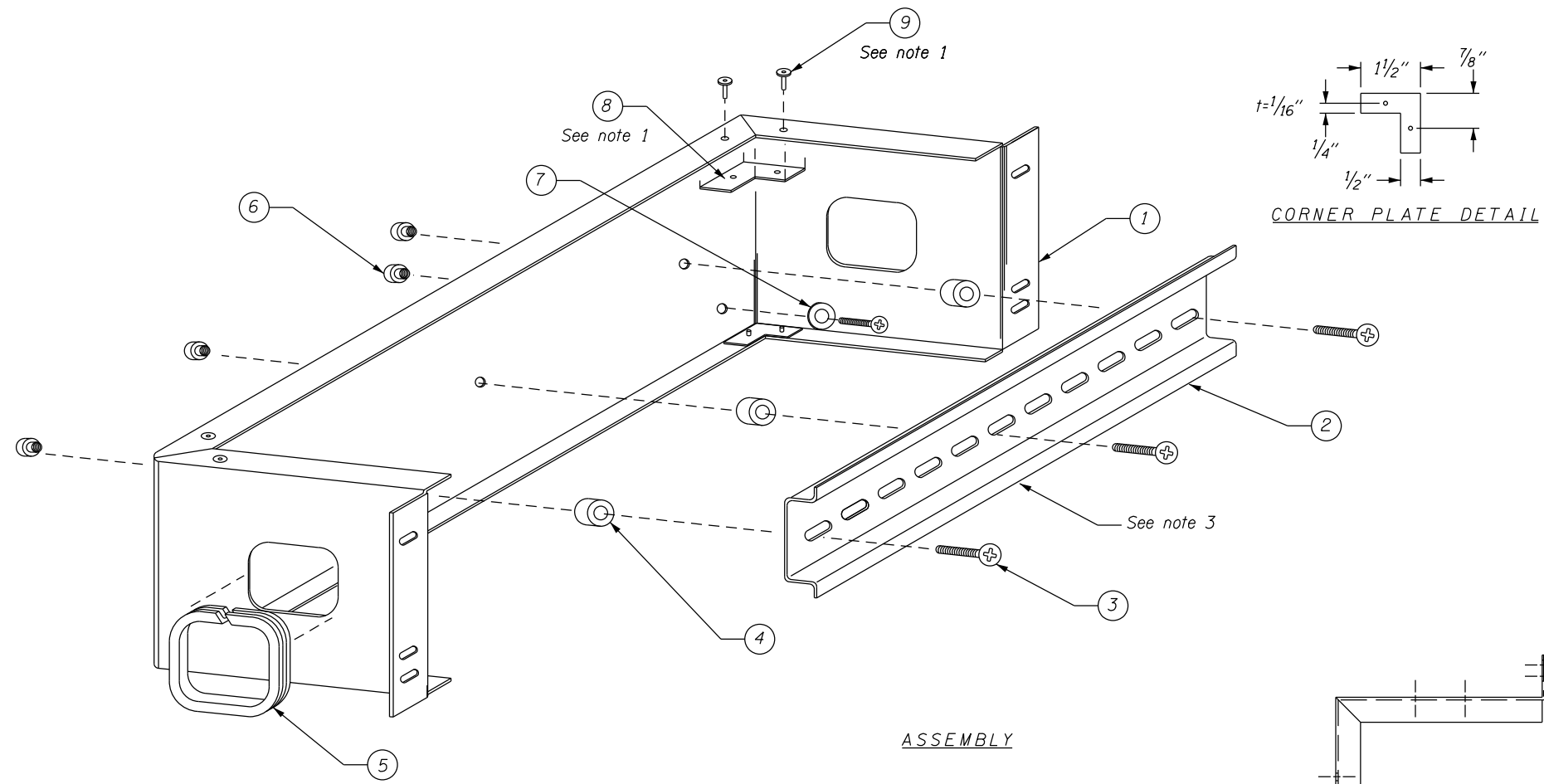
FRONT VIEW

OREGON DEPARTMENT OF TRANSPORTATION
TRAFFIC - ROADWAY SECTION

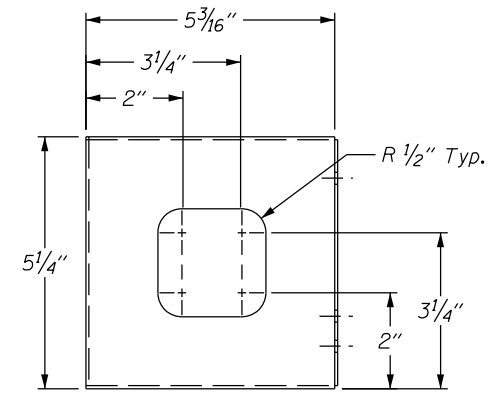
SIGNALS COMMUNICATION BRACKET
19" HINGED RACK MOUNTED ASSEMBLY
(FOR 336 CABINETS ONLY)

REVISION HISTORY: REVISION 1 (5/31/13)

REVISION DATE **5/31/13**



Item No.	Part	Material	Qty.
1	Rack frame	Alum. plate 5052 H-32, 1/16"	1
2	"35mm x 15mm" DIN Rail, pre-punched, 16" long	Electrolitically plated steel	1
3	10-32 x 3/4" Pan head machine screw	Type 304 Stainless	3
4	Spacer, 5/8" deep x 1/4" I.D. x 5/8" O.D.	Aluminum or HDPE	3
5	Polyethylene adhesive lined grommet edging	Polyethylene	2
6	10-32 Self clinching sheet metal nut	Type 304 Stainless	4
7	10-32 x 1/2" Green bonding screw w/ washer	Type 304 Stainless	1
8	Corner plate	Alum. plate 5052 H-32, 1/16"	4
9	3/32" dia. blind rivet, button head	Aluminum	8



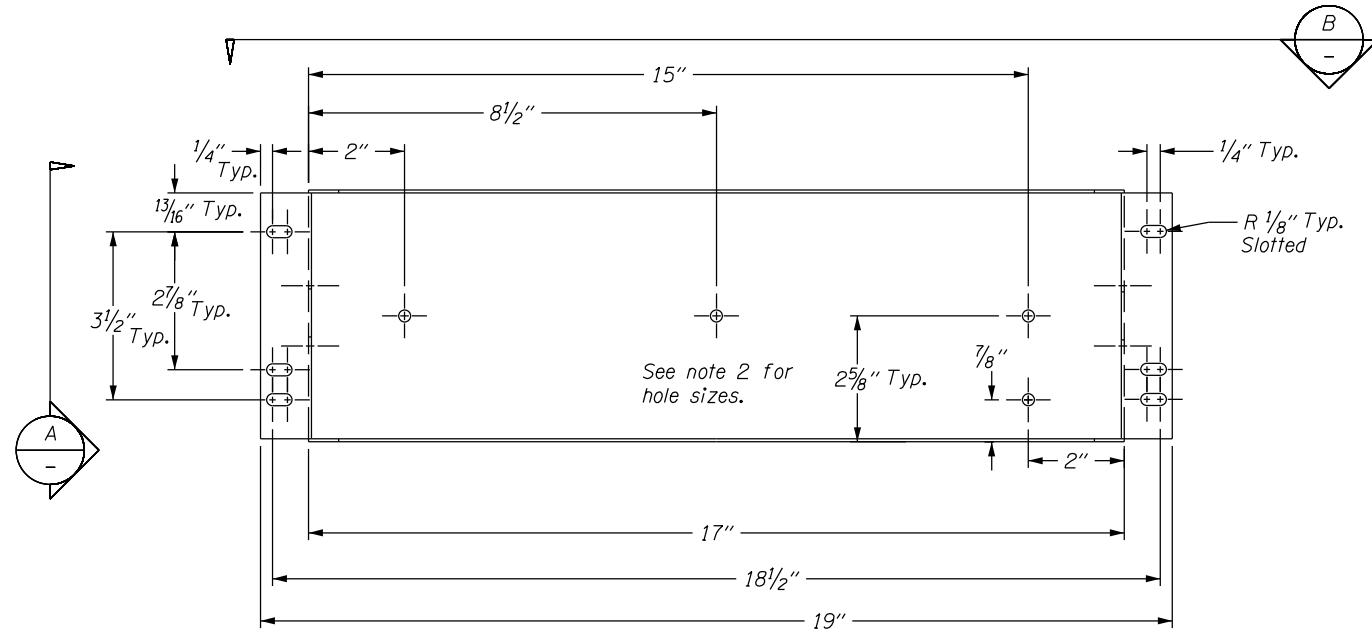
A SIDE VIEW

General notes:

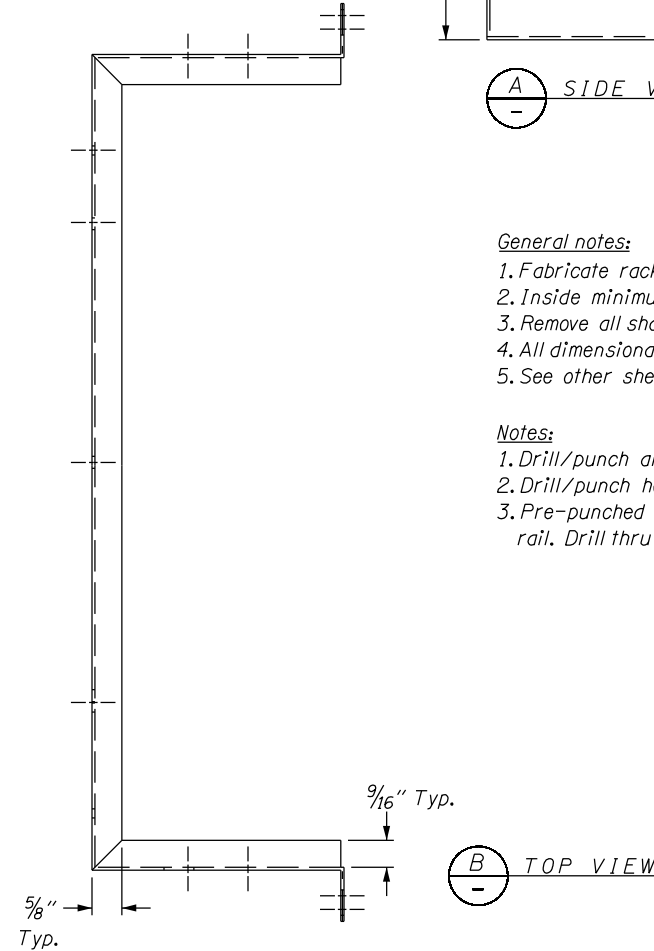
1. Fabricate rack frame using bends of single aluminum sheet.
2. Inside minimum bend radii are 1/32".
3. Remove all sharp corners.
4. All dimensional tolerances are +/- 1/32".
5. See other sheet for component assembly.

Notes:

1. Drill/punch and blind rivet corner plates on each inside corner.
2. Drill/punch holes as required to secure self clinching metal nuts.
3. Pre-punched DIN rail may be substituted with solid DIN rail. Drill thru holes as necessary for 10-32 screws.



B FRONT VIEW



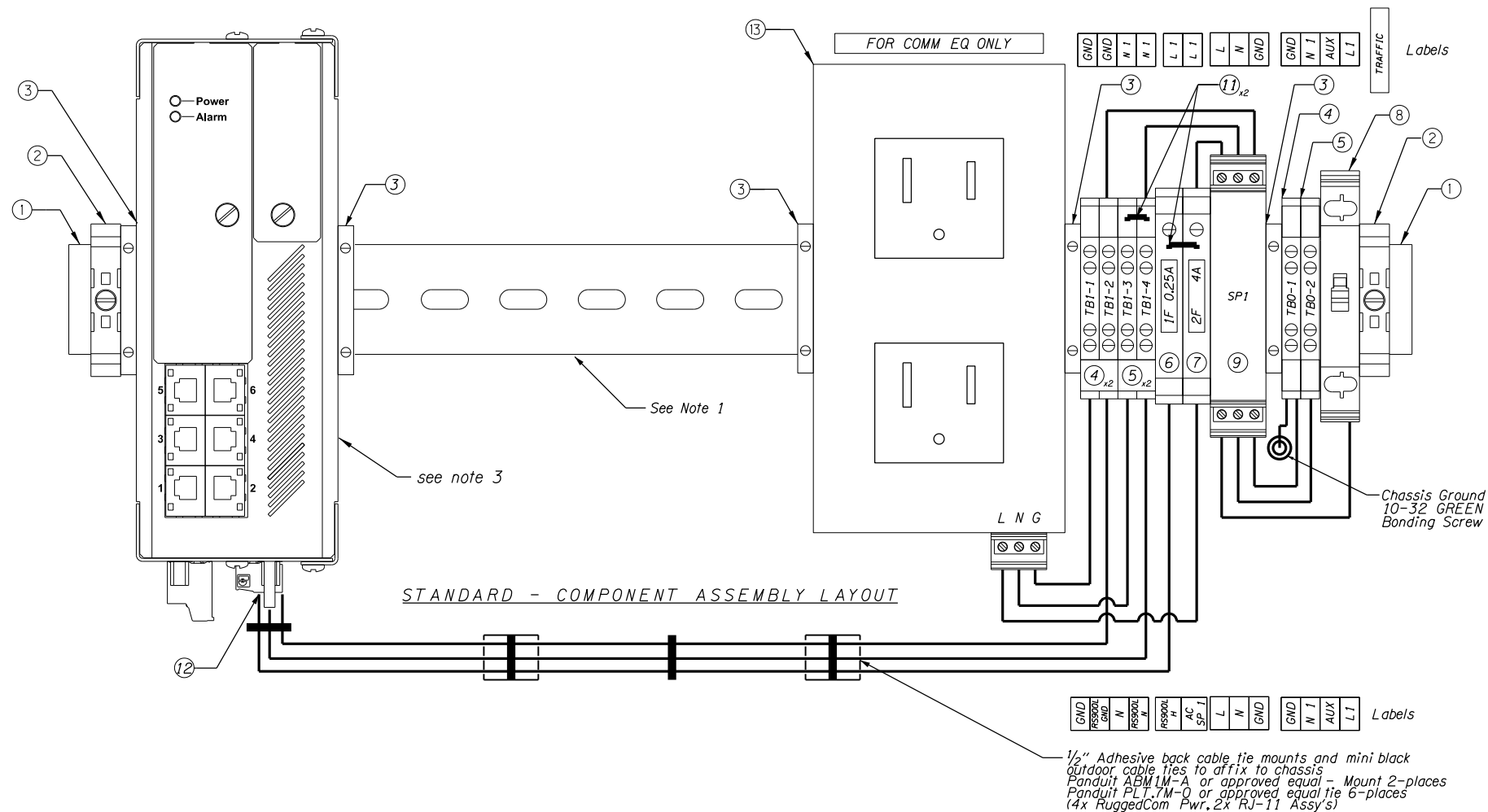
B TOP VIEW

OREGON DEPARTMENT OF TRANSPORTATION
TRAFFIC - ROADWAY SECTION

SIGNALS COMMUNICATION BRACKET
19" NON-HINGED RACK MOUNTED ASSEMBLY
(FOR 332 CABINETS)

REVISION HISTORY: REVISION 1 (5/31/13)

REVISION DATE **5/31/13**



Item	Description	Drawing #	Qty.
1	"35mm x 15mm" DIN Rail End Cap	-	2
2	"35mm x 15mm" DIN Rail End Clamp	-	2
3	"35mm x 15mm" DIN Rail Spacer	-	5
4	Ground Terminal Block, see specifications #3	TB0-1, TB1-1&2	3
5	Terminal Block, see specifications #3	TB0-2, TB1-3&4	3
6	Resettable Fuse Terminal Block - 0.25A Fuse, see specifications #3	1F	1
7	Resettable Fuse Terminal Block - 4A Fuse, see specifications #3	2F	1
8	10A Modular Circuit Breaker, see specifications #2	CB1	1
9	Power Surge Protection Device, see specifications #1	SP1	1
10	Labels	-	-
11	Terminal Jumpers	-	2
12	RuggedCom Power Connector, see note 3	-	1
13	NEMA 5-15R Duplex Receptacle, see specifications #6	-	1

SPECIFICATIONS

- Power Surge Protection Device - Each communication rack shall be protected from electrical transients using surge suppression. Each surge suppressor shall meet the following specifications:
 Listing: UL 1449 2nd Edition
 Mounting: "35mm x 15mm" DIN Rail
 Peak Surge Current: 10,000 Amperes or more
 Suppression Voltage: 330 Volts or less
 Nominal Voltage: 120 Volts AC
 Max Continuous Current: 10 Amperes or more
- Circuit Breaker 10A - Each communication rack shall be protected from overload conditions using a supplemental circuit breaker. Each circuit breaker shall meet the following specifications:
 Listing: UL 489 or UL 1077
 Mounting: "35mm x 15mm" DIN Rail
 Voltage Rating: 120 Volts AC or more
 Current Rating: 10 Amperes
- All terminal blocks shall be DIN rail mounted and meet the requirements of UL 1059. All terminal blocks shall have a voltage rating of 300 Volts or more, current rating of 15A or more, and shall be one piece or factory assembled, sectional, double terminal, barrier type, with binder screw terminals. Fused terminal blocks shall be provided for protecting equipment which are not internally fused. Fuses shall be resettable, quick acting and sized as shown.

 Ground terminal blocks shall be mechanically and electrically connected to the DIN rail, green in color and accept wire sizes ranging from #22 to #12 AWG.

- Wiring - All point-to-point wire shall be UL 1015, 600V PVC insulated, stranded, tinned copper. Black (hot) and white (neutral) wire shall be 16 awg, green/ yellow (ground) wire shall be 16 awg. All conductors attached to a terminal block shall be terminated with insulated wire ferrules. 1/2" adhesive back cable tie mounts and cable ties shall be used accordingly to secure conductors.
- Grounding and Bonding - Electrical grounds shall be bonded to the 10-32 x 1/2" green bonding screw. All grounding and bonding shall be in accordance with UL 467.
- NEMA 5-15R Duplex Receptacle shall meet the following specifications:
 Listing: UL 498
 Mounting: "35mm x 15mm" DIN Rail
 Nominal Voltage: 120 Volts AC
 Current Rating: 15 Amperes

NOTES

- Assemble components on DIN rail as shown. Use additional DIN rail spacers, end clamps and end plates where necessary.
- Network switch is state furnished and installed.
- Pre-wire assembly in accordance with wire diagram shown. RuggedCom Power Connector shall be Phoenix Contact Combincon plug P/N: "MVSTBW-2.5/5(3)-STF-5.08" or approved equal.

OREGON DEPARTMENT OF TRANSPORTATION
 TRAFFIC - ROADWAY SECTION

SIGNALS COMMUNICATION BRACKET
STANDARD DIN RAIL ASSEMBLY
 (FOR WIRELESS & FIBER COMMUNICATIONS)

REVISION HISTORY: REVISION 1 (5/31/13)

REVISION DATE **5/31/13**

Appendix C



Oregon Department of Transportation
Standard Specification
for
**Microcomputer Signal
Controller**

September 4, 2001

Includes specifications for 170E/HC-11 Controller and ITS Cabinets



OREGON DEPARTMENT of TRANSPORTATION
HIGHWAY DIVISION
TRAFFIC MANAGEMENT SECTION
<http://www.odot.state.or.us/tstrafmgtpublic/>



TE 01-3
Standard Specification for Microcomputer Signal Controller
©2001 Oregon Department Of Transportation
Highway Division
Traffic Management Section
<http://www.odot.state.or.us/tstrafmgtpublic/>
Standard Spec 170ATC-4.doc

Oregon Department of Transportation
Transportation Operations Division
Technical Services
Traffic Management Section

Standard Specification for Microcomputer Signal Controller

This document also includes specifications for peripheral equipment.

Approved by:

Original Signed and on File
David W. Greenberg, P.E., Traffic Design Engineer

9/11/01
Date

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SPECIFICATION PRIORITIES In case of conflict, the individual chapter shall govern over Appendix B and Appendix B shall govern over Chapter 1, General Requirements.

ITEMS SUPPLIED Items supplied shall be new and unused.

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CHAPTER 1

GENERAL SPECIFICATIONS FOR TRAFFIC SIGNAL CONTROL EQUIPMENT

This chapter contains general requirements applicable to all equipment specified in this document.

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SECTION 1 – GLOSSARY

1.1 **Wherever the following terms or abbreviations are used, the intent and meaning shall be interpreted as follows:**

A – Ampere

AC – Alternating Current

AC+ - 120 volts AC, 60 hertz ungrounded power source

AC- - 120 volts AC, 60 hertz grounded return to the power source

ACIA – Asynchronous Communications Interface Adapter device, Motorola MC6850
(or equal)

amp(s) – Ampere(s)

ANSI – American National Standard Institute

ASCII – American Standard Code for Information Interchange

Assembly – A complete machine, structure, or unit of a machine that was
manufactured by fitting together parts and/or modules

ASTM – American Society for Testing and Materials

ATC – Advanced Transportation Controller

AWG – American Wire Gage

AWS – American Welding Society

C – Celsius

C Language – The ANSI C Programming Language

Cabinet – An outdoor enclosure for housing the controller unit and associated
equipment

Certificate of Compliance – A certificate signed by the manufacturer of the material
or the manufacturer of assembled materials stating that the materials involved
comply in all respects with the requirements of the specifications

Channel – An information path from a discrete input to a discrete output

CMOS – Complementary Metal Oxide Semiconductor

Component – A component shall be defined as any electrical or electronic device

Contractor – The person or persons, manufacturer, firm, partnership, corporation, vendor, or combination thereof, who have entered into a contract with the STATE, as party or parties of the second part or their legal representative

Controller Unit – That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly

CPU – Central Processing Unit

CR – ACIA Control Register

CRC – Cyclic Redundancy Check

Daughterboard - A printed circuit auxiliary interface board

DC – Direct Current

DIN – Deutsche Industrie Norm

DMA – Direct Memory Access

DRAM – Dynamic Random Access Memory

DTA – Down Time Accumulator

dB – Decibel

dBa – Decibels above reference noise, adjusted

EG – Equipment Ground

EIA – Electronic Industries Association

EMI – Electro Magnetic Interference

Engineer – The Director of the Department of Transportation, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them

EPROM – Ultraviolet Erasable Programmable Read Only Memory

EEPROM – Electrically Erasable Programmable Read Only Memory

Equal – Interpretation shall be in the judgement of the Engineer:

Connectors: Having identical physical dimensions, contact/pin material, plating, and method of connection.

Devices: conforming to function, pin out, electrical and operating parameter requirements, access times, and interface parameters of the specified device.

ETL – Electrical Testing Laboratories, Inc.

Firmware – A computer program or software stored permanently in PROM, EPROM or ROM, or semi-permanently in EEPROM

FLASH – A +5 VDC powered IC memory device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features

FPA – Front Panel Assembly

HEX – Hexadecimal

Hz – Hertz

IC – Integrated Circuit

I.D. – Identification

IEEE – Institute of Electrical and Electronics Engineers

IMP – Integrated Multi-protocol Processor

IRQ – Interrupt Request

ISO – International Standards Organization

Jumper – A means of connecting/disconnecting two or more conductive points by soldering or de-soldering a conductive wire or by PCB post connection or disconnection.

KB – Kilobytes

KBps - Kilobytes per second

kHz – kilohertz

Laboratory – The established laboratory of the Department of Transportation or other laboratories authorized by the Department to test materials involved in the contract

LED – Light Emitting Diode

LOGIC – Negative Logic Convention (Ground True) State

LSB – Least Significant Byte

lsb – Least Significant Bit

lx – Lux

m – Meter

mA – Milliampere

MB – Megabyte

MCU – Micro Controller Unit

MIL – Military Specification(s)

Modem – Modulate/Demodulate Unit

Module – A functional unit that plugs into an assembly

Motherboard – A printed circuit connector interface board

MOS- Metal Oxide Semiconductor

MOV – Metal Oxide Varistor

MPU – Microprocessor Unit

ms – Millisecond(s)

MS – Military Standards

MSB – Most Significant Byte

msb – Most Significant Bit

mV – Millivolt(s)

mW – Milliwatt(s)

M/170 – Program Module/Model 170E Controller Unit Connector

M/170E – Model 170E Auxiliary Board Connector

N – Newton (SI unit of force)

NA – Presently not assigned - cannot be used by the contractor for other purposes

NEMA – National Electrical Manufacturer’s Association

NETA – National Electrical Testing Association, Inc.

N.C. – Normally closed contact

NLSB – Next Least Significant Byte

nlsb – Next Least Significant Bit

NMSB – Next Most Significant Byte

nmsb – Next Most Significant Bit

N.O. – Normally open contact

ns – Nanosecond

PCB – Printed Circuit Board

PDA – Power Distribution Assembly

pF – Picofarad

PLA/PAL – Programmable Array Logic Device

ppm – Parts per million

PWM – Pulse Width Modulation

RAM – Random Access Memory

RBF – Random Block File

RDR – ACIA Receiver Data Register

RF – Radio Frequency

RMS – Root-Mean-Square

ROM – Read Only Memory

RTC – Model 170E Controller Unit Real Time Clock

RTCA – Real Time Clock Adjuster Circuitry

RTS – Request to Send

R/W – Read/Write Control Line

S – Logic State

s – Second

SCC – Serial Communication Controller

SCI – Serial Communications Interface

SDLC – Synchronous Data Link Control

Second Sourced – Produced by more than one manufacturer

SI – International System of Units

SMC – Serial Management Controller

SP – Serial Port (Switchpack when used in Tables B-2 and B-3)

SR – ACIA Status Register

SRAM – Static Random Access Memory

STATE – State of Oregon

SW – Switch

TBK – Terminal Block

TDR – ACIA Transmit Data Register

TOD – Time-of-Day Clock

Triac – Silicon-controller rectifier which controls power bilaterally in an AC switching circuit

Thumb Screw Device (TSD) – A retractable screw fastener with projecting stainless steel screw, spring, and natural aluminum knob finish

TTL – Transistor-Transistor Logic

UL – Underwriter’s Laboratories, Inc.

VAC – Voltage Alternating Current

VDC – Voltage Direct Current

VMA – Valid Memory Address

VME – Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2

Watchdog Timer (WDT) – A monitoring circuit, external to the device watched, which senses an Output Line from the device and reacts

x – Number Value

XX – Manufacturer's Option

μ A – Microampere

μ F – Microfarad

μ H – Microhenry

μ S – Microsecond

SECTION 2 – GENERAL REQUIREMENTS

- 1.2.1 **In case of conflict**, the individual chapter shall govern over Appendix C and Appendix C shall govern over all subsequent paragraphs in Chapter 1, General Requirements. All equipment furnished under these specifications shall be of the solid state design. Use of vacuum or gaseous tubes or electromechanical devices within the equipment is not acceptable unless otherwise indicated.
- 1.2.2 **Documentation**
- 1.2.2.1 Each controller cabinet assembly shall include two copies of the latest manual for each item of equipment that is furnished with the cabinet. The STATE, at our option, may reduce the number of manuals required on a project.
- 1.2.2.2 Manuals shall be printed in font of Helvetica Bold 12 (or equal) on 216 mm by 280 mm paper. Schematics, layouts, parts lists, and plan details shall have a minimum font of Gothic Legal 18 (or larger) and may be on 280 mm by 432 mm sheets, but the sheets must be neatly folded to 216 mm by 280 mm size. The manual shall be bound in durable covers.
- 1.2.2.3 Each manual shall include the following
- Table of Contents
 - Glossary
 - General Description
 - General Characteristics
 - Installation
 - Adjustments
 - Theory of Operation
 - Systems Description (include block diagram)
 - Detailed Description of Circuit Operation
 - Maintenance
 - Preventive Maintenance
 - Trouble Analysis
 - Troubleshooting Sequence Chart
 - Wave Forms
 - Voltage Measurements
 - Alignment Procedures
 - Parts List (to include circuit and board designation, part type and class, power rating and component manufacturer, original manufacturer's part number and data specification sheets for special design components.)
 - Electrical Interconnection Drawing
 - Schematic and Logic Diagram
 - Assembly drawings and a pictorial diagram showing physical locations and identification of each component.

- 1.2.2.3.1 The date of revision, serial numbers and revision numbers of equipment covered by manuals shall be printed on the front cover of the manuals.
- 1.2.2.3.2 A Mean-Time-Between-Failure Analysis Report for Model 2070 Controller Units shall be provided with the Qualified Products List Submittal. It shall encompass the 2070 Unit (complete) and its individual modules and assemblies. The report shall describe in detail the methodology used.
- 1.2.2.4 Manuals for the Controller Unit and Models 332, 334, 336, 336S and ITS Cabinets shall be furnished with the item and enclosed in the shipping container.
- 1.2.2.5 Prior to final printing, a preliminary draft of all manuals shall be submitted to the Engineer for approval.
- 1.2.3 **Interchangeability** – The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

ASSEMBLIES

ASSOCIATED DEVICES

Output File #1 and #2

Model 200 Switch Pack
Model 210 Monitor Unit
Model 430 Heavy Duty Relay

Auxiliary Output File

Model 200 Switch Pack
Model 430 Heavy Duty Relay

Input File

Models 222, 222T, 224 & 232E Detectors
Models 242 & 252 Isolators

Power Distribution Assembly #2

Model 204 Flasher Unit
Model 206 Power Supply Module

Output/Power Distribution Assembly #3

Model 200 Switch Pack
Model 206 Power Supply Module
Model 208 Watchdog Monitor
Model 430 Heavy Duty Relay

Power Distribution Assembly #4 & #5

Refer to Cabinet Models 340 & 344

Power Distribution Assembly #6
(FUTURE)

Model 206 Power Supply Module

Model 170E Controller Unit

Model 400 Modem
Model 412 Program Module

Table continued on next page

Continued from previous page

ASSEMBLIES

ASSOCIATED DEVICES

Model 2070 Controller Unit

Model 2070-1 CPU Module
Model 2070-2A and 2B Field I/O Module
Model 2070-3 Front Panel Assembly
Model 2070-4 Power Supply
Model 2070-5 VME Cage Assembly
Model 2070-6 Serial Comm Module
Model 2070-7A and 7B Serial Comm Module

Model 170ATC Controller Unit

Model 170ATC-1 Engine Board Module -
MC68360 microcomputer, memory
devices and communication ports
Model 170ATC-2 Interface Module (Field I/O)
Model 170ATC-3 Front Panel Assembly
Model 170ATC-4 Power Supply
Model 400 Modem

Cabinet Models 332, 336, & 336S

Model 170E Controller Unit
Model 170ATC Controller Unit
Input File
Power Distribution Assembly #2
Output File #1
Auxiliary Output File

Cabinet Model 334

Model 170E Controller Unit
Model 170ATC Controller Unit
Input File
Output/Power Distribution Assembly #3
Auxiliary Output File

Cabinet Model 340

Power Distribution Assembly #4

Cabinet Model 344

Power Distribution Assembly #5

Cabinet Model ITS (FUTURE)

Model 170E Controller Unit
Model 170ATC Controller Unit
Model 2070 Controller Unit
Model 2070-x peripherals
Input File
PDA #2, #3 and #6
Output File #1 & #2

1.2.4 Indicators and Character Displays

1.2.4.1 All indicators and character displays shall have a minimum of $\pm 45^\circ$ cone of visibility with the axis perpendicular to the front panel. All indicators and character displays shall be readily visible at a radius of up to 1.2 m within the cone of visibility when the indicator is subjected to 97,000 lx of white light with the light source at $45^\circ (\pm 2^\circ)$ to the front panel. If characters are not self-luminous, illumination shall be provided for viewing at low levels of ambient light. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15° minimum shall be provided for Models 208, 210, 212, 222, 222T, 242, 232, and 252, as well as a clearance of 30° minimum for Models 200, 204, and 206.

1.2.4.2 All indicators and character displays shall have a rated life of 100,000 hours, minimum.

1.2.4.3 Liquid Crystal Displays (LCD's) shall operate at temperatures of -34°C to 73°C without bleeding or loss of visibility. LCD's shall be back-lighted.

1.2.5 **Connectors** - Unless otherwise noted, connector specifications apply to both the plug (with suffix "P") and the receptacle or socket (with suffix "S").

1.2.5.1 General Requirements:

1.2.5.1.1 All connectors shall be keyed to prevent improper insertion of the wrong connector or PCB.

1.2.5.1.2 The Type 25 connector shall be a 25 contact AMP HDP-20 connector (or equal) with gold on nickel-plated contacts. The female mating connector with socket contacts is designated Type 25S and the male mating connector with pin contacts is designated Type 25P. The Type 25P connector shall be provided with lock spring clips for latching to its mating connector.

1.2.5.1.3 The Type T connector shall be a single row, 10 position, feed through TBK. The TBK shall be a barrier type with 6 mm (or longer), nickel-plated, brass binder head screws. Each terminal shall be permanently identified as to its function.

1.2.5.1.4 The mating connectors shall be designated as to the connector number and male/female relationship such as C1P (pin contact) and C1S (socket contact).

1.2.5.2 Connectors C1, C2, C20, C30, C40, C4, C5, and C6

- 1.2.5.2.1 Pin and socket contacts for connectors C1, C2, C20, C30, C40, C4, C5, and C6 shall be beryllium copper construction, subplated with 0.0013 mm nickel and plated with 0.0008 mm gold. Pin diameter shall be 1.6 mm. Connectors shall have the following number of contacts:
- C1 – 104 contacts
 - C2, C20, C30, C40 – 14 contacts
 - C4 – 37 contacts
 - C5 & C6 – 24 contacts
- 1.2.5.2.2 All pin and socket contacts for connectors C1, C2, C20, C30, C40, C4, C5, and C6 shall use the AMP #601105-1 or #91002-1 contact insertion tool, and the AMP #305183 contact extraction tool.
- 1.2.5.2.3 The C1, C2, C20, C30, and C40 connector blocks shall be constructed of phenolic resin (or equal) and shall have an insulation resistance of 5,000 megohms. The contacts shall be secured in the blocks with stainless steel springs.
- 1.2.5.2.4 Connectors C1, C2, C20, C30, and C40 shall have stainless steel corner guides. The guide pins shall be 27.86 mm in length and the guide sockets 15.88 mm in length.
- 1.2.5.2.5 Connectors C4, C5, and C6 shall be circular plastic type with quick connect/disconnect capability and thread assist, positive detent coupling. The connectors shall be UL listed glass-filled Nylon, 94 V-1 rated, heat stabilized, and fire resistant.
- 1.2.5.3 PCB Connectors:
- 1.2.5.3.1 PCB edge connectors shall have bifurcated, gold-plated contacts.
- 1.2.5.3.2 The PCB receptacle connector shall meet or exceed the following:
- | | |
|------------------------|---|
| Operating Voltage: | 600 VAC (RMS) at sea level |
| Current Rating: | 5 amps |
| Insulation Material | Diallyl Phthalate or Thermoplastic |
| Insulation Resistance: | 5,000 megohms |
| Contact Material: | Copper alloy plated with:
0.00127 mm of nickel &
0.00038 mm of gold |
| Contact Resistance: | 0.006 ohm, maximum |
- 1.2.5.3.3 The two-piece PCB connector shall meet or exceed the DIN 41612.
- 1.2.5.3.4 The PCB 22/44 connector shall have 22 independent contacts per side, dual-sided with 3.96 mm contact centers.

- 1.2.5.3.5 The PCB 28/56 connector shall have 28 independent contacts per side, dual-sided with 3.96 mm contact centers.
- 1.2.5.3.6 The PCB 36/72 connector shall have 36 independent contacts per side, dual-sided with 2.5 mm contact centers.
- 1.2.5.3.7 The PCB 43/86 Connector shall have 43 independent contacts per side; dual sided with 2.5 mm contact centers.
- 1.2.5.4 Wire Terminal Connectors: Each wire terminal shall be solderless with PVC insulation and a heavy-duty short-locking spade type connector. All wire terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.
- 1.2.5.5 Flat Cable Connectors
 - 1.2.5.5.1 Each flat cable connector shall be designed for use with 26 AWG cable.
 - 1.2.5.5.2 Each flat cable connector shall have dual cantilevered phosphor bronze contacts plated with 500 nm gold over 1270 nm of nickel.
 - 1.2.5.5.3 Each flat cable connector shall have a current rating of 1 ampere minimum and an insulation resistance of 5 megohms minimum.
- 1.2.5.6 PCB Header Post Connectors
 - 1.2.5.6.1 Each PCB header post shall be 1.0 mm square by 8.7 mm high.
 - 1.2.5.6.2 PCB header posts shall be mounted on 4.0 mm centers.
 - 1.2.5.6.3 PCB header posts shall be tempered hard brass plated with 380 nm of gold over 1.270 mm nickel.
- 1.2.5.7 PCB Header Socket Connectors: Each PCB header socket block shall be nylon or diallyl phthalate.
 - 1.2.5.7.1 PCB header sockets shall be removable, but crimp connected to its conductor.
 - 1.2.5.7.2 PCB header socket contacts shall be brass or phosphor bronze plated with 560 nm of gold over 1270 nm of nickel.
 - 1.2.5.7.3 The supplier shall list the part number of the extraction tool recommended by its manufacturer.
- 1.2.6 **Packaging:** Each item delivered shall be individually packed in its own shipping container. When loose Styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the Styrofoam.

- 1.2.7 **Delivery:** Each item delivered for testing shall be complete, including manuals, and ready for testing.
- 1.2.8 **Metals**
- 1.2.8.1 Aluminum:
- 1.2.8.1.1 Sheet shall be Type 5052-H32 ASTM Designation B209.
- 1.2.8.1.2 Rod, Bar, and Extruded shall be Type 6061-T6 (or equal).
- 1.2.8.2 Stainless Steel:
- 1.2.8.2.1 Sheet shall be annealed or one-quarter-hard, complying with the ASTM Destination: A666 for Type 304, Grades A or B, stainless steel sheet.
- 1.2.8.3 Cold Rolled Steel:
- 1.2.8.3.1 Sheet, Rod, Bar, and Extruded shall be Type 1018/1020.
- 1.2.8.3.2 Plating – All cold rolled steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2, Class 1, or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.
- 1.2.8.4 All sharp edges and corners shall be rounded.
- 1.2.8.5 All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

SECTION 3 – COMPONENT REQUIREMENTS

- 1.3.1 **All components shall be second sourced** and shall be of such design, fabrication, nomenclature, or other identification as to be purchased from a wholesale electronics distributor or from the component manufacturer, except as follows:
 - 1.3.1.1 When a component is of such special design that it precludes the purchase of identical components from any wholesale electronics distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used per contract job. The STATE, at our own option, may reduce the number required.
 - 1.3.1.2 Circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.
 - 1.3.1.3 Within the circuit of any device, module, or PCB, electrical isolation shall be provided between DC logic ground, equipment ground and the AC grounded conductor. They shall be electrically isolated from each other by 500 megohms, minimum, when tested at the input terminals with 500 VDC.
- 1.3.2 **Memory, MPU, and ACIA devices** shall be socket mounted onto the PCBs. No other device shall be socket mounted unless specifically called out.
- 1.3.3 **No component** shall be operated above 80% of its maximum rated voltage, current, or power ratings. Digital components shall not be operated above 3% of their nominal voltage, current, or power ratings.
- 1.3.4 **No component** shall be provided with a manufactured date that is two years older than the contract award date. The design life of all components operating for 24 hours a day in their circuit application shall be 10 years or longer.
- 1.3.5 **All discrete components**, such as resistors, capacitors, diodes, transistors, and integrated circuits shall be individually replaceable. Components shall be arranged so they are easily accessible for testing and maintenance.
 - 1.3.5.1 Encapsulation of two or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators, and transistor arrays.
- 1.3.6 **The Contractor** shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

1.3.7 **Capacitors**

- 1.3.7.1 The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst case design parameters of the circuitry by 150%.
- 1.3.7.2 A capacitor that may be damaged by shock or vibration shall be supported mechanically by a clamp or fastener.
- 1.3.7.3 Capacitor encasements shall be resistant to cracking, peeling, and discoloration.
- 1.3.7.4 All capacitors shall be insulated and shall be marked with their capacitance value and working voltage.
- 1.3.7.5 Electrolytic capacitors shall not be used for capacitance values of less than 1.0 μF and shall be marked with polarity.

1.3.8 **Potentiometers**

- 1.3.8.1 Potentiometers with ratings from 1 to 2 watts shall be equivalent to Military Type RV4.
- 1.3.8.2 No potentiometers with less than a 1-watt rating shall be used (except for trimmer type function).
- 1.3.8.3 The power rating of any potentiometer shall be at least 100% greater than the maximum power requirements of the circuit.

1.3.9 **Resistors**

- 1.3.9.1 Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications: MIL-R-11F or MIL-R-22684.
 - 1.3.9.1.1 All resistors shall be insulated and shall be marked with their resistance value. The EIA color codes, or stamped value (power resistor) shall indicate resistance values.
- 1.3.9.2 Resistors shall be 10% or less tolerance.
- 1.3.9.3 The value of the resistors shall not vary by more than 5% between -37°C and 74°C .
- 1.3.9.4 Resistors that have a rating exceeding 2 watts shall not be used unless special ventilation or heat sinking is provided. They shall be insulated from the PCB.

1.3.10 **Semiconductor Devices**

- 1.3.10.1 All solid-state devices, except LEDs, shall be of the silicon type.
- 1.3.10.2 All transistors, integrated circuits, and diodes shall be a standard type listed by EIA and clearly identifiable.
- 1.3.10.3 All MOS and CMOS components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.
- 1.3.10.4 The device Pin 1 location shall be marked on the PCB adjacent to the pin.

1.3.11 **Transformers and Inductors**

- 1.3.11.1 All power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly stamped on the case or laminations.
 - 1.3.11.2 All transformers and inductors shall have their windings insulated and shall be protected to exclude moisture.
 - 1.3.11.3 All transformers and inductor leads shall be color coded with an approved EIA color code or identified in a manner to facilitate proper installation.
- 1.3.12 Triacs: Each triac with a designed circuit load of greater than 0.5 A at 120 VAC shall be mounted to a heat sink with a machine screw and nut with integral lockwasher.

1.3.13 **Circuit Breakers [10 amps (or greater)]**

- 1.3.13.1 Circuit breakers shall be listed by UL or ETL. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the ampere rating shall be visible from the front of the breaker. All circuit breakers [30 amps (or greater)] shall be quick-break on either automatic or manual operation. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. An ambient air temperature range of from -18°C to 50°C shall not influence overload tripping. Minimum interrupting capacity shall be 5,000 amps, RMS.
- 1.3.13.2 Circuit breakers shall be the trip-free type.
- 1.3.13.3 Multi-pole breakers shall be the common-trip type.

1.3.14 **Switches**

- 1.3.14.1 Dual-Inline-Package (DIP) Quick Snap Switches: DIP switches shall be rated for a minimum of 30,000 operations per position at 50 mA, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 mA, 30 VDC. The contacts shall be gold over brass or silver. 120 VAC or 28 VDC DIP switches shall be silver over brass (or equal).

- 1.3.14.2 Logic Switches: The switch contacts shall be rated for a minimum of one ampere resistive load at 120 VAC or 28 VDC and shall be silver over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.
- 1.3.14.3 Control Switches: The switch contacts shall be rated for a minimum of 5 amp resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.
- 1.3.14.4 Power Switches: Ratings shall be the same as for Control switches, except the contact rating shall be a minimum of 10 amps at 125 VAC.

SECTION 4 – MECHANICAL REQUIREMENTS

1.4.1 Assemblies and PCB Design

1.4.1.1 Assemblies (including Controller Unit): All assemblies shall be easily replaceable and incorporate plug-in capability for their associated devices or PCBs with the following exceptions:

- Motherboard and daughterboard assemblies
- The controller power supply may be a plug-in assembly.

1.4.1.2 Assemblies shall be provided with two guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 20 mm from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.4.1.3 PCBs: No component, traces, brackets, or obstructions shall be within 3 mm of the board edge (guide edges).

1.4.1.4 The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all items.

1.4.2 **Workmanship:** Workmanship shall be in accordance with the highest industry standards.

1.4.3 Model Numbers

1.4.3.1 In addition to any assignment of model numbers by the manufacturer, a model number assigned in the table below shall be displayed on the front panel in bold type, at least 6 mm high. Other model numbers may be approved at the discretion of the Engineer.

<u>MODEL #</u>	<u>TITLE</u>	<u>MODEL #</u>	<u>TITLE</u>
170E	CONTROLLER UNIT	224	Future
170E/HC-11	CONTROLLER UNIT	232e	Future
200	SWITCH PACK	242	DC ISOLATOR
204	FLASHER UNIT	252	AC ISOLATOR
206	POWER SUPPLY MODULE	400	MODEM
208	WATCHDOG MONITOR UNIT	412	PROGRAM MODULE
210	CONFLICT MONITOR UNIT	430	HEAVY DUTY RELAY
222	LOOP SENSOR UNIT	170ATC	CONTROLLER UNIT
222T	LOOP SENSOR UNIT (Time delay)		

- 1.4.4 **All PCB connectors** mounted on a motherboard or daughterboard shall be mechanically secured to the chassis or frame of the unit.
- 1.4.5 **All screw type fasteners** shall utilize locking devices or locking compounds except for finger screws, which shall be captive.
- 1.4.6 **Tolerances:** The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	± 1.3 mm
PCB	0, -0.25 mm
Edge Guides	± 0.38 mm

SECTION 5 – ENGINEERING REQUIREMENTS

1.5.1 Human Engineering

- 1.5.1.1 To the highest practicable degree, the unit shall be engineered for simplicity and ease of operation and maintenance. This shall include the following:
 - 1.5.1.1.1 No more than two potentiometers, controls, or switches may be mounted concentrically. Knobs for such devices shall have diameters in a ratio of 2:1 outer to inner. The outer knob shall have a diameter of at least 25 mm.
 - 1.5.1.1.2 Knobs shall be of large enough diameter (at least 12 mm diameter) and of great enough separation (at least 12 mm edge to edge) to assure ease of adjustment without disturbance of adjacent knobs.
 - 1.5.1.1.3 All fuses shall be easily accessible and shall be replaceable without the use of any tools.
 - 1.5.1.1.4 PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors.
 - 1.5.1.1.4.1 PCBs shall require a force of no less than 2.25 kg nor greater than 22.5 kg for insertion or removal.

1.5.2 Design Engineering

- 1.5.2.1 The following practices shall be employed in the design of solid state equipment circuitry:
 - 1.5.2.1.1 The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range.
 - 1.5.2.1.2 For reasons of personal safety, personnel shall be protected from all dangerous voltages.

- 1.5.3 **Generated Noise:** No item, component, or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of 1 m away from its surface.

SECTION 6 – PRINTED CIRCUIT BOARD REQUIREMENTS

- 1.6.1 **Design, Fabrication, and Mounting**
- 1.6.1.1 All contacts on PCBs shall be plated with a minimum thickness of 0.00076 mm gold over a minimum thickness of 0.0019 mm nickel.
- 1.6.1.2 PCB design shall be such that components may be removed and replaced without damage to boards, conductive traces, or tracks.
- 1.6.1.3 Fabrication of PCBs shall be in compliance with Military Specification: MIL-P-13949, except as follows:
 - 1.6.1.3.1 Only NEMA FR-4 glass cloth base epoxy resin, copper-clad laminates 1.59 mm minimum thickness shall be used. Inter-component wiring shall be by laminated copper-clad track having a minimum weight of 570 g/m², with adequate cross section for current to be carried. All copper tracks shall be plated or soldered to provide complete coverage of all exposed copper track. Jumper wires will not be permitted, except from plated-through padded holes to an external component or for designed function selection with the jumper insulated and as short as possible.
 - 1.6.1.3.2 In Section 3.3 of Military Specification: MIL-P-13949G, Grade of Pits and Dents shall be of Grade B quality (3.5.1.3) or better.
 - 1.6.1.3.3. In Section 3.3 of Military Specification: MIL-P-13949G, class of permissible bow or twist shall be Class C (Table V) or better.”
 - 1.6.1.3.4. Sections 4.2 through 6.6 of Military Specification: MIL-P-13949 (inclusive) shall be omitted except as referenced in previous sections of this specification.
- 1.6.1.4 The fabrication of PCBs and the mounting of parts and assemblies thereon shall conform to Military Specification: MIL-STD-275E, except as follows:
 - 1.6.1.4.1 All semiconductor devices required to dissipate more than 250 mw or any case temperature that is 10°C above ambient shall be mounted with spacers, transipads, or heat sinks to prevent direct contact with the PCB.
 - 1.6.1.4.2 When completed, all residual flux shall be removed from the PCB.
 - 1.6.1.4.3 The resistance between any two isolated, independent conductor paths shall be at least 100 megohms when a 500 VDC potential is applied.
 - 1.6.1.4.4 All PCBs shall be coated with a moisture resistant coating.

- 1.6.1.4.5 Where less than 6 mm lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.8 (± 0.4) mm thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.
- 1.6.1.5 Each PCB connector edge shall be chamfered at 30° from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 1.1 (± 0.1) mm for 2.5 mm spacing and 1.4 (± 0.1) mm for 4 mm spacing.
- 1.6.2 **Soldering**
 - 1.6.2.1 Hand soldering shall comply with Military Specification: MIL-STD-2000.
 - 1.6.2.2 Automatic flow soldering shall conform to the following conditions:
 - 1.6.2.2.1 Constant speed conveyor system
 - 1.6.2.2.2 Conveyor speed shall be the optimum to minimize solder peaks or points that form at component terminals.
 - 1.6.2.2.3 Temperature shall be controlled to within $\pm 8^{\circ}\text{C}$ of the optimum temperature.
 - 1.6.2.2.4 The soldering process shall result in the complete coverage of all copper runs, joints, and terminals with solder, except that which is covered by an electroplating process.
 - 1.6.2.2.5 Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.
 - 1.6.2.2.6 If exposure to the temperature bath is of such a time-temperature duration as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.
- 1.6.3 **Definitions:** Definitions for the purpose of this section on PCBs shall be taken from MIL-P-55110D Section 3.3 and any current addendum.

SECTION 7 – ELECTRICAL, ENVIRONMENTAL, AND TESTING REQUIREMENTS

Signal Controller Testing Procedure Performed by STATE

1.7.1 Submittals

1.7.1.1 The Contractor is required to submit a proposed material list within 30 days after award of contract.

1.7.1.2 All traffic signal control equipment is to be delivered to:

Oregon Department of Transportation
Traffic Signal Services Unit
2445 Liberty Street NE
Salem, Oregon 97303

1.7.1.3 The Contractor shall allow six (6) weeks for testing. All required equipment including wiring diagrams shall arrive in one shipment. Partial shipments will not be accepted and will be returned to the Contractor freight collect.

1.7.2 Categories

1.7.2.1 All traffic signal control equipment will be tested in three (3) categories: physical, environmental, and operational. STATE procedures for accomplishing these tests are contained in Appendix A of this specification.

1.7.2.2 If a failure occurs at any step in the test – physical, environmental, or operational – the Contractor will be permitted to make on-site repairs within five (5) days after notification of the malfunction. The test will then be restarted at the beginning of the category in which the malfunction occurred. Failure to make repairs within five (5) days after notification will result in rejection.

1.7.2.3 If equipment malfunctions twice in the same category, the equipment will be rejected. When equipment is rejected, items rejected will be returned, freight collect, to the Contractor or may be picked up by the Contractor within 10 days after notification. New equipment, having a different serial number, must then be submitted for testing. Rejected equipment shall not be used on signal projects within the State of Oregon.

1.7.3 Failures

1.7.3.1 A failure shall be defined as any occurrence where results are other than normal operation of the equipment. The test specimen is considered to have incurred a failure if any of the following examples of discrepancies occur:

1.7.3.1.1 If the controller unit skips intervals or phases, places false calls, displays false indicator lights, exhibits disruption of normal sequence, or produces changes in timing beyond specified tolerances

- 1.7.3.1.2 If the load switches produce incorrect signal indications
- 1.7.3.1.3 If the signal conflict monitor fails to satisfy the requirements of the contract specification

1.7.4 **Test Results**

- 1.7.4.1 A copy of the test results will be sent to the Contractor, Vendor, Project Manager, District Maintenance Supervisor, Regional Engineer, and Traffic Engineer, as applicable.

1.7.5 **Delivery to Project Site**

- 1.7.5.1 After the successful testing of controller equipment, the Contractor shall pick up and install all tested equipment, except that the STATE shall have the option of holding all or selected cabinet control equipment at the testing shop until such time as the controllers are required for turn-on. Successful completion of the test does not relieve the Contractor of equipment warranty obligations.

- 1.7.5.2 On projects where the STATE has held the controller at the testing shop, the STATE will deliver and install the controller, check the field wiring and, with the Regional Traffic Engineer, set timing. The Contractor, and/or Representative, shall be at the project site and is to assist the STATE in any way necessary to accomplish the turn-on.

1.7.6 **Physical Testing**

- 1.7.6.1 Inspection - A visual and physical inspection shall include mechanical, dimensional, and assembly conformance of all parts to these specifications.
- 1.7.6.2 Evaluation - The capabilities of the controller and auxiliary equipment shall be evaluated for conformance to these specifications.

1.7.7 **Environmental and Electrical Testing**

- 1.7.7.1 All components shall properly operate within the following limits unless otherwise noted:

- Applied Line Voltage: 95 to 130 VAC*
- Frequency: 60 (+/-3.0) Hertz
- Humidity: 5 to 95 percent
- Ambient Temperature: -34°C to +73°C
- Shock: Test per Specification MIL-STD-810E Method 516.4
- Vibration: Test per Specification MIL-STD-810E Method 514.4, equipment class G

*Refer to Power Failure and Power Restoration requirements of individual equipment.

- 1.7.7.2 All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 ± 0.5 volts/second.
- 1.7.7.3 All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in a STATE accepted cabinet connected to the commercial power lines.
- 1.7.7.4 The power line surge protection shall enable the equipment being tested to withstand and operate normally following the discharge of a 25-microfarad capacitor:
 - 1.7.7.4.1 The capacitor shall be charged to $\pm 2,000$ volts and applied directly across the incoming AC line.
 - 1.7.7.4.2 The capacitor shall discharge at a rate of once every 10 seconds for a maximum of 50 occurrences per test.
 - 1.7.7.4.3 The unit under test will be operated at $20^\circ \pm 5^\circ\text{C}$ and at 120 ± 12 VAC.
- 1.7.7.5 The equipment being tested shall withstand and operate normally when one discharge pulse of ± 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second:
 - 1.7.7.5.1 Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns.
 - 1.7.7.5.2 The unit under test will be operated at $20^\circ \pm 5^\circ\text{C}$ and at 120 ± 12 VAC.
- 1.7.7.6 The controller unit communications modules shall be tested resident in a STATE accepted controller unit, which in turn is housed in the cabinet.
- 1.7.7.7 Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."
- 1.7.7.8 Equipment shall continue normal operation when subjected to the following:
 - 1.7.7.8.1 Low Temperature Test - With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be lowered from 20°C to -34°C at a rate of not more than 16°C per hour. The item shall be cycled at -34°C for a minimum of 12 hours and then returned to 20°C at the same rate. The test shall be repeated with the line voltage at 135 VAC.

- 1.7.7.8.2 High Temperature Test - With the item functioning at a line voltage of 90 VAC in its intended operation, the ambient temperature shall be raised from 20°C to 73°C at a rate of not more than 16°C per hour. The item shall be cycled at 73°C for 12 hours and then returned to 20°C at the same rate. The test shall be repeated with the line voltage at 135 VAC.
- 1.7.7.8.3 All equipment shall resume normal operation following a period of at least 12 hours at -34°C and less than 10 percent humidity and at least 12 hours at 73°C and 90 percent humidity when 90 VAC is applied to the incoming AC.
- 1.7.7.9 The relative humidity and ambient temperature values in the following table shall not be exceeded.

AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY
AT BAROMETRIC PRESSURES (29.92 Inches of Hg.)

Ambient Temperature/ Dry Bulb (in °C)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in °C)
-34.0 to 1.1	10	-17.2 to 42.7
1.1 to 46.0	95	42.7
48.8	70	42.7
54.4	50	42.7
60.0	38	42.7
65.4	28	42.7
71.2	21	42.7
73.0	18	42.7

- 1.7.7.10 All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

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CHAPTER 2

SPECIFICATIONS FOR MODEL 170E CONTROLLER UNIT MODEL 412 PROGRAM MODULE MODEL 170E/HC-11 CONTROLLER UNIT AND HC-11 CPU BOARD

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SECTION 1 – GENERAL REQUIREMENTS

- 2.1.1 **Power Failure:** A power failure is said to have occurred when the incoming line voltage falls below 92 (± 2) VAC for 50 ms. The determination of the 50 ms interval shall be completed within 67 ms of the time the voltage falls below 92 (± 2) VAC.
- 2.1.2 **Power Restoration:** Power is said to be restored with the incoming line voltage equals or exceeds 97 (± 2) VAC for 50 ms. The determination of the 50 ms interval shall be completed within 67 ms of the time the voltage first reaches 97 (± 2) VAC.
- 2.1.3 **Power Conditions:** A reaction period of 16.7 ms (one 60 Hz cycle) may be added to the 50 ms Power Failure or Power Restoration timing as shown in Section 2.1.1 or Section 2.1.2 respectively. The hysteresis between power failure and power restoration voltage settings shall be a minimum of 5 volts with a threshold drift of no more than 0.2 VAC.
- 2.1.4 **The general system address organization** of the Model 170E controller shall be as listed below. The internal module address organization shall be as specified in the appropriate module section.

Function	Address Range	Comments
CPU SRAM	0000 – 07FF	----
DTA Minutes	5000 – READ	5000 Write reset DTA
Input/Output	5001 – 500A	5001 BIT 1 Input assigned to restart timer – 5009 & 500A Read <i>reserved</i>
<i>Reserved</i>	500B – 500E	----
DTA Seconds	500F – READ	500F Write <i>reserved</i>
<i>Reserved</i>	5010 – 5FFF	----
Real Time Clock Reset	5FFF – WRITE	5FFF Read <i>reserved</i>
ACIA No. 1	6000	Write CR, Read SR
ACIA No. 1	6001	Write TDR, Read RDR
ACIA No. 2	6002	Write CR, Read SR
ACIA No. 2	6003	Write TDR, Read RDR
ACIA No. 3	6004	Write CR, Read SR
ACIA No. 3	6005	Write TDR, Read RDR
ACIA No. 4	6006	Write CR, Read SR
ACIA No. 4	6007	Write TDR, Read RDR
<i>Reserved</i>	6008 – 6FFF	----
Program Module	0800 - 4FFF	----
	7000 - FFFF	----

Table Note:
Address locations noted as *Reserved* are assignable by the STATE only and shall not be used.

2.1.5

The general system address organization of the Model 170E/HC-11 controller unit shall be as listed below. The internal module address organization shall be as specified in the appropriate module section.

Function	Block Size (Bytes)	Location	Comments
170 RAM	24K	0000-5FFF	CPU Board RAM
RAM	4K	6000-6FFF	INT. Jumper Position (See note below)
CONFIG. REG. + RAM	1K	7000-73FF	Initiate immediately on start up.
Input/Output	512	7400-75FF	External I/O Functions
RAM	2K	7600-7FFF	CPU Board RAM
EPROM	32K	8000-FFFF	CPU Board PROM Memory
Switch	1	700A	Feature Switch HC-11 Port E
Switch	1	7000	Location Switch HC-11 Port A
Switch	1	7002	PROM Bank Switch Select HC-11 Port G - BIT 1
Status Indicator	1	7002	HC-11 Port G - BIT 3 (1 = on)
Configuration Reg.	96	7000-705F	68HC-11 Configuration Registers
RAM	1K (-96)	7060-73FF	68HC-11 RAM
DTA Minutes	1	7400	I/O DTA Read Minutes
DTA Seconds	1	740F	I/O DTA Read Seconds
Input/Output	10	7401-740A	I/O READ and WRITE
ACIA	8	7410-7417	Serial Ports SP1 - SP4
DPR	8	7500-7507	Dual Port Semaphores
IRQ/STAT	1	75FF	60 Hz RESET and IRQ STATUS
RAM	2K	7600-7FF7	CPU Board RAM
Reserved	8	7FF8-7FFF	Reserved Clock/Calendar operation

Table Note: EXT JUMPER position is Configuration #2.
 Configuration #2 redirects address 6000-6FFF to the Prom Module slot.

2.1.6

The total memory access time including buffering, decoding, device access time, and accessed data presented to the controller data bus shall not exceed 300 ns. The memory device shall have read and write (if applicable) times suitable to perform either function in one MPU instruction cycle.

2.1.7

Each memory device shall stabilize to normal operation within 10 ms following power restoration and shall be in standby until addressed. Each device shall have the following maximum power drain at +5 VDC in its various states:

<u>MEMORY</u>	<u>ACTIVE</u>	<u>STANDBY</u>	<u>POWERDOWN</u>
EPROM	100 mA	40 mA	-
SRAM	85 mA	20 mA	100 µA (non-internal power)

- 2.1.8 **CPU EPROM memory sockets** shall be a 28 Pin AMP Diplomate LF #641894 2 (or equal). The MPU, ACIA and other memory sockets shall be an AUGAT #500/800 series AG10DPC (or equal). Each socket number shall be permanently marked on the PCB adjacent to its Pin 1. Should the "...or equal MPU" Pin/Package be other than the 40 pin package, the MPU socket used shall match the above specified socket features.
- 2.1.9 **If a PAL, EPROM, or ROM device is used** in address decoding and timing algorithms, the device code listing, together with data sheet(s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the Contractor uses to directly reproduce the device.
- 2.1.10 **The traffic signal control program** and PROMS with PROM module for the Model 170E will be furnished by the STATE.

SECTION 2 – MODEL 170E CONTROLLER UNIT REQUIREMENTS

2.2.1 Unit Composition

2.2.1.1 The Controller Unit shall consist of the following:

- Central Processing Unit with 6800 MPU
- Input/Output Interface
- Unit Chassis
- Unit Power Supply with external power connection
- Unit Standby Power
- Front Panel Assembly (FPA)
- Internal System Interface
- Connectors C1S, C2S, C20S, C30S, C40S, and T-1
- Communications System Interface
- Model 400 Modem
- Model 412 Program Module

2.2.1.2 The composition weight shall not exceed 11.5 kg.

2.2.2 Central Processing Unit (CPU)

2.2.2.1 The CPU shall be provided with a 6800 MPU and shall properly execute object programs developed to operate on the MPU. The MPU interrupt requirements shall be as follows:

2.2.2.1.1 Non-Maskable Interrupt (NMI): The NMI is exclusively assigned to the power failure function. A power failure shall cause the MPU NMI line to immediately go LOW. The line shall be held LOW until the RES goes LOW to prevent multiple NMI issuance.

2.2.2.1.2 Reset Interrupt (RES): The RES is exclusively assigned to power restoration and MPU startup. The RES line shall go LOW 3 (± 1) ms following the NMI going LOW. The line shall remain LOW until 150 (± 75) ms after power restoration.

2.2.2.1.3 Interrupt Request (IRQ): The IRQ line shall be jointly used by the RTC and the four ACIAs to initiate an IRQ to the MPU.

2.2.2.1.3.1 Real Time Clock (RTC): RTC circuitry shall be provided to trigger an interrupt to the MPU on the IRQ line once every 1/60 of a second during the 270° to 330° portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency. The RTC shall be READ at bit 8, Address 5FFF (status) and reset by a WRITE to Address 5FFF.

- 2.2.2.1.3.2 Asynchronous Communication Interface Adapter (ACIA): Four ACIAs shall be provided, each capable of receiving and transmitting up to 8 bits of parallel data from the MPU for serial data communications. Each ACIA shall have four registers that are addressable by the MPU. The MPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR), and writing in the Transmit Data Register (TDR) and in the Control Register (CR).
- 2.2.2.1.3.3 Each ACIA shall be provided with a 2-post type jumper between its IRQ output and the MPU IRQ input. The controller shall be delivered with these jumpers installed.
- 2.2.2.2 CPU Clock Timing - The CPU clock circuitry shall be provided to generate the MPU clock timing. The clock circuitry and the MPU shall provide two selectable MPU machine cycle times of 0.651 and 1.302 ($\pm 0.0015 \mu\text{S}$). The machine cycle time selection shall be by Post Jumper (3-post type) with jumper in for 1.302 μS . The CPU clock circuitry shall be located no further than 50 mm from the MPU clock pin inputs.
- 2.2.2.3 SRAM memory, DALLAS 1235Y (or equal), shall be provided.
- 2.2.2.4 An EPROM memory, INTEL 27256A (or equal), shall be provided in socket U6.
- 2.2.2.5 Restart Timer: A Restart Timer Circuitry shall be provided to react to the duration of power outage. The Restart Timer output is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (± 0.25) seconds, its output state shall go to LOW and remain in that state for 50 (± 24) ms after the RES line goes HIGH. If power is restored prior to the timer timing out, the output shall remain HIGH and the timer shall be reset to "0".
- 2.2.3 **Downtime Accumulator (DTA)**
 - 2.2.3.1 A DTA shall be provided to accumulate time between power failure and restoration. The DTA shall start counting immediately upon NMI line going LOW and continue counting until the RES line goes HIGH following power restoration.
 - 2.2.3.2 The DTA shall have two, 8-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ± 1 second over the 255-minute range. The DTA shall stop counting when the Minutes register equals 255 decimal. Both DTA registers shall reset to "0" by a WRITE to Address 5000. The DTA shall READ minutes at Address 5000 and seconds at Address 500F. The Seconds register shall count 0 to 59 seconds decimal in 1 second increments. At 60 seconds, the Minutes register shall be incremented and the Seconds register shall reset to "0".
 - 2.2.3.3 Total current drain for DTA and Restart Timer Circuitry (powerdown mode) shall not exceed 400 μA at 5 VDC, 35° C while timing and 100 μA at 5 VDC when timeout is latched.

2.2.4 Input/Output Interface

2.2.4.1 Input/Output interface shall utilize a ground true logic. The transfer of data between interface and working registers within the MPU shall be in 8-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of MPU read/write command at the time the given address is valid.

2.2.4.1.1 Output Interface: The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

2.2.4.1.2 Input Interface: The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each Logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC; shall be turned OFF (false) when the input current is less than 100 μ A or the input voltage exceeds 8.5 VDC; shall pull up to 12 VDC; and shall not deliver in excess of 20 mA to a short circuit to Logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

2.2.5 Unit Chassis

2.2.5.1 The controller unit shall be housed in a compact, portable metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 483 mm rack. The enclosure shall be designed for convenient removal of PCBs without use of tools.

2.2.6 Unit Power Supply

2.2.6.1 A power supply shall be provided to produce all DC power necessary to operate the controller unit. In addition, the supply shall provide the following voltages and current:

1,000 mA at	+12	(\pm 0.5 VDC)
300 mA at	-12	(\pm 0.5 VDC)
500 mA at	+5	(\pm 0.25 VDC)
400 mA at	-5	(\pm 0.25 VDC)

- 2.2.6.2 The DC ground shall not be connected to the EG.
- 2.2.6.3 Controller unit power shall be held up (DC Logic voltages at normal operating levels) for a minimum of 50 (± 17) ms beyond the NMI line going LOW.
- 2.2.6.4 The maximum DC voltage generated shall not exceed 45 volts.
- 2.2.6.5 The power supply shall be so designed that no further filtering regulation is needed for the required DC voltages.
- 2.2.6.6 Radio frequency suppressors shall be provided on the AC+ and AC- power lines. The part shall be a COR COM 3VS1 (or equal).
- 2.2.7 **Unit Standby Power**
 - 2.2.7.1 A standby power shall be provided to retain power (minimum of 72 hours) to the CPU Restart Timer, DTA and Internal RTCA during power failure in the controller unit. The supply shall consist of holdup capacitors, capacitor charging circuitry, and power sense/transfer circuitry.
 - 2.2.7.2 The power sense/transfer circuitry shall sense power loss and transfer capacitor power immediately to the required circuits. The transfer circuitry shall isolate the capacitors by transistor or relay until power loss transfer. The circuitry shall sense power restoration and transfer back to the normal isolation mode.
 - 2.2.7.3 A charging circuit that shall, under normal operating conditions, fully charge and float the standby capacitors consistent with manufacturer's recommendations.
- 2.2.8 **Front Panel Assembly**
 - 2.2.8.1 The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.
 - 2.2.8.2 The front panel shall be electrically connected by means of Connector C3. The front panel shall be connected to EG through Connector C3.
 - 2.2.8.3 The character displays shall be hexadecimal with circuits to accept, store, and display 4 bit binary data. The characters shall be 10 mm high, minimum. Each character shall have latch, strobe, and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent resistant. The transfer of data from the MPU through the output interface to the display shall result in the display of each character in its non-inverted state.

- 2.2.8.4 The front panel shall be provided with 10 LED call/ACTIVE indicators.
- 2.2.8.5 A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MPU shall result in each character being received in its non-inverted state. The character shall consist of four bits of binary data, while the character control shall consist of one bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 5 mm², and shall be mounted on 13 mm centers, minimum; shall have an actuation force between 50 and 100 grams; and shall provide a positive tactile indication of contact. Key contacts shall have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact opening.
- 2.2.8.6 The front panel shall be provided with a toggle Logic switch to enable the stop timing function and shall be labeled "STOP TIMING".
- 2.2.8.7 An "ON-OFF" toggle control switch and fuse shall be provided for AC power. The switch and fuse shall protrude through the front panel, but shall remain with the controller unit chassis when the front panel is removed. The fuse shall be a 3AG Slow Blow type, rated at either 1 or 2 amps, dependent upon the controller unit power requirements.
- 2.2.8.8 The Front Panel used with a Model 170E/HC-11 Controller Unit does not require a program module opening as shown on Drawing No. 1 and specified in note 3 thereon. A Front Panel supplied with such an opening shall have the opening covered. The material used for the FPA Blank Cover shall be the same material as used for the Front Panel and of a size sufficient to provide secure mounting to the FPA, but in no case larger than 165 x 55 mm. Exposed corners shall be rounded.
- 2.2.9 **Internal System Interface**
- 2.2.9.1 PCB to PCB Connector spacing shall be a minimum of 25 mm. Continuous Nylon card guides (permanent locking type) shall be provided for the modules and all internal PCBs.
- 2.2.9.2 Two PCB 22/44S Connectors shall be provided for the Modem Modules MC1 and MC2.
- 2.2.9.3 The depth placement of the program module connector shall be such that the program module front panel shall be flush with the Controller Unit front panel when the module is connected.

2.2.10 **Data and Address Bus Requirements**

- 2.2.10.1 All data bus buffers and data bus drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 pF. The propagation delay time shall be less than 30 ns.
- 2.2.10.2 All address bus inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 pF.

2.2.11 **Connector Requirements**

- 2.2.11.1 Connector C1S shall be mounted on the controller unit providing 44 inputs and 56 outputs of control interface to and from external devices or files.
- 2.2.11.2 The Model 400 Modem and ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (TYPE T Connector). The control and data transmission lines for ACIA 1 shall be paralleled through C2S and T-1 connectors. ACIA 2 lines shall be routed to C20S Connector, ACIA 3 to C30S, and ACIA 4 to C40S.

2.2.12 **Communication System Interface**

- 2.2.12.1 The communication system shall consist of the CPU; ACIAs; motherboard and daughterboard connectors & lines; Modem Module Connectors MC1 & MC2 & interfaces between ACIA & Modem; and both Modem & ACIA to C2S, C20S, C30S, C40S, and Connector T-1 Terminal. The interface between the ACIA and Modem shall comply with EIA-232-C Standards and all functions under T-1, C2S, C20S, C30S, and C40S Connectors are referenced to the ACIA. AUDIO IN and AUDIO OUT are referenced to the Modem. The RTS and TX data lines to the Modem shall have MARK and SPACE voltages of -12 and 12 VDC respectively. Schematic diagrams for the motherboard and daughterboard are provided in Drawing Numbers 16 and 17, respectively.
- 2.2.12.2 C20S, C30S, and C40S Connectors shall meet the requirements for the C2 Connector.
- 2.2.12.3 A minimum of four baud rate frequencies, 19.2 kHz, 38.4 kHz, 76.8 kHz, and 153.6 kHz shall be provided at the ACIA Rx/Tx Clock Inputs (pins 3 & 4). The frequency selection shall be by post type jumpers. Each ACIA shall have independent baud rate selection with jumpers delivered pinned for 19.2 kHz.

2.2.13 Electrical Requirements

2.2.13.1 The front panel and chassis shall be connected to EG.

2.2.13.2 A surge arrestor shall be provided between the AC+ and AC- for protection against power line noise transients. The surge arrestor shall meet the following requirements:

Recurrent peak voltage: 212 volts
Energy rating, maximum: 20 Joules
Power dissipation, average: 0.85 watt
Peak current for pulses less than 6 μ S: 2,000 amperes
Standby currents: Less than 1 mA

2.2.13.3 Two 0.5 ohm, 10 watt wire-wound power resistors with a 0.2 μ H inductance shall be provided (one on the AC+ power line and one on the AC- line). Three surge arrestors rated for 20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68 μ F capacitor shall be added between AC+ and AC- coming off the 0.5 ohm resistor.

2.2.13.4 The AC power to the controller unit shall be supplied by a 3-conductor cable at least one meter in length. The cable shall terminate in a NEMA Type 5-15P grounding-type plug.

2.2.13.5 Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 1.6 mm diameter and 5 mm high, minimum. The clearance between test points and other components shall be 6.5 mm, minimum.

SECTION 3 – MODEL 412 PROGRAM MODULE REQUIREMENTS

- 2.3.1 **System Memory Module** (Provided with Model 170E Controller only.)
- 2.3.1.1 The module shall comply with the details and connections shown on the drawings herein for the controller PROM module.
- 2.3.1.2 All electrical connections in and out of this module shall be through a printed circuit connector having two rows of 36 independent bifurcated contacts on 2.54 mm centers. The module PCB connector shall be provided with electrostatic charge protection to prevent CMOS device damage.
- 2.3.1.3 The module shall be designed so that persons inserting or removing the assembly shall not be required to insert hands or fingers within the controller unit housing this modular assembly. A handle or gripping device protruding no more than 30 mm from the front panel shall be attached to the front of the assembly. The front panel shall be connected to EG.
- 2.3.1.4 The total module current requirements shall not exceed 450 mA at +12 VDC and 100 mA at +5 VDC.
- 2.3.1.4.1 All data inputs and outputs shall be tri-state buffered, enabling them to drive a load consisting of 10 TTL gates and 200 pF. When this module is not being addressed, the data output and input shall be disabled into a high impedance state and the data I/O lines shall not source or sink more than 100 μ A. All address inputs shall not load the bus by more than 1TTL gate load and 100 pF.
- 2.3.1.5 The memory shall consist of addressable locations (blocks) from 0000 to FFFF. The minimum configurations the module shall be capable of addressing are the following:

Configuration 1

A000 – FFFF	EPROM (27256)
8000 – 9FFF	RAM, NON-VOLATILE RAM
7000 – 77FF	RAM, NON-VOLATILE RAM
0800 – 4FFF	RAM, NON-VOLATILE RAM

Configuration 2

8000 – FFFF	EPROM (27256)
7000 – 7FFF	RAM, NON-VOLATILE RAM
0400 – 4FFF	RAM, NON-VOLATILE RAM

- 2.3.1.5.1 The module will be user programmable, capable of a minimum of the previously defined configurations. The memory devices to be used on the module (EPROM, RAM, NON-VOLATILE RAM) will be specified by the STATE.
- 2.3.1.6 The module shall operate and intermate with the controller unit.
- 2.3.1.7 The front panel of the module shall be labeled "Model 412".

SECTION 4 – MODEL 170E/HC-11 CONTROLLER UNIT REQUIREMENTS

2.4.1 Unit Composition

2.4.1.1 The Controller Unit shall consist of the following:

- Central Processing Unit with 68HC11F1 MPU
- Input/Output Interface
- Unit Chassis (per Model 170E)
- Unit Power Supply with external power connection
- Unit Standby Power
- Front Panel Assembly (FPA per Model 170E)
- FPA Blank Cover
- Internal System Interface
- Connectors C1S, C2S, C20S, C30S, C40S, and T-1
- Communications System Interface
- Model 400 Modem(s)

2.4.1.2 The composition weight shall not exceed 11.5 kg.

2.4.2 Central Processing Unit (CPU) Module

2.4.2.1 This specification defines a replacement CPU board for the 6800 MPU based CPU board in the standard 170E controller and should conflicts arise in components or parameters, those components or parameters necessary to support the functions specified in this section shall take precedence.

2.4.2.2 The HC-11 CPU Module shall operate a 68HC11F1 MPU and shall functionally replace the existing 6800 MPU and prom board (System Memory Module) in the Model 170E.

2.4.2.2.1 The MPU shall operate with a crystal frequency of 8MHz.

2.4.2.2.2 The MPU shall be socket mounted in an AMP PLCC socket #821574-1 series HPT or equal.

2.4.2.3 Four 6850 communication ICs operating with a crystal frequency of 6.144 MHz shall be provided.

2.4.2.3.1 Each communication IC shall have programmable jumpers to select baud rates of 1200, 2400, 4800, 9600 and 19200.

2.4.2.3.2 No IRQ inhibits shall be provided. All ACIA ports shall be active and shall be software initialized at startup.

2.4.2.3.3 An IRQ status register shall be provided as specified in Chapter 2, Section 2 of this specification.

- 2.4.2.4 The RAM shall be socket mounted and resident on the CPU board.
 - 2.4.2.4.1 The RAM socket shall be a 28 pin Augat 828 series or equal.
 - 2.4.2.4.2 If an RTC clock is not required, the RAM will be continuous from locations \$0000 to \$6FFF. The RAM shall be a zero power device exclusively (Dallas 1230 or equal).
 - 2.4.2.4.3 If an RTC clock is required, the RAM shall be a Dallas 1644 or equal. The clock address shall be in the I/O map at location \$7FF8 to \$7FFF.
 - 2.4.2.4.4 A jumper select shall be provided to switch RAM locations \$6000 to \$6FFF from 'internal' (Configuration #1) to 'external' (Configuration #2) for access to the remote Dual Port location. The status of the jumper position shall be read at bit 5 on the IRQ register. Dedicated access for dual port configuration to RAM locations \$6000 to \$6FFF only shall be provided when an enhanced Program Module is used.
- 2.4.2.5 The EPROM shall be socket mounted and resident on the CPU board.
 - 2.4.2.5.1 The EPROM socket shall be a 32 pin ZIF force device.
 - 2.4.2.5.2 The EPROM shall be jumper selectable to function as either a 32K x 8 or a 128K x 8 device.
 - 2.4.2.5.3 When using a 128K EPROM, a bank switch shall be enabled within the EPROM memory system and shall function by moving to the upper 64K segment. The bank switch jumper controls address line A16. The bank shall be activated by a 'write' to location \$7002 (directly connected to Port G on the HC-11 MPU) and will enable an extra 32K of EPROM memory. The status of A16 will be read at bit 6 on the IRQ register.
- 2.4.2.6 An eight-position, front reading DIP switch used as a 'feature switch' and addressed at \$700A (Port E), shall be provided on the front portion of the CPU board.
- 2.4.2.7 An eight-position, front reading DIP switch used as a 'location switch' and addressed at \$7000 (Port A), shall be provided on the front portion of the CPU board.
- 2.4.2.8 A header shall be provided near the front of the CPU module for the SPI and serial interface pins.
- 2.4.2.9 An LED indicator shall be located on the front of the CPU board and shall be controlled by a software output of Port G, bit 3.
- 2.4.2.10 Transorb protection shall be provided on voltages (+12VDC, -12VDC and +5VDC) input to the CPU board.

2.4.2.11 Internal Module Address Organization

2.4.2.11.1 The decoder for the two CPU Module system address organizations shall be furnished in address '1'.

2.4.2.11.2 The two address configurations shall be selectable by use of a three-post jumper labeled 'INT' and 'EXT'. The input line 'state condition' shall cause the decoder to provide the address configuration shown below.

Input Line	Configuration	Function
INT	1	Address 6000 – 6FFF shall reside on the internal RAM.
EXT	2	Address 6000 – 6FFF shall reside on the external Program Module.

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CHAPTER 3

SPECIFICATIONS FOR MODEL 200 SWITCH PACK, MODEL 204 FLASHER UNIT, AND MODEL 430 FLASH TRANSFER RELAY

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SECTION 1 – GENERAL REQUIREMENTS

- 3.1.1 **The module chassis** providing rigid unit support (for connector mounting, PCB support, module alignment, and insertion/removal) and triac heat sinking shall be made of metal suitable to meet support and environmental requirements. Where electrical isolation protection is the only requirement, plastic insulation material may be used in lieu of metal.
- 3.1.2 **Each module** shall be so constructed such that persons inserting or removing the module will not be exposed to any parts having live voltage. A handle shall be attached to the front of Model 200 and 204 modules to facilitate the module insertion or removal from its mating connector.
- 3.1.3 **The Model 200 and 204 modules** shall be so constructed that their lower surfaces will be no more than 53 mm below the centerline of the connector and that no part will extend more than 23 mm to the left or 28 mm to the right of the centerline of the connector pin array.
- 3.1.4 **Continuous edge guides** shall be provided on the Model 200 and 204 modules.
- 3.1.5 **The front panel** of the Model 200 and 204 modules shall be provided with one indicator per switch. The indicators shall be vertically centered on the front panel with top and bottom indicators no more than 25 mm from the panel vertical center.
- 3.1.6 **Switches**
- 3.1.6.1 Each switch shall have the capability of switching any current from 0.05 to 15 amps (AC) of tungsten lamp load or 15 amps (AC) at a power factor of 0.85.
- 3.1.6.2 Each switch shall turn ON within $\pm 5^\circ$ of the "0" voltage point of the AC sinusoidal line, and shall turn OFF within $\pm 5^\circ$ of the "0" current point of the AC sinusoidal line. After power restoration, the "0" voltage turn ON may be within $\pm 10^\circ$ of the "0" voltage point only during the first half cycle of line voltage during which an input signal is applied. Turn ON and OFF shall be within 8.33 ms following application or removal of the Logic signal, respectively.
- 3.1.6.3 Each switch shall be designed for a minimum of 300 million operations while switching a tungsten filament load of 1,500 watts at 70°C.
- 3.1.6.4 Each switch shall have isolation between input DC control and AC to lights output circuit of at least 2,000 VDC and 10,000 megohms DC.
- 3.1.6.5 Each switch shall have a 1-cycle surge rating of 175 amps RMS and a 1-second surge rating of 40 amps RMS.

- 3.1.6.6 Each switch shall be capable of withstanding a peak inverse voltage of 500 volts at 70°C and no more than 20 mA leakage.
- 3.1.7 **The connector plug contact tails** shall be solder hook or eye styles only. PCB (soldered to the PCB) and quick connect connection styles are not allowed.
- 3.1.7.1 Exception: Load switches and flashers having all components totally encapsulated on the connector shall be permitted [Traftech 200/204 (or equal)].

SECTION 2 – MODEL 200 REQUIREMENTS

- 3.2.1 **The Model 200 Solid State Switch Pack** shall be a modular plug-in device containing three solid state switches to be used for opening and closing connections between the applied power and an external load.
- 3.2.2 **A LOW state input** (negative true logic) from the controller unit (saturated NPN transistor, 0 to 6 VDC) shall cause the switch to be energized. A HIGH state input [cut-off NPN transistor, 10 VDC (or greater)] shall cause the switch to de-energize. The state transition (conducting to nonconducting or vice versa) shall occur between 6 and 16 VDC.
- 3.2.3 **The incoming logic signal** shall not sink more than 20 mA nor be subjected to more than 30 VDC.
- 3.2.4 **The module** shall not draw more than 60 mA at +16 VDC (or greater) from the cabinet power supply with all switches ON.
- 3.2.5 **Each switch** shall have an OFF state dv/dt rating of 100 volts per μ S (or greater).
- 3.2.6 **The indicators** shall be labeled or color-coded from top to bottom: “Red”, “Yellow”, and “Green”. Each indicator shall indicate a controller unit output circuit.
- 3.2.7 **The input circuit** of each switch shall have reverse polarity protection.
- 3.2.8 **The resistance** between the AC+ input terminal and the AC+ output terminal of each switch shall be 15,000 ohms, minimum, when the switch is in the open position. The output current from the switch through the load when the load switch is in the OFF state shall not exceed 20 mA, peak.
- 3.2.9 **Each switch** shall be isolated so that line transients or switch failure will not adversely affect the controller unit.
- 3.2.10 **The plug connector** shall be a BEAU P-5412-LAB (or equal).

SECTION 3 – MODEL 204 REQUIREMENTS

- 3.3.1 **The Model 204 Flasher Unit** shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. The module's function is to alternately open and close connections between the applied power and an external lamp load during flashing operation.
- 3.3.2 **The module** shall generate its own internal DC power for Logic and Control from the AC line.
- 3.3.3 **The module** shall commence flashing operation when AC power is applied to the module.
- 3.3.4 **The circuit** shall provide 50 to 60 flashes per minute with a 50% duty cycle.
- 3.3.5 **A surge arrestor** shall be provided between AC+ (Pin 11) and Flasher Out (Pins 7 & 8). The surge arrestor shall be capable of reducing the effects of a transient voltage applied to the field signal circuits and shall have the following ratings:
- Recurrent peak voltage: 212 volts
 - Energy rating, maximum: 50 Joules
 - Power dissipation, average: 0.85 watt
 - Peak current for pulses less than 6 μ S: 2,000 amperes
 - Standby currents: Less than 1 mA
- 3.3.6 **Each switch** shall have an OFF state dv/dt rating of 100 volts per μ S (or greater).
- 3.3.7 **The indicators** shall indicate the output state of the switches.
- 3.3.8 **The plug connector** shall be a BEAU P-5406-LAB (or equal).
- 3.3.9 **Each circuit** shall be designed to operate in an open circuit condition (without load) for 10 years (or greater).

SECTION 4 – MODEL 430 REQUIREMENTS

3.4.1 Flash Transfer Relay

- 3.4.1.1 The flash transfer relays shall be heavy-duty type. The coil of the relay shall be energized only when the signals are in flashing operation and the police panel ON/OFF switch is ON. The relay shall transfer the field outputs from switch pack output to flash control. The transfer shall not interrupt the controller unit operation.
- 3.4.1.2 Relays shall be the electro-mechanical type designed for continuous duty.
- 3.4.1.3 Each relay shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating, and part number shall be placed on the cover. They shall be permanent, durable, and readily visible.
- 3.4.1.4 Each relay shall be provided with DPDT contacts. Contact points shall be of fine silver, silver alloy, or superior alternative material. Contact points and arms shall be capable of switching a 20 ampere at 120 VAC tungsten load per contact once every 2 seconds with a 50% duty cycle for at least 250,000 operations without contact welding or excessive burning, pitting, or cavitation.
- 3.4.1.5 The relay coil shall have a power consumption of 10 volt-amperes, maximum.
- 3.4.1.6 Each relay shall withstand a potential of 1,500 VAC at 60 Hz between insulated parts and between current carrying or non-current carrying parts. Each relay shall have a 1-cycle surge rating of 175 amperes RMS.

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CHAPTER 4

SPECIFICATIONS FOR MODELS 208 AND 210 MONITOR UNITS

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SECTION 1 – GENERAL REQUIREMENTS

- 4.1.1 **The monitor unit** shall render reliable detection and cause a relay output contact condition FAILED state when sensing the following:
 - 4.1.1.1 In the Model 208 Monitor Unit:
 - The cabinet +24 VDC power supply voltage is below specified threshold
 - A WDT time-out condition
 - 4.1.1.2 In the Model 210 Monitor Unit:
 - The cabinet +24 VDC power supply voltage is below specified threshold
 - A WDT time-out condition
 - Conflicting field output circuits are ON together
- 4.1.2 **FAILED State Output Circuits**
 - 4.1.2.1 An electro-mechanical relay shall be provided to switch an output circuit during a FAILED state. The relay coil shall be energized in a non-FAILED state.
 - 4.1.2.2 The relay contacts shall be rated for a minimum of 3 amps at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 ms (or less).
- 4.1.3 **Monitor Unit Reset**
 - 4.1.3.1 A momentary SPST switch labeled RESET shall be provided on the unit front panel to reset the monitor unit circuitry to a non-FAILED state. The switch shall be so positioned on the front panel that the switch can be operated while gripping the front panel handle.
 - 4.1.3.2 A reset issuance (Unit Reset) shall be a 1-time input to prevent the monitor from constant reset.
- 4.1.4 **A monitor Logic and driver power** shall be generated from an internal unit power supply except for WDT and +24 VDC cabinet voltage sense circuits. The WDT sense circuit power may be derived from either power supply. Circuits on the monitor that are “powered” by the +24 VDC cabinet power supply shall be optically isolated from those deriving their power from the monitor unit internal supply. The monitor shall not draw more than 500 mA from the +24 VDC cabinet power supply. Failure to provide reliable operating voltage levels shall cause a FAILED state.

SECTION 2 –POWER SUPPLY MONITOR REQUIREMENTS

- 4.2.1 **The monitor unit** shall sense an external +24 VDC power supply output voltage.
- 4.2.2 **Voltages** sensed at +18 VDC (or below) for a duration of 500 ms (or longer) shall cause a FAILED state.
- 4.2.3 **Voltages** sensed at +22 VDC (or above) shall NOT cause a FAILED state.
- 4.2.4 **Voltages** sensed below +22 VDC for a duration of 200 ms (or less) shall NOT cause a FAILED state.
- 4.2.5 **All timing and voltage conditions** other than those specified above may or may not cause a FAILED state.
- 4.2.6 **A FAILED state** caused by sensing the power supply shall illuminate a front panel indication light labeled “VDC FAILED”. The indicator shall remain ON until Unit Reset.
- 4.2.7 **Only Unit Reset** shall reset the power supply sense circuitry from a FAILED state.

SECTION 3 – WATCHDOG TIMER MONITOR REQUIREMENTS

- 4.3.1 **WDT circuitry** shall be provided to monitor a controller unit output line state routed to the monitor unit at its assigned pin. The WDT circuitry shall sense any line state change and the time between it and the last change. No state change for 1.5 (± 0.1) seconds shall cause a FAILED state. The timer shall reset at each state change in a non-FAILED state.
- 4.3.2 **Only the Unit Reset** or a WDT inactive due to the voltage sense shall reset the WDT from a FAILED state.
- 4.3.3 **A FAILED state** caused by the WDT shall illuminate a front panel indicator light labeled “WDT ERROR”. The indicator shall remain ON until WDT is reset from a failed state.
- 4.3.4 **The WDT circuitry** shall sense the incoming VAC line and, when the voltage falls below 98 (± 2) VAC for 50 (± 17) ms, shall inhibit the WDT function. When the WDT circuitry senses the incoming VAC line rise above 103 (± 2) VAC for 50 (± 2) ms, the WDT shall become active. A hysteresis between the Voltage Inhibit and the Voltage Active settings shall be a minimum of 3 volts.

SECTION 4 – MODEL 210 CONFLICT MONITOR REQUIREMENTS

4.4.1 Conflicting Field Output Circuits

- 4.4.1.1 The monitor unit shall monitor up to 32 field output circuits using a 16 conflicting channel (green and yellow outputs logically OR-gated internally together) comparison setup. The specified, associated cabinet output file assignment or operator-selected output switches will determine channel assignment.
- 4.4.1.2 All monitored field output voltages shall be measured as true RMS responsive (up to 3 kHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of two cycles. If digital means are used in calculating RMS, a minimum of two samples shall be taken per alternation.
- 4.4.1.3 Sensed conflicting field output voltages 25 VAC (or greater) for a duration of 500 ms (or longer) shall cause a FAILED state.
- 4.4.1.4 Sensed conflicting field output voltages 15 VAC (or less) or any voltage having a duration of 200 ms (or less) shall NOT cause a FAILED state.
- 4.4.1.5 Sensed conflicting field output voltages between 15 and 25 VAC and for a duration greater than 200 ms and less than 500 ms may or may not cause a FAILED state.
- 4.4.1.6 The conflict monitoring circuitry shall be capable of detecting both a positive and negative half-wave failure under the foregoing conditions.
- 4.4.1.7 A FAILED state caused by sensing voltage conflicts shall be reset only by the Unit Reset.
- 4.4.1.8 Sixteen (16) indicators shall be provided on the unit front panel to indicate if the channel output is sensed ON. The indicators shall remain ON in a latched state during a FAILED state unless unlatched by Unit Reset or a unit loss of power during said FAILED state.

4.4.2 Conflict Programming Card

- 4.4.2.1 A plug-in PCB programming card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes [#1N4148, (or equal)]. Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically labeled and laid out for easy identification of the diodes by channel. With diodes in place, all output channels being monitored shall be in conflict. When the diode (anode to numerical pins and cathode to alphabetical pins) has been removed, the channels shall be defined as non-conflict.

- 4.4.2.2 A pad for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin and the 'inhibit common' shall disable sensing the said channel yellow.
- 4.4.2.3 The programming card shall be 152 mm in depth and 131 mm to 134 mm in height, and shall intermate with a 28/56 pin, double-sided connector having bifurcated contacts on 3.96 mm centers. The printed circuit board shall bisect its edge board fingers at their centers to within ± 0.41 mm. The center of the edge board fingers shall be 67 mm from either edge of the board. This card, when installed, shall be provided with card ejectors [Stanford Applied Engineering Type 6100 (or equal)] for removal from the front panel. This programming card shall be flush with the front panel and slide smoothly on its tracks while being inserted into or removed from the monitor module.
- 4.4.2.4 Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.
- 4.4.2.5 The programming cards shall be supplied with all diodes installed. The yellow inhibit jumpers shall be installed on all 16 channels to inhibit all yellow monitoring.
- 4.4.3 **A front panel indicator** labeled "CONFLICT" shall be provided. The indicator shall illuminate when there is a FAILED state caused by conflicting channels and go off only by Unit Reset issuance.
- 4.4.4 **The output relay contact** for FAILED state shall be closed.
- 4.4.5 **A second output circuit** (STOPTIME controller input) shall be provided to sink an NPN open collector transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50 mA at up to 30 VDC. A blocking diode shall be provided on the transistor output to prevent it from sourcing power into the controller unit.
- 4.4.6 **An internal SPST logic toggle switch** shall be provided on the monitor unit to activate the WDT function. When the switch is ON, the WDT circuitry shall be active. The switch shall be mounted on the module PCB in a readily accessible location.
- 4.4.7 **The front panel reset switch** shall be tied to the external test reset input line (Pin Z). The external line shall be optically isolated from internal circuitry.
- 4.4.8 **The conflict monitor** shall reset after a power failure if the monitor was not in a FAILED state prior to the onset of the power failure.

SECTION 5 – MONITOR CONNECTOR PIN AND CHANNEL ASSIGNMENTS

- 4.5.1 **Model 208 connector wiring assignments**
See Table B-1

- 4.5.2 **Model 210 Connector wiring assignments**
See Table B-2

- 4.5.3 **Model 210 Program Card Assignments**
See Table B-3

CHAPTER 5

SPECIFICATIONS FOR DETECTOR SENSOR UNITS AND ISOLATORS

MODEL 222 TWO-CHANNEL LOOP DETECTOR SENSOR UNIT

MODEL 222T TIME DELAY TWO-CHANNEL LOOP DETECTOR SENSOR UNIT

MODEL 242 TWO-CHANNEL DC ISOLATOR

MODEL 252 TWO-CHANNEL AC ISOLATOR

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SECTION 1 – GENERAL REQUIREMENTS

- 5.1.1 **The sensor unit and isolator channels** shall operate independently from each other.
- 5.1.2 **Each sensor unit or AC isolator channel** shall draw no more than 100 mA from the +24 VDC cabinet power supply and shall be insensitive to 700 mV RMS ripple on the incoming +24 VDC line.
- 5.1.3 **The sensor unit or isolator front panel** shall be provided with a hand pull to facilitate insertion and removal from the input file.
- 5.1.4 **All control switches and channel indicators** shall be mounted on the front panel, with the exception of the 222T detector. Each sensor unit or isolator channel shall have an indicator to provide visual indication of detection or incoming signal. Presence indicators shall be wide-angle, high-brightness type LED's suitable for sunlight visibility.
- 5.1.5 **Each sensor unit or isolator channel output** shall be an optically isolated NPN open collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs.
- 5.1.6 **A valid channel input** shall cause a channel ground true output to the controller unit of a minimum 100 ms in duration. An onboard jumper shall be provided to bypass the above minimum timing requirement.
- 5.1.7 **The loop detector sensor unit** shall operate and interface successfully with an associated ODOT standard inductive loop.
- 5.1.8 **The output transistor** shall switch from the OFF state to the ON state in a period equal to (or less than) 20 μ S. The transistor shall switch from the ON state to the OFF state in a period equal to (or less than) 20 μ S.
- 5.1.9 **The numbered and lettered sides of the PCB connector** shall be commonly assigned.

SECTION 2 – MODEL 222 AND 222T LOOP DETECTOR UNIT REQUIREMENTS

- 5.2.1 **The sensor unit channel** shall produce an output signal when a vehicle passes over or remains over wire loops embedded in the roadway. The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease inductance of the circuit measured at the input terminals of the sensor unit.
- 5.2.2 **An open loop** shall cause the sensor unit channel to output a ground true signal.
- 5.2.3 **Each sensor unit channel** shall be capable of detecting all types of vehicles.
- 5.2.4 **The sensor unit** shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 20 to 2,000 μH with a Q-parameter as low as 5 at the sensor unit operating frequency.
- 5.2.5 **Loop inputs to each channel** shall be transformer isolated.
- 5.2.6 **Each individual channel** shall have a minimum of three switch-selectable operating frequencies.
- 5.2.7 **The sensor unit channel tuning circuits** shall be automatic and shall be so designed that drift, caused by environmental changes, or changes in applied power shall not cause an actuation. Manual tuning detector amplifiers will not be permitted.
- 5.2.8 **Mode Selection Requirements**
 - 5.2.8.1 Each sensor unit channel shall have Pulse and Presence selectable modes.
 - 5.2.8.1.1 Pulse Mode:
 - 5.2.8.1.1.1 In the Pulse mode, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 (± 25) ms in duration.
 - 5.2.8.1.1.2 Should a vehicle remain in a portion of the detection zone for a period in excess of 2 seconds, the sensor unit channel shall automatically “tune out” the presence of said vehicle. The sensor unit channel shall then be capable of detecting another vehicle entering the same detection zone. The recovery time between the first vehicle pulse and channel capability to detect another vehicle will be 3 seconds, maximum.

5.2.8.1.2 Presence Mode:

5.2.8.1.2.1 In the Presence mode, the sensor unit channel shall recover to normal sensitivity within 1 second after termination of vehicle presence in the detection zone regardless of the duration of the presence.

5.2.8.1.2.2 Channel sensitivity settings shall be provided that detect the presence of a vehicle in the detection zone for a specified time period and inductance change(s). The conditions are as follows:

<u>Minimum detection time duration in minutes</u>	<u>Detector input inductance change</u>
4	Equal to selected sensitivity
16	0.02% greater than selected sensitivity

5.2.9 **Sensitivity**

5.2.9.1 Each sensor unit channel shall be equipped with eight front panel selectable sensitivity settings in Presence and Pulse modes.

5.2.9.2 The sensor unit channel shall not detect vehicles, moving or stopped, at distances of 1 m or more from any loop perimeter.

5.2.9.3 All sensitivity settings shall not differ $\pm 40\%$ from the nominal value chosen.

5.2.10 **Response time of the sensor unit channel level 2 setting** shall be less than 20 ms. That is, for any decreased inductive change that exceeds its sensitivity threshold, the channel shall output a ground true logic level within 20 ms. When such change is removed, the output shall become an open circuit within 20 ms.

5.2.11 **The sensor unit channels** shall begin normal operation within 2 seconds after the application of power or after a reset signal of 15 μS .

5.2.12 **Lightning protection** shall be installed within the sensor unit.

5.2.12.1 The protection shall enable the sensor unit to withstand the discharge of a 10 μF capacitor charged to $\pm 1,000$ volts directly across the sensor unit input pins with no loop load present. The protection shall enable the sensor unit to withstand the discharge of a 10 μF capacitor charged to $\pm 2,000$ volts directly across either the sensor unit input inductance pins or from either side of the sensor unit input inductance pins to EG. The sensor unit input pins shall have a dummy resistive load attached that is equal to 5.0 ohms.

5.2.13 **Tracking Rate**

5.2.13.1 The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.

5.2.14 **Tracking Range**

5.2.14.1 The sensor unit shall be capable of normal operation as the input inductance is changed $\pm 5\%$ from the quiescent tuning point regardless of internal circuit drift.

5.2.14.2 The sensor unit shall be capable of normal operation as the input resistance is changed $+0.5\%$ from the quiescent tuning point regardless of internal circuit drift.

5.2.15 **Temperature Change**

5.2.15.1 The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes with the rate of temperature change not exceeding 1°C per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18°C between the inside and outside air shall not affect the proper operation of the sensor unit.

5.2.16 **A switch or switch position** shall be provided on the front panel to disable each channel output.

5.2.17 **The Model 222T** shall offer a selection of switch activated DELAY times from 0 to 31 seconds in 1-second increments. The detector indicator will flash at 4 Hz while the output is being delayed, subject to the status of the control input.

5.2.18 **The Model 222T** shall offer a selection of switch activated EXTENSION times from 0 to 7.5 seconds in 0.5-second increments. The detector indicator will flash at 12 to 16 Hz while the output is being extended, subject to the status of the control input.

5.2.19 **Each detector unit** shall sequentially scan (excite and measure) its channel inputs to eliminate cross talk (mutual interference/coupling) between closely spaced large loops in adjacent lanes and/or Lead-ins in common saw cuts and/or home runs in common conduits.

SECTION 3 – MODEL 242 TWO-CHANNEL DC ISOLATOR REQUIREMENTS

- 5.3.1 **The Model 242 Two-Channel DC Isolator** shall contain 2 isolation channels which provide isolation between electrical contacts external to the module and the controller unit input. The method of isolation shall be based upon a design that shall provide reliable operation.
- 5.3.2 **Each isolation channel** shall have a front panel-mounted test switch to simulate a valid input. The test switch shall be a single-pole, double-throw, 3-position control test switch: The position assignment shall be UP = constant ON; MIDDLE = OFF; and DOWN = momentary ON.
- 5.3.3 **The isolator** shall have an internal power supply that shall supply 20 (± 4) VDC to the field input side of the isolation channels. The isolator shall not draw more than 2.5 watts of AC power. No current shall be drawn from the cabinet power supply.
- 5.3.4 **A channel contact closure input of 5 ms (or less)** shall not cause an output (ground true) to the controller. An input of 25 ms (or greater) shall cause an output to the controller. An input of duration between 5 ms and 25 ms may or may not cause an output to the controller. The channel circuitry shall be able to react to a new input closure within 25 ms of an input opening.
- 5.3.5 **Each isolation channel field input** shall be turned ON (true) when a contact closure causes an input voltage of less than 8 VDC and shall be turned OFF (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA or more than 40 mA to an electrical contact closure or short from the power supply.
- 5.3.6 **The minimum isolation** shall be 1,000 megohms and 2,500 VDC measured between the input and output of the same channel.
- 5.3.7 **Lightning protection** shall be installed within the isolator unit.
- 5.3.7.1 **The protection** shall enable the isolator to withstand the discharge of a 10 μ F capacitor charged to $\pm 1,000$ volts directly across the input pins with no load present. The protection shall enable the isolator to withstand the discharge of a 10 μ F capacitor charged to $\pm 2,000$ volts directly across either the input pins or from either side of the input pins to EG. The input pins shall have a dummy resistive load attached that is equal to 5.0 ohms.

SECTION 4 – MODEL 252 TWO-CHANNEL AC ISOLATOR REQUIREMENTS

- 5.4.1 **The Model 252 Two-Channel AC Isolator** shall contain two isolation channels that provide isolation between external 120 VAC input circuits and the controller unit input circuits. The method of isolation shall be based upon a design that provides reliable operation.
- 5.4.2 **A channel input voltage** (V_{on}) of $>80 (\pm 5)$ VAC applied for a minimum duration of 100 ms shall cause an output (ground true) to the controller.
- 5.4.3 **A channel input voltage** (V_{on}) of <40 VAC applied for a minimum duration of 100 ms shall cause an output (false) to the controller.
- 5.4.4 **Switching circuitry** to invert inputs to read ground false logic (by switch jumper) shall be provided.
- 5.4.5 **The transistor** shall be capable of sinking 50 mA at 30 VDC.
- 5.4.6 **The minimum isolation** shall be 1,000 megohms between the input and output terminals at 2,500 VDC applied voltage.
- 5.4.7 **Lightning protection** shall be installed within the isolator unit.
 - 5.4.7.1 Each channel input shall withstand, without damage, the discharge of a 10 μ F capacitor charged to $\pm 1,000$ volts when connected directly to the open input pins. Each channel shall withstand, without damage, the discharge of a 10 μ F capacitor charged to $\pm 2,000$ volts when connected between either input pin or EG.

CHAPTER 6

SPECIFICATIONS FOR CABINET MODELS 332, 334 AND 340

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SECTION 1 – GENERAL REQUIREMENTS AND CABINET MODEL COMPOSITION

- 6.1.1 **Unless otherwise specified**, the model shall be furnished, ready for operation, with the following composition:
- 6.1.1.1 A Model 332 Cabinet shall consist of:
- | | |
|--------------------------------|--------------------------|
| Housing #1 | C1 Harness #1 |
| Mounting Cage #1 | C2 Harness |
| Power Distribution Assembly #2 | Service Panel #1 |
| Input Files I & J | Input Panel #1 |
| Output File #1 | Pull-Out Drawer Assembly |
- 6.1.1.2 A Model 334 Ramp Meter Cabinet shall consist of:
- | | |
|---------------------------------------|--------------------------|
| Housing #1 | C1 Harness #2 |
| Mounting Cage #1 | C2 Harness |
| Input File I | Service Panel #1 |
| Output/Power Distribution Assembly #3 | Input Panel #3 |
| | Pull-Out Drawer Assembly |
- 6.1.1.3 A Model 340 ITS Cabinet shall consist of:
- | | |
|--------------------------------|--------------------------|
| Housing #1 | Pull-Out Drawer Assembly |
| Mounting Cage #1 | Two Full Depth Shelves |
| Power Distribution Assembly #4 | Service Panel #1 |
- 6.1.1.4 The controller unit with Model 400 Modem shall be furnished with Model 332 and Model 334 cabinets. These cabinets shall have all input and output files installed and wired complete for 8-phase operation, or local ramp meter, respectively. However, only those input and output devices, such as detector sensor units, isolator units, and switch packs necessary to provide the operation required by the plans or specifications shall be furnished.
- 6.1.1.4.1 Model 332 and Model 334 cabinet wiring shall include a harness and C5 connector for an auxiliary output file. An auxiliary output file shall be supplied and installed in the cabinet when specified.
- 6.1.1.5 All assemblies and files included in Model 332 and Model 334 cabinets shall be mounted on the cage mounting rails per cabinet model detail. Cabinet model interface wiring shall be per specified C1 Harness, detailed wiring lists, and required cabinet wiring diagram.

6.1.2 **Cabinet Shipping Requirements**

6.1.2.1 The cabinet shall be delivered mounted on a plyboard shipping pallet. The pallet shall be bolted to the cabinet base. The housing doors shall be blocked to prevent movement during transportation.

6.1.3 **Cabinet Finish**

6.1.3.1 Inside and outside of walls, doors, and ceiling of the cabinet shall be anodized after fabrication.

6.1.3.2 All nuts, bolts, washers, screws [4 mm (or larger)], hinges, and hinge pins shall be stainless steel unless otherwise specified.

6.1.3.3 A cage mounting clear area for the controller unit shall be provided in Model 332 and Model 334 cabinets. The area shall extend 38 mm in front of and 406 mm behind the front EIA mounting angles. A minimum of 184 mm above the supporting portion of the angle shall be kept clear for the controller.

6.1.3.4 All conductors, terminals, and parts that could be hazardous to maintenance personnel shall be protected with suitable insulating material.

6.1.4 **Anchor Bolts**

6.1.4.1 The cabinet shall be furnished with anchor bolts of the size and grade recommended by the manufacturer.

SECTION 2 – HOUSING REQUIREMENTS

6.2.1 **The housing** shall be NEMA ICS-6 type 3R rated and shall include, but not be limited to the following:

Enclosure	Police Panel (Models 332 and 334 only)
Doors	Ventilation
Latches/Locks	Gaskets
Hinges and Door Catches	Cage Supports and Mounting
	Light Fixture

6.2.2 **Housing Construction**

6.2.2.1 The housing shall be rainproof with the top of the enclosure crowned to prevent standing water. It shall have single front and rear doors, each equipped with a lock.

6.2.2.2 The enclosure including doors, lifting eyes, gasket channels, police panel (where furnished) and all supports welded to the enclosure and doors shall be fabricated of 3.2 mm minimum thickness, aluminum sheet alloy 5052-H32 or 6061-T6. Bolted-on supports shall either be the same material and thickness as the enclosure or 2.7 mm minimum steel. The side panels and filter shell shall be fabricated of 2.0 mm minimum aluminum sheet.

6.2.2.3 All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filed to a radius of 0.8 mm, minimum. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders, and welding operators shall conform to the requirements and practices on AWS B3.0 and C5.6 for aluminum.

6.2.2.4 Aluminum surfaces shall conform to the following:

6.2.2.4.1 An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning procedure shall be to immerse in inhibited alkaline cleaner [Oakite 61A, Diversey 909 (or equivalent) in mix of 45 to 60 g per liter of distilled water] at 71°C for 5 minutes. Rinse in cold water. The etching procedure shall be to immerse in a sodium solution [3.7 g sodium fluoride plus 37.5 g sodium hydroxide mix per liter of distilled water] at 66°C for 5 minutes. Rinse in cold water. Desmut in a 50% by volume nitric acid solution at 20°C for 2 minutes. Rinse in cold water.

6.2.2.4.2 The anodic coating shall conform to MIL-A-8625C (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, Class I Coating except the outer housing surface coating shall have a 0.018 mm minimum thickness and a 20 mg per 500 mm² minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution (pH 5.0 to 6.5) of nickel acetate at 99°C for 15 minutes.

- 6.2.2.5 The enclosure doorframes shall be double flanged out on all four sides and shall have strikers to hold tension on and form a firm seal between the door gasket and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 4 (± 2) mm.
- 6.2.2.6 Gaskets shall be provided on all door openings and shall be dust-tight. Gaskets shall be 6 mm minimum thickness, closed cell neoprene or silicone [BOYD R-10480 (or equal)] and shall be permanently bonded to the metal. If neoprene is used, the mating surface of the gasket shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A gasket top channel shall be provided to support the top gasket on the door (prevents gasket gravitational fatigue).
- 6.2.2.7 Cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness of either 4.8 mm aluminum or 2.7 mm steel.
- 6.2.2.8 The housing shall be provided with two lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 20 mm. Each eye shall be able to support a weight load of 450 kg.
- 6.2.2.9 All exterior bolt heads shall be tamperproof type.

6.2.3 **Door Latches and Locks**

- 6.2.3.1 The latching handles shall have provision for padlocking in the closed position. Each handle shall be 20 mm minimum diameter stainless steel with a minimum 13 mm shank. The padlocking attachment shall be placed at 100 mm from the handle shank center to clear the lock and key. An additional 100 mm minimum gripping length shall be provided.
- 6.2.3.2 The latching mechanism shall be a 3-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 6 mm thick by 20 mm wide, minimum.
- 6.2.3.3 When the door is closed and latched, the door shall be locked. The locks and handles shall be on the right side of the front door and left side of the rear door. The lock support shall be rigidly mounted on the door. In the locked position, the bolt throw shall extend a minimum of 6 (± 0.8) mm into the latch cam area. A seal shall be provided to prevent dust or water entry through the lock opening.
- 6.2.3.4 The locks shall be a Best Company 5L7RD Series (or an approved equal) with a red construction core in Model 332 and Model 334 Cabinets and a white construction core in Model 340 Cabinets. Two keys shall be supplied with each cabinet. The keys shall be removable in the locked position only.
- 6.2.3.5 The center latch cam shall be fabricated of 4.7 mm minimum thickness steel or aluminum. The bolt surface shall horizontally cover the cam thickness. The cam

shall be structured to only allow the door to open when the handle is moved toward the center of the door.

6.2.3.6 Rollers shall have a 22 mm minimum diameter, with Nylon wheels and steel ball bearings.

6.2.4 **The general requirements for housing ventilation** including intake, exhaust, filtration, fan assembly, and environmental control, as follows:

6.2.4.1 The front door shall be provided with louvered vents. The louvered vent depth shall be a maximum of 6 mm. A removable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter, providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 6 mm to house the filter. The filter and shell shall be held firmly in place with a bottom bracket and a spring-loaded upper clamp. No incoming air shall bypass the filter. The bottom filter bracket shall be formed to create a waterproof sump with drain holes to the outside housing.

6.2.4.1.1 The filter shall be 305 mm high by 406 mm wide by 22 mm thick. The filter shall trap particles 2 microns and larger.

6.2.4.2 The intake (including filter with shell) and exhaust areas shall pass a minimum of 1.7 m³ of air per minute.

6.2.4.3 The housing shall be equipped with an electric fan with ball or roller bearings and a capacity of at least 2.8 m³ of free air delivery per minute. The fan shall be mounted within the housing and vented.

6.2.4.4 The fan shall be thermostatically controlled and shall be manually adjustable to turn on between 33°C and 65°C with a differential of not more than 6°C between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor ampacity. The manual adjustment shall be graded in 10°C increments.

6.2.5 **Hinges and Door Catches**

6.2.5.1 Hinges with two bolts per leaf shall be provided to bolt the door to the enclosure. Each door shall have four stainless steel hinges. Each hinge shall be 90 mm minimum length and have a fixed pin. The pin ends shall be welded to the hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

6.2.5.2 Front and rear doors shall be provided with catches to hold the door open at both 90° and 180° (±10°). The catch minimum diameter shall be either 9.5 mm for plated steel or aluminum rods, or 6 mm for stainless steel. The catches shall be capable of holding the door open at 90° in a 95 km/hr wind, acting at an angle perpendicular to the plane of the door.

6.2.6 **Police Panel** (Model 332 and Model 334 Cabinet)

6.2.6.1 A police panel assembly shall be provided to allow limited access to intersection control by police officers. The police panel assembly, including switches, shall not extend into the cabinet more than 38 mm.

6.2.6.2 The police panel door shall be equipped with a lock. The lock shall be keyed with a master police key. Two keys shall be furnished with each police lock. Each police key shall have a shaft at least 44 mm in length.

6.2.6.3 The police panel shall contain two DPST toggle power switches.

6.2.6.3.1 The Model 332 shall have one switch labeled "ON-OFF" and the other "FLASH/AUTOMATIC".

6.2.6.3.2 The Model 334 shall have one switch labeled "ON-OFF LIGHTS" and the other "POLICE CONTROL ON-OFF".

6.2.6.4 The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

6.2.6.5 The panel assembly shall have a drain to prevent water collecting within the assembly. The drain shall be channeled to the outside.

6.2.7 **Cabinet Light Fixture**

6.2.7.1 A 15 watt, self-starting, fluorescent cabinet light shall be installed in each controller cabinet (see Cabinet Details Drawings). The fixture shall be mounted to the cabinet exhaust area cover plate by screw and self-locking nut. The mounting hardware shall not penetrate the exterior of the cabinet shell. The fixture and fluorescent tube shall not interfere with access to any cabinet component or TBK. The fixture will be controlled from a door-operated switch located at the rear door. The fixture power shall be switched "ON" when the rear door is opened. In addition to the rear door switch, the fixture circuit shall incorporate an accessible power "ON-OFF" switch. Power for the light fixture shall be supplied from the load side of the 15 amp Equipment breaker of the PDA through an "in-line" type fuse holder (1 amp fuse) through the normally closed cabinet rear door switch to the light fixture (see Equipment Mounting Drawing).

SECTION 3 – CABINET CAGE REQUIREMENTS

- 6.3.1 **A standard EIA 483 mm rack cage** shall be installed inside the housing for mounting of the controller unit and cabinet assemblies.
- 6.3.2 **The EIA rack portion of the cage** shall consist of two pairs of continuous, adjustable equipment mounting angles. The angle nominal thickness shall be 3.4 mm plated steel, 2.7 mm stainless steel, or 3.9 mm aluminum. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angle shall comply with Standard EIA-310-B and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.
- 6.3.3 **Clearance** between rails for mounting assemblies shall be 450 mm.
- 6.3.4 **Two steel supporting angles** extending from the front to the back rails shall be supplied with Model 332 or Model 334 cabinets to support the controller unit. The angles shall be designed to support a minimum of 23 kg each. The horizontal side of each angle shall be a minimum of 75 mm. The angles shall be vertically adjustable.
- 6.3.5 **The cage** shall be bolted to the cabinet at eight points, via the housing cage supports and associated spacer brackets - four at the top and four at the bottom of the rails.
- 6.3.6 **The cage** shall be centered within the cabinet.

SECTION 4 – CABINET ASSEMBLIES REQUIREMENTS

6.4.1 General Requirements

6.4.1.1 The following equipment shall be completely removable from the cabinet without removing any other equipment and using only a slotted or Phillips screwdriver:

- Power Distribution Assembly
- Input File (Model 332 and Model 334 cabinets)
- Output File (Model 332 cabinet)
- Auxiliary Output File (Model 332 and Model 334 cabinets)
- Pull-Out Drawer Assembly

6.4.1.2 All fuses, circuit breakers, switches (except police panel switches, fan fuse and cabinet light fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

6.4.1.3 All equipment in the cabinet, when required, shall be permanently and clearly labeled. The marker strips shall be made of material that can be easily and legibly written upon using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with all items installed.

6.4.1.4 Assemblies and files shall be fabricated of 1.5 mm minimum thickness aluminum or stainless steel sheet. The metal surface shall be treated with clear chromate.

6.4.1.4.1 Additional requirements for Model 332 and Model 334 Cabinets:

6.4.1.4.1.1 Resistor-capacitor transient suppression shall be provided at all AC relay sockets (across relay coil) except for the flash transfer relays (FTR) in the output files, where one suppression device may be common for all.

6.4.1.4.1.2 A leakage resistor which permits a small amount of current to pass through the heavy duty relay coil, shall be installed across the terminals of relay sockets to overcome the residual magnetism.

6.4.1.4.1.3 Assembly or file depth dimension shall include TBKs.

6.4.1.4.1.4 All assemblies and files (except pullout drawer assembly) shall allow air circulation through the top and bottom unless specifically called out otherwise.

6.4.1.4.1.5 Socket types for the following equipment shall be:

Switch Pack	BEAU S-5412-XX (or equal)
Heavy Duty Relay	BEAU S-5408-XX (or equal)
Flasher Unit & Power Supply Module	BEAU S-5406-XX (or equal)
210 Monitor Unit	PCB 28/56S

6.4.1.4.1.6 Connector sockets for flasher unit, power supply, and switch pack modules shall be mounted with their front face 190 mm deep from assembly or file front panel (note output file exception).

6.4.1.4.1.7 Guides (top and bottom) shall be provided for switch pack modules, flasher units, monitor unit, WDT module, detector and isolator modules, and power supply module (bottom only). The guides shall begin 25 (± 13) mm from the front panel surface and extend to within 13 mm of the connector socket face.

6.4.2 **Power Distribution Assembly**

6.4.2.1 The following equipment shall be provided with the power distribution assemblies:

6.4.2.1.1 PDA #2:

- 1– Duplex NEMA 5-15R Controller Receptacle
- 2– Duplex NEMA 5-15R Equipment Receptacle
- 1 – 1 Pole, 50 amp, 120 VAC Main Circuit Breaker
- 1 – 1-Pole, 15 amp, 120 VAC Equipment Circuit Breaker
- 6 – 1 Pole, 15 amp, 120 VAC Signal Bus and Illuminated Sign Circuit Breaker
- 1 – 2 Pole Ganged, 20 amp, 120 VAC Flash Bus Circuit Breaker
- 1 – Mercury Contactor, 60 amp, 120 VAC
- 2 – Model 204 Flasher Unit and Socket
- 1 – Model 206 Power Supply Module and Socket
- 1 – AUTO/FLASH Control Switch
- 1 – FLASH On Indicator Light
- 3 – 10 Position TBK T1, T2 & T4
- 1 – 4 Position TBK T3

6.4.2.1.2 Output/PDA #3:

- 1– Duplex NEMA 5-15R Controller Receptacle
- 2– Duplex NEMA 5-15R Equipment Receptacle
- 1 – 1 Pole, 30 amp, 120 VAC Main Circuit Breaker
- 3 – 1 Pole, 15 amp, 120 VAC Circuit Breaker (Equip & Field)
- 1 – Model 206 Power Supply Module and Socket
- 1 – Model 208 Monitor Unit and Socket
- 1 – Model 430 Heavy Duty Relay and Socket (Transfer Relay)
- 1 – Watchdog Timer ON/OFF-RESET Control Switch
- 3 – Model 200 Switchpack Socket
- 3 – 10 Position TBK T1, T2, and T4
- 1 – 4 Position TBK T3

6.4.2.1.3 PDA #4:

- 2 - Duplex NEMA 5-15R GFCI Receptacles
- 4 - Duplex NEMA 5-15R Equipment Receptacles
- 1 - 1 Pole, 50 amp, 120 VAC Main Circuit Breaker
- 2 - 1 Pole, 15 amp, 120 VAC Equipment Circuit Breakers
- 1 - 1 Pole, 15 amp, 120 VAC GFI Receptacle Breaker
- 1 - 1 Pole 15 amp, 120 VAC Cabinet Accessory Breaker (Fan and Light)
- 1 - 1 Pole, 15 amp, 120 VAC Spare Breaker

6.4.2.2 Breaker ratings shall be shown on face of breaker or handle. Breaker function shall be labeled below breaker on front panel.

6.4.2.3 The equipment receptacles shall have ground-fault circuit interruption as defined in the National Electrical Code.

6.4.2.4 All conductors from the power distribution assembly routed to the cabinet wiring shall be connected to the TBK on the common side, except for the AC power conductor between the service TBK and main circuit breaker. All internal conductors terminating at the blocks shall be connected to the other side of the blocks.

6.4.2.5 Additional requirements for Model 332 and Model 334 Cabinets:

6.4.2.5.1 The AUTO/FLASH switch, when placed in FLASH position (down), shall energize the Mercury Contactor (MC) coil. When the switch is placed in the AUTO position (up), the switch packs shall control the signal indications. The switch shall be a SPST toggle control switch.

6.4.2.5.2 The FLASH indicator light labeled "FLASH ON" shall be mounted on the PDA front panel. The lamp shall be driven as specified in Section 6.4.2.5.6.2.

6.4.2.5.3 Ganged circuit breakers shall be certified by the circuit breaker manufacturer that their circuit breakers shall gang trip.

6.4.2.5.4 Illuminated Sign Circuit Breaker - A 15 amp, 120 volt, AC circuit breaker shall be installed for illuminated sign circuit protection. The breaker shall be placed on the load side of the main breaker. The breaker shall be located on the front panel of the PDA assembly next to the other breakers.

6.4.2.5.5 The monitor unit ON/OFF-RESET switch shall be a DPST toggle control mounted on the PDA #3 front panel. When placed in the OFF-RESET (down) position, a grounded input shall be presented at the monitor unit Pin 21 (resetting the WDT circuitry). The other side of the switch circuit bypasses the monitor unit.

6.4.2.5.6 Signal Bus Circuit Breakers:

6.4.2.5.6.1 Five, single-pole, 15 amp circuit breakers with auxiliary switch feature and medium trip delay characteristic shall be provided.

6.4.2.5.6.2 The five breakers shall be wired and routed per the Circuit Breaker Line Diagram. The breaker auxiliary switch circuit shall be open when the breaker is in the ON position. The auxiliary circuits shall be wired in parallel so that any tripped breaker shall energize the mercury contactor coil, flash transfer relay coils, and the FLASH ON indicator (Section 6.4.2.5.2). The auxiliary contacts shall be rated at 5 amps, 120 VAC, minimum (fast-on type connection).

6.4.2.5.7 Model 206 Power Supply Module:

6.4.2.5.7.1 A power supply shall be provided to supply +24 VDC to the input and output files for use by their associated devices. The front panel shall include AC and DC fuses, POWER ON light, and test points for monitoring the output voltages. The power supply shall be of ferro-resonant design having no active components and will conform to the following requirements:

1. Line Regulation: 2% from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1% frequency change
2. Load Regulation: 5% from 1 amp to 5 amps with a maximum temperature rise of 30°C above ambient
3. Design Voltage: +24 (± 0.5) VDC at full load, 30°C, 115 VAC incoming after a 30-minute warm-up period
4. Full Load Current: 5 amps, minimum
5. Ripple Noise: 2 volts peak-to-peak and 500 mV RMS at full load
6. Line Voltage: 90 to 135 VAC
7. Efficiency: 70% minimum
8. Minimum Voltage: +22.8 VDC
9. Circuit capacitors shall be rated for 40 volts, minimum.

6.4.2.5.7.2 The module chassis shall be vented. Its top and side shall be open except for unit supports.

6.4.2.5.7.3 When resident in the PDA assembly, the module shall be held firmly in place by its stud screw, assembly connector support panel, and a wingnut.

6.4.2.5.7.4 Two 0.5 ohm, 10 watt minimum, wire-wound power resistors with a 0.2 μ H inductance shall be provided; one on the AC+ power line and one on the AC- line. Three MOV surge arrestors rated for 20 Joules minimum, shall be provided between AC+ and EG, AC- and EG, and between AC+ and AC-. A 0.68 μ F capacitor shall be placed across AC+ and AC- between the 2 power resistors and the MOV's.

6.4.2.5.7.5 Terminal screw size shall be 10-32 for TBK T1, T2, & T4 and 6-32 for TBK T3.

6.4.3 **Input File** (Model 332 and Model 334 Cabinets)

6.4.3.1 The file shall have a maximum depth of 215 mm and shall intermate with and support 14, 2-channel detector or isolator units.

6.4.3.2 The file shall provide a PCB 22/44S connector which shall be a DALE EB7CS22GY (or equal) and shall be centered vertically for each 2-channel detector. The associated number and letter side connectors shall be shorted internally. Pins D, E, F, J, K L, and W shall be brought out to an 8-position TBK on the back of the file. The output emitters shall be common grounded with the ground terminating at TB 15, position 4. Position 8 of the TBK is assigned to EG and is used to terminate lead-in shields.

6.4.3.3 The input file shall be provided with marker strips to identify isolators and detectors in the file.

6.4.3.4 TBK terminal screw size shall be 8-32.

6.4.4 **Output File** (Model 332 and Model 334 Cabinets)

6.4.4.1 General Requirements:

6.4.4.1.1 The output file shall be provided with marker strips to identify switch packs when mounted in the file.

6.4.4.1.2 Switch pack connectors, monitor unit connectors, flash transfer relay sockets, and flash programming connectors shall be accessible from the back of the output file without the use of tools or removal of any other equipment.

6.4.4.1.3 TBK 01 and 03 terminal positions shall be labeled functionally. Terminal screw size shall be 8-32.

6.4.4.1.4 Field wire TBKs shall be mounted vertically on the back of the assembly. The output file shall have three TBKs with 12 positions. Terminal position screw size shall be 10-32.

6.4.4.1.5 The depth of the file shall not exceed 368 mm.

6.4.4.1.6 The flash programming connectors shall be Molex Type 1375 (or equal). The receptacle shall be mounted on the file with a programmable plug connected. The plug connector, with programming jumpers, shall be furnished for each circuit to allow red or yellow flash programming. Plug pins shall be crimped and soldered.

6.4.4.1.7 TBK 02 and 04 terminal screw size shall be 6-32.

- 6.4.4.1.8 Output file connectors and sockets shall be hard wired and PCBs will not be allowed.
- 6.4.4.2 Output File #1:
 - 6.4.4.2.1 The output file shall be capable of containing 12 Model 200 switch packs, four Model 430 flash transfer relays, and the Model 210 monitor unit. A monitor unit shall be furnished with each output file. The construction plans shall determine the number of flash transfer relays and switch packs that will be furnished with the output file.
 - 6.4.4.2.2 The red and yellow output circuits of switch packs 1, 2, 4, 5, 7, 8, 10, and 11 shall be made available at a Molex receptacle/plug connection for flash selectability.
 - 6.4.4.2.3 It shall be possible to remove the Model 210 monitor unit without causing the intersection to go into flashing operation. The cabinet shall be wired so that, with the front cabinet door closed and with the monitor unit removed, the intersection shall go into flashing operation (see One Line Diagram). The cabinet shall contain a conspicuous warning against operation with the monitor unit removed.
 - 6.4.4.2.4 The monitor unit compartment including the housed monitor unit, exclusive of the handle, shall extend no farther than 32 mm in front of the rack front surface. The switch pack socket connector front surface shall be no more than 216 mm in depth from the front surface of the output file.
- 6.4.4.3 Auxiliary Output File (Model 420):
 - 6.4.4.3.1 The auxiliary output file shall be capable of containing six Model 200 switch packs and two Model 430 flash transfer relays. The construction plans shall determine the number of flash transfer relays and switch packs that will be furnished with the auxiliary output file.
 - 6.4.4.3.2 The red and yellow output circuits of switch packs A1, A2, A4, and A5 shall be made available at a Molex receptacle/plug connection for flash selectability.
- 6.4.5 **Side Panels** (Model 332 and Model 334 Cabinets)
 - 6.4.5.1 Two panels shall be provided and mounted on the cage parallel to the cabinet sides. In viewing from the back door, the left side panel shall be designated as the "Input Panel" and the right side panel shall be designated as the "Service Panel".
 - 6.4.5.2 Terminal blocks shall be mounted on the panel and wired to the designated terminations as per applicable cabinet diagrams. The use of raceways shall not be permitted. Terminal blocks and terminals shall be identified as shown on the cabinet wiring diagram. Input panel TBK screw size shall be 8-32.

6.4.6 **Cabinet Harnesses** (Model 332 and Model 334 Cabinets)

6.4.6.1 The C1 harness shall be a minimum of 1.2 m in length. The harness wire bundle shall be provided with external protection and routed on the input panel side of the cabinet. Adequate length shall be provided to allow the C1P connector to properly connect any STATE approved controller unit mounted in the cabinet.

6.4.6.2 One end of the C1 harness shall be the C1P connector with pin contacts wired per the detail assignment. The other ends of the harnesses shall terminate as follows:

- Harness #1 - C4S connector (connected to C4P on output file)
C5S connector (connected to C5P on either the input panel or auxiliary output file)
Assigned input files I & J positions and logic ground bus
- Harness #2 - C5S connector (same as harness #1)
C6S connector (connected to C6P on output/PDA assembly)
Assigned input file positions and logic ground bus

6.4.6.3 Conductors between the C1 connector and the input file(s) shall be of adequate length to allow any conductor to be connected to any detector output terminal (positions S, F, or W).

6.4.7 **Pullout Drawer Assembly**

6.4.7.1 Pullout Drawer/Cabinet Print Holder: A pullout drawer shall be installed in the cabinet cage (see Equipment Mounting Drawing).

6.4.7.2 The drawer shall be 430 mm long by 430 mm wide by 44 mm deep. It shall have a hinged top that covers the storage box area and also provides a smooth surface to write on.

6.4.7.3 The drawer shall be General Devices D4080-19W (or equal).

SECTION 5 – CABINET WIRING REQUIREMENTS

6.5.1 Cabinet Wiring Diagram

6.5.1.1 The cabinet wiring diagram for Models 332 or 334 cabinets shall be furnished on current ODOT drawings for the appropriate cabinet model. One full-sized reproducible master copy of the drawing will be furnished, upon request. The drawings are available from the Traffic Signal Services Unit manager. A cabinet wiring diagram for Model 340 cabinet shall be furnished.

6.5.1.2 The Contractor shall add to the drawing all information and details required giving an accurate description of the wiring and operation of each individual cabinet. For Model 332 and Model 334 Cabinets, the information required includes the following:

1. Software program number and C1 connector pin program assigned functions
2. Input panel phase and loop number references
3. Input and output file phase references
4. Location and phase reference for all input/output devices furnished
5. Modifications made to standard cabinet wiring
6. Intersection layout
7. Phase sequence diagram
8. Preemption sequence diagram (if applicable).

6.5.1.2.1 For Model 332 and Model 334 Cabinets, the intersection layout shall include all vehicle signals, pedestrian signals, vehicle detectors, push buttons, lane usage arrows, and special devices located and identified as shown on the plans. A north arrow shall also be included and the intersecting streets shall be identified.

6.5.1.2.2 For Model 332 and Model 334 Cabinets, the phase and preemption sequence diagrams shall refer to the phase designations and sequence shown on the plans for both normal phase rotation and preemption.

6.5.1.3 Four OZALID-type (or equivalent) copies of the wiring diagram shall be furnished with each Model 332 or Model 334 controller cabinet. The copies shall not be reduced in size.

6.5.2 Conductors (Model 332 and Model 334 Cabinets)

6.5.2.1 All conductors used in cabinet wiring shall terminate with properly sized, insulated, spring spade type terminals except when soldered to a through-panel solder lug on the rear side of the TBK or as specified otherwise. All spade connectors on wires connecting the input panel to the input files shall be crimped and soldered to the wires.

6.5.2.1.1 All crimp-style connectors shall be applied with a tool that prevents opening of the handles until the crimp cycle is completed.

- 6.5.2.1.2 All conductor sizes shown are AWG.
- 6.5.2.2 Conductors between the service terminal AC- and EG and their associated bus, the EG bus conductor to power distribution assembly and cage rail, and the AC- bus to power distribution assembly shall be No. 8 (or larger).
- 6.5.2.3 All conductors, unless otherwise specified, shall be stranded No. 22 (or larger). Conductors shall be rated for 600 volts and shall conform to IMSA Specification 50-2 (or better). The insulation shall have a minimum thickness of 10 mils and shall be Nylon-jacketed polyvinyl chloride, except that conductors No. 14 and larger may have Type THHN/THWN insulation.
- 6.5.2.4 All conductors, except those that can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.
- 6.5.2.5 All conductors shall conform to the following color-code requirements:
1. The grounded conductors of AC circuits shall be identified by a continuous white or gray color.
 2. The equipment-grounding conductors shall be identified by a solid green color or by a continuous green color with one or more yellow stripes.
 3. The DC logic ground conductors shall be identified by a solid white color with a red stripe.
 4. The ungrounded conductors shall be identified by any color not specified in 1, 2, or 3 above.
- 6.5.2.6 All wiring harnesses shall be neat, firm, and routed to minimize crosstalk and electrical interference.
- 6.5.2.6.1 Wiring containing AC shall be routed and bundled separately or shielded separately from all logic voltage control circuits.
- 6.5.2.6.2 Cabling and wiring shall be routed to prevent conductors from being in contact with metal edges. Cabling and wiring shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.
- 6.5.2.7 Within the cabinet, the DC logic ground and EG shall be electrically isolated from the AC grounded conductor and each other by 500 megohms when tested at 500 VAC, with the power line surge protector disconnected.
- 6.5.2.8 The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 6 mm shall be used for securing the bus to the service panel.
- 6.5.2.9 The cabinet power supply DC ground shall be connected to the DC logic ground bus using a No. 14 (or larger) stranded copper wire.

6.5.2.10 Each detector lead-in pair for input panels #1 and #3, from the field terminals to the input file terminals, shall be a cable of IMSA type 50-2 (or better). The stranded, tinned, copper drain wire shall be connected to the "L" terminal on the input file TBKs. This input terminal shall be connected to the equipment grounding bus through a single conductor. Each connection shall be made by using a crimp connector that is soldered after the connector is crimped to the wire. These cables shall be heat shrunk protected - both the drain wire and the foil shield, to prevent shorting against the contacts on the back of the input file.

6.5.3 **Conductors** (Model 340 Cabinet)

6.5.3.1 All conductors used in cabinet wiring shall terminate with properly sized, insulated, spring spade type terminals. All spade connectors on wires shall be crimped. Sensor and device wiring shall be terminated per manufacturer's instructions. In the absence of manufacturer termination instructions, the sensor and device wiring shall be terminated with a spade connector that has been crimped and soldered to the wire.

6.5.3.2 All crimp style connectors shall be applied with a tool that prevents openings of the handles until the crimp cycle is completed.

6.5.3.3 All conductors shall conform to the following color code requirements:

1. The grounded conductors of AC circuits shall be identified by a continuous white or gray color.
2. The equipment-grounding conductors shall be identified by a solid green color or by a continuous green color with one or more yellow stripes.
3. The ungrounded conductors shall be identified by any color not specified in 1 or 2 above.

6.5.3.4 Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

6.5.3.5 The AC copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 6 mm shall be used for securing the bus to the service panel. Maintenance personnel shall protect the bus from accidental contact.

6.5.4 **Terminal Blocks** (Model 332 and Model 334 Cabinets)

6.5.4.1 The TBKs shall be barrier type, rated at 20 amps, 600 volts RMS, minimum. The terminal screws shall be 7.9 mm minimum length, nickel-plated, brass binder head type with screw inserts of the same material. Screw size is called out under associated cabinet assembly, file or side panel.

- 6.5.4.2 The terminals of the power line service TBK shall be labeled “L1”, “AC-“, and “EG” and shall be covered with a clear insulating material to prevent inadvertent contact. Terminating lugs large enough to accommodate No. 2 conductors shall be furnished for the service TBK. The TBK shall be rated for 50 amps at 600 volts peak, minimum. The block shall be either a double row, three position screw/insert with shorting bar (screws, inserts, and shorting bars shall be nickel plated brass) or a Marathon #1423552 (or equal). If the Marathon block is used, the surge protectors shall be terminated under a screw head (not common with AC+, AC-, or EG service conductors). The AC+, AC-, and EG conductors connecting to the service terminals and appropriate busses shall not be spade lugged.
- 6.5.5 **Terminal Blocks** (Model 340 Cabinet)
- 6.5.5.1 All terminal blocks shall comply with UL 1059 or NEMA ICS 4.
- 6.5.5.2 For No. 10 AWG conductors or smaller, one-piece double terminal, barrier type with binder screw terminals shall be used. Terminal ampacities shall be equal or greater than conductor ampacities.
- 6.5.5.3 For No. 8 AWG conductors or larger, use either one-piece or factory-assembled sectional barrier type with box-lug terminals having a pressure plate between screw and conductor. Use terminals of correct size for the conductors to be connected.
- 6.5.6 **Detector Test Buttons** (Model 332 and Model 334 Cabinets)
- 6.5.6.1 A detector test panel containing 12 normally open pushbuttons shall be furnished and installed on the inside front cabinet door or across the top front of the rack assembly. All pushbuttons shall be wired directly to the back of the input file.
- 6.5.6.1.1 There shall be a pushbutton for one detector input in a Model 332 Cabinet associated with each of the eight vehicle (count and extend) and four pedestrian phases, whether or not such phases are used at a particular location.
- 6.5.6.1.2 There shall be a pushbutton in a Model 334 Cabinet for one detector input associated with the following C1 inputs: 39, 44, 45, 47, 48, 50, 52, 56, 57, 59, 61, and 81.
- 6.5.6.2 The panel shall have a connector for disconnecting all panel wiring from the input file.
- 6.5.6.3 All pushbuttons shall be labeled by function. Pushbuttons in a Model 332 Cabinet shall also be labeled by phase

SECTION 6 – CABINET TRANSIENT SURGE SUPPRESSION REQUIREMENTS

6.6.1 Power Line

6.6.1.1 The power line surge protector shall be metal oxide varistor (MOV). One shall be installed between AC+ and EG and the other between AC- and EG. The MOV shall have the following ratings:

Recurrent peak voltage:	212 volts
Energy rating:	50 Joules, maximum
Power dissipation:	0.85 watt, average
Peak current for pulses:	2,000 amps for less than 6 μ S
Standby current:	Less than 1 mA

6.6.2 Modem Interconnect Lines (Model 332 and Model 334 Cabinets)

6.6.2.1 General Requirements:

Shall be installed in all cabinets
Shall suppress bipolar and bi-directional transients
Shall fail in the open circuit configuration
Shall be of solid state design and contain no spark gap or gas tube
Leakage current to ground, maximum: 0.2 mA
Circuit impedance loading: $<25\Omega$

6.6.2.2 TVSS Performance:

1. Rated single transient energy: 75
(10 x 100 μ S, Joules)
2. Single pulse transient current: 2,000
(8 x 20 μ S, amps peak)
3. Maximum clamping voltage: 36
(1 kV, 200 A 8 x 50 μ S, V peak)

6.6.2.3 Physical Characteristics:

1. Operating temperature: -34°C to 74°C
2. Dimensions, maximum: L 125 mm x W 100 mm x D 50 mm

6.6.3 Telephone Line Protection (Model 340 Cabinet)

Protection Modes	Line-to-Line (L-L) and Line-to-Ground (L-G) Mode
Dynamic Response Time	1 nanosecond (maximum)
Max. Peak Signal Voltage	24
Nominal Breakdown Voltage	30
Max. Current (I _p 10x1000 μ S)	71 amps
Max. Clamp Voltage @ I _p	38
Capacitance	<1400 pf
Max. Continuous Current	150 mA
Nominal Series Resistance	8 ohms

CHAPTER 7

SPECIFICATIONS FOR CABINET MODELS 336, 336S AND 344

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SECTION 1 – GENERAL REQUIREMENTS AND CABINET MODEL COMPOSITION

- 7.1.1 **Unless otherwise specified**, the model shall be furnished, ready for operation, with the following composition:
- 7.1.1.1 A Model 336 or 336S Intersection Cabinet shall consist of:
- | | |
|-------------------------------------|--------------------------|
| Housing #2 (336) or #3 (336S) | C1 Harness #3 |
| Mounting Cage #2 (336) or #3 (336S) | C2 Harness |
| Power Distribution Assembly #2 | Service Panel #2 |
| Input File | Input Panel #2 |
| Output File #1 | Pull-Out Drawer Assembly |
- 7.1.1.2 A Model 336 or 336S Ramp Meter Cabinet (panel termination) shall consist of:
- | | |
|-------------------------------------|--------------------------|
| Housing #2 (336) or #3 (336S) | C1 Harness #2 |
| Mounting Cage #2 (336) or #3 (336S) | C2 Harness |
| Power Distribution Assembly #3 | Service Panel #2 |
| Input File | Input Panel #3 |
| | Pull-Out Drawer Assembly |
- 7.1.1.3 A Model 344 ITS Cabinet shall consist of:
- | | |
|--------------------------------|--------------------------|
| Housing #3 | Pull-Out Drawer Assembly |
| Mounting Cage #3 | 1-Full Depth Shelf |
| Power Distribution Assembly #5 | Service Panel #1 |
- 7.1.1.4 The controller unit with Model 400 Modem shall be furnished with Model 336 and Model 336S cabinets. These cabinets shall have all input and output files installed and wired complete for 8-phase operation. However, only those input and output devices, such as detector sensor units, isolator units, and switch packs necessary to provide the operation required by the plans or specifications shall be furnished.
- 7.1.1.5 All assemblies and files included in Model 336 and Model 336S cabinets shall be mounted on the cage mounting rails per cabinet model detail. Cabinet model interface wiring shall be per specified C1 Harness, detailed wiring lists, and required cabinet wiring diagram.
- 7.1.2 **Cabinet Shipping Requirements**
- 7.1.2.1 The cabinet shall be delivered mounted on a plyboard shipping pallet. The pallet shall be bolted to the cabinet base. The housing doors shall be blocked to prevent movement during transportation.

7.1.3 **Cabinet Finish**

- 7.1.3.1 Inside and outside of walls, doors, and ceiling of the cabinet shall be anodized after fabrication.
- 7.1.3.2 All nuts, bolts, washers, screws [4 mm (or larger)], hinges, and hinge pins shall be stainless steel unless otherwise specified.
- 7.1.3.3 A cage mounting clear area for the controller unit shall be provided in Model 336 and Model 336S cabinets. The area shall extend 38 mm in front of and 406 mm behind the front EIA mounting angles. A minimum of 184 mm above the supporting portion of the angle shall be kept clear for the controller.
- 7.1.3.4 All conductors, terminals, and parts that could be hazardous to maintenance personnel shall be protected with suitable insulating material.

7.1.4 **Anchor Bolts**

- 7.1.4.1 The cabinet shall be furnished with anchor bolts of the size and grade recommended by the manufacturer.

SECTION 2 – HOUSING REQUIREMENTS

7.2.1 **The housing** shall include, but not be limited to the following:

Enclosure	Police Panel (Models 336 and 336S only)
Doors	Ventilation
Latches/Locks	Gaskets
Hinges and Door Catches	Cage Supports and Mounting
	Light Fixture

7.2.2 **Housing Construction**

7.2.2.1 The housing shall be rainproof with the top of the enclosure crowned to prevent standing water. It shall have single front and rear doors, each equipped with a lock.

7.2.2.2 The enclosure including doors, lifting eyes, gasket channels, police panel (where furnished) and all supports welded to the enclosure and doors shall be fabricated of 3.2 mm minimum thickness, aluminum sheet alloy 5052-H32 or 6061-T6. Bolted-on supports shall either be the same material and thickness as the enclosure or 2.7 mm minimum steel. The side panels and filter shell shall be fabricated of 2.0 mm minimum aluminum sheet.

7.2.2.3 All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filed to a radius of 0.8 mm, minimum. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders, and welding operators shall conform to the requirements and practices on AWS B3.0 and C5.6 for aluminum.

7.2.2.4 Aluminum surfaces shall conform to the following:

7.2.2.4.1 An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning procedure shall be to immerse in inhibited alkaline cleaner [Oakite 61A, Diversey 909 (or equivalent) in mix of 45 to 60 g per liter of distilled water] at 71°C for 5 minutes. Rinse in cold water. The etching procedure shall be to immerse in a sodium solution [3.7 g sodium fluoride plus 37.5 g sodium hydroxide mix per liter of distilled water] at 66°C for 5 minutes. Rinse in cold water. Desmut in a 50% by volume nitric acid solution at 20°C for 2 minutes. Rinse in cold water.

7.2.2.4.2 The anodic coating shall conform to MIL-A-8625C (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, Class I Coating except the outer housing surface coating shall have a 0.018 mm minimum thickness and a 20 mg per 500 mm² minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution (pH 5.0 to 6.5) of nickel acetate at 99°C for 15 minutes.

- 7.2.2.5 The enclosure doorframes shall be double flanged out on all four sides and shall have strikers to hold tension on and form a firm seal between the door gasket and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 4 (± 2) mm.
- 7.2.2.6 Gaskets shall be provided on all door openings and shall be dust-tight. Gaskets shall be 6 mm minimum thickness, closed cell neoprene or silicone [BOYD R-10480 (or equal)] and shall be permanently bonded to the metal. If neoprene is used, the mating surface of the gaskets shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A gasket top channel shall be provided to support the top gasket on the door (prevents gasket gravitational fatigue).
- 7.2.2.7 Cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness of either 4.8 mm aluminum or 2.7 mm steel.
- 7.2.2.8 The housing shall be provided with two lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 20 mm. Each eye shall be able to support a weight load of 450 kg.
- 7.2.2.9 All exterior bolt heads shall be tamperproof type.

7.2.3 **Door Latches and Locks**

- 7.2.3.1 The latching handles shall have provision for padlocking in the closed position. Each handle shall be 20 mm minimum diameter stainless steel with a minimum 13 mm shank. The padlocking attachment shall be placed at 100 mm from the handle shank center to clear the lock and key. An additional 100 mm minimum gripping length shall be provided.
- 7.2.3.2 The latching mechanism shall be a 3-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 6 mm thick by 20 mm wide, minimum.
- 7.2.3.3 When the door is closed and latched, the door shall be locked. The locks and handles shall be on the right side of the front door and left side of the rear door. The lock support shall be rigidly mounted on the door. In the locked position, the bolt throw shall extend a minimum of 6 (± 0.8) mm into the latch cam area. A seal shall be provided to prevent dust or water entry through the lock opening.
- 7.2.3.4 The locks shall be a Best Company 5L7RD Series (or an approved equal) with a red construction core. Two keys shall be supplied with each cabinet. The keys shall be removable in the locked position only.

- 7.2.3.5 The center latch cam shall be fabricated of 4.7 mm minimum thickness steel or aluminum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.
- 7.2.3.6 Rollers shall have a 22 mm minimum diameter, with Nylon wheels and steel ball bearings.
- 7.2.4 **The general requirements** for housing ventilation including intake, exhaust, filtration, fan assembly, and environmental control, as follows:
 - 7.2.4.1 Both doors shall be provided with louvered vents. The louvered vent depth shall be a maximum of 6 mm. A removable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter, providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 5 mm to house the filter. The filter and shell shall be held firmly in place with a bottom bracket and a spring-loaded upper clamp. No incoming air shall bypass the filter. The bottom filter bracket shall be formed to create a waterproof sump with drain holes to the outside housing.
 - 7.2.4.1.1 The filter shall be 152 mm high by 406 mm wide by 22 mm thick. The filter shall trap particles 2 microns and larger.
 - 7.2.4.2 The intake (including filter with shell) and exhaust areas shall pass a minimum of 0.74 m³ of air per minute.
 - 7.2.4.3 The housing shall be equipped with an electric fan with ball or roller bearings and a capacity of at least 2.8 m³ of free air delivery per minute. The fan shall be mounted within the housing and vented.
 - 7.2.4.4 The fan shall be thermostatically controlled and shall be manually adjustable to turn on between 33°C and 65°C with a differential of not more than 6°C between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor ampacity. The manual adjustment shall be graded in 10°C increment.
- 7.2.5 **Hinges and Door Catches**
 - 7.2.5.1 Hinges with 2 bolts per leaf shall be provided to bolt the door to the enclosure. Each door shall have 3 stainless steel hinges. Each hinge shall be 90 mm minimum length and have a fixed pin. The pin ends shall be welded to the hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

7.2.5.2 Front and rear doors shall be provided with catches to hold the door open at both 90° and 180° (±10°). The catch minimum diameter shall be either 9.5 mm for plated steel or aluminum rods, or 6 mm for stainless steel. The catches shall be capable of holding the door open at 90° in a 95 km/hr wind, acting at an angle perpendicular to the plane of the door.

7.2.6 **Police Panel** (Model 336 and Model 336S Cabinet)

7.2.6.1 A police panel assembly shall be provided to allow limited access to intersection control by police officers. The police panel assembly, including switches, shall not extend into the cabinet more than 38 mm.

7.2.6.2 The police panel door shall be equipped with a lock. The lock shall be keyed with a master police key. Two keys shall be furnished with each police lock. Each police key shall have a shaft at least 44 mm in length.

7.2.6.3 The police panel shall contain two DPST toggle power switches.

7.2.6.3.1 The Model 336 and 336S Intersection Cabinets shall have one switch labeled “ON-OFF” and another labeled “FLASH/AUTOMATIC”.

7.2.6.3.2 The Model 336 and 336S Ramp Meter Cabinets shall have one switch labeled “ON-OFF LIGHTS” and another labeled “POLICE CONTROL ON-OFF”.

7.2.6.4 The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

7.2.6.5 The panel assembly shall have a drain to prevent water collecting within the assembly. The drain shall be channeled to the outside.

7.2.7 **Cabinet Light Fixture**

7.2.7.1 An 8-watt, self-starting fluorescent cabinet light shall be installed in each controller cabinet (see Cabinet Details Drawings). The fixture shall be mounted to the cabinet exhaust area cover plate by screw and self-locking nut. The mounting hardware shall not penetrate the exterior of the cabinet shell. The fixture and fluorescent tube shall not interfere with access to any cabinet component or TBK. The fixture will be controlled from a door-operated switch located at the rear door. The fixture power shall be switched “ON” when the rear door is opened. In addition to the rear door switch, the fixture circuit shall incorporate an accessible power “ON-OFF” switch. Power for the light fixture shall be supplied from the load side of the 15 amp Equipment breaker of the PDA through an “in-line” type fuse holder (1 amp fuse) through the normally closed cabinet rear door switch to the light fixture (see Equipment Mounting Drawings).

SECTION 3 – CABINET CAGE REQUIREMENTS

- 7.3.1 **A standard EIA 483 mm rack cage** shall be installed inside the housing for mounting of the controller unit and cabinet assemblies.
- 7.3.2 **The EIA rack portion of the cage** shall consist of two pairs of continuous, adjustable equipment mounting angles. The angle nominal thickness shall either be 3.4 mm plated steel, 2.7 mm stainless steel, or 3.9 mm aluminum. The angles shall be tapped with 10-32 threads with EIA universal spacing. The angle shall comply with Standard EIA-310-B and shall be supported at the top and bottom by either welded or bolted support angles to form a cage.
- 7.3.3 **Clearance** between rails for mounting assemblies shall be 450 mm.
- 7.3.4 **Two steel supporting angles** extending from the front to the back rails shall be supplied with Model 336 or Model 336S cabinets to support the controller unit. The angles shall be designed to support a minimum of 23 kg each. The horizontal side of each angle shall be a minimum of 75 mm. The angles shall be vertically adjustable.
- 7.3.5 **The cage** shall be bolted to the cabinet at eight points, via the housing cage supports and associated spacer brackets - four at the top and four at the bottom of the rails.
- 7.3.6 **The cage** shall be centered within the cabinet.

SECTION 4 – CABINET ASSEMBLIES REQUIREMENTS

7.4.1 General Requirements

7.4.1.1 The following equipment shall be completely removable from the cabinet without removing any other equipment and using only a slotted or Phillips screwdriver:

Power Distribution Assembly
Pull-Out Drawer Assembly (336S)

7.4.1.2 All fuses, circuit breakers, switches (except police panel switches, fan fuse and cabinet light fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

7.4.1.3 All equipment in the cabinet, when required shall be permanently and clearly labeled. The marker strips shall be made of material that can be easily and legibly written upon using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with all items installed.

7.4.1.4 Assemblies and files shall be fabricated of 1.5 mm minimum thickness aluminum or stainless steel sheet. The metal surface shall be treated with clear chromate.

7.4.1.4.1 Additional requirements for Model 336 and Model 336S Cabinets:

7.4.1.4.1.1 Resistor-capacitor transient suppression shall be provided at all AC relay sockets (across relay coil) except for the flash transfer relays (FTR) in the output files, where one suppression device may be common for all.

7.4.1.4.1.2 A leakage resistor which permits a small amount of current to pass through the heavy duty relay coil, shall be installed across the terminals of relay sockets to overcome the residual magnetism.

7.4.1.4.1.3 Assembly or file depth dimension shall include TBKs.

7.4.1.4.1.4 All assemblies and files (except pullout drawer assembly) shall allow air circulation through the top and bottom unless specifically called out otherwise.

7.4.1.4.1.5 Socket types for the following equipment shall be:

Switch Pack	BEAU S-5412-XX (or equal)
Heavy Duty Relay	BEAU S-5408-XX (or equal)
Flasher Unit & Power Supply Module	BEAU S-5406-XX (or equal)
210 Monitor Unit	PCB 28/56S

7.4.1.4.1.6 Connector sockets for flasher unit, power supply, and switch pack modules shall be mounted with their front face 190 mm deep from assembly or file front panel (note output file exception).

7.4.1.4.1.7 Guides (top and bottom) shall be provided for switch pack modules, flasher units, monitor unit, WDT module, detector and isolator modules, and power supply module (bottom only). The guides shall begin 25 (± 13) mm in from the front panel surface and extend to within 13 mm of the connector socket face.

7.4.2 Power Distribution Assembly

7.4.2.1 The following equipment shall be provided with the power distribution assemblies:

7.4.2.1.1 PDA #2:

- 1– Duplex NEMA 5-15R Controller Receptacle
- 2– Duplex NEMA 5-15R Equipment Receptacle
- 1 – 1 Pole, 50 amp, 120 VAC Main Circuit Breaker
- 1 – 1 Pole, 15 amp, 120 VAC Equipment Circuit Breaker
- 6 – 1 Pole, 15 amp, 120 VAC Signal Bus and Illuminated Sign Circuit Breaker
- 1 – 2 Pole Ganged, 20 amp, 120 VAC Flash Bus Circuit Breaker
- 1 – Mercury Contactor, 60 amp, 120 VAC
- 2 – Model 204 Flasher Unit and Socket
- 1 – Model 206 Power Supply Module and Socket
- 1 – AUTO/FLASH Control Switch
- 1 – FLASH On Indicator Light
- 3 – 10 Position TBK T1, T2 & T4
- 1 – 4 Position TBK T3

7.4.2.1.2 PDA #3:

- 1– Duplex NEMA 5-15R Controller Receptacle
- 2– Duplex NEMA 5-15R Equipment Receptacle
- 1 – 1 Pole, 30 amp, 120 VAC Main Circuit Breaker
- 3 – 1 Pole, 15 amp, 120 VAC Circuit Breaker (Equip & Field)
- 1 – Model 206 Power Supply Module and Socket
- 1 – Model 208 Monitor Unit and Socket
- 1 – Model 430 Heavy Duty Relay and Socket (Transfer Relay)
- 1 – Watchdog Timer ON/OFF-RESET Control Switch
- 3 – Model 200 Switchpack Socket
- 3 – 10 Position TBK T1, T2, and T4
- 1 – 4 Position TBK T3

7.4.2.1.3 PDA #5

- 2 - Duplex NEMA 5-15R GFCI Receptacles
- 2 - Duplex NEMA 5-15R Equipment Receptacles
- 1 - 1 Pole, 40 amp, 120 VAC Main Circuit Breaker
- 2 - 1 Pole, 15 amp, 120 VAC Equipment Circuit Breaker
- 1 - 1 Pole, 15 amp, 120 VAC GFI Receptacle Breaker
- 1 - 1 Pole 15 amp, 120 VAC Cabinet Accessory Breaker (Fan and Light)
- 1 - 1 Pole, 15 amp, 120 VAC Spare Breaker

7.4.2.2 Breaker ratings shall be shown on face of breaker or handle. Breaker function shall be labeled below breaker on front panel.

7.4.2.3 The equipment receptacles shall have ground-fault circuit interruption as defined in the National Electrical Code.

7.4.2.4 All conductors from the power distribution assembly routed to the cabinet wiring shall be connected to the TBK on the common side, except for the AC power conductor between the service TBK and main circuit breaker. All internal conductors terminating at the blocks shall be connected to the other side of the blocks.

7.4.2.5 Additional requirements for Model 336 and Model 336S Cabinets:

7.4.2.5.1 The AUTO/FLASH switch, when placed in FLASH position (down), shall energize the Mercury Contactor (MC) coil. When the switch is placed in the AUTO position (up), the switch packs shall control the signal indications. The switch shall be a SPST toggle control switch.

7.4.2.5.2 The FLASH indicator light labeled "FLASH ON" shall be mounted on the PDA front panel. The lamp shall be driven as specified in Section 7.4.2.5.6.2.

7.4.2.5.3 Ganged circuit breakers shall be certified by the circuit breaker manufacturer that their circuit breakers shall gang trip.

7.4.2.5.4 Illuminated Sign Circuit Breaker - A 15 amp, 120 volt AC circuit breaker shall be installed for illuminated sign circuit protection. The breaker shall be placed on the load side of the main breaker. The breaker shall be located on the front panel of the PDA assembly next to the other breakers.

7.4.2.5.5 The monitor unit ON/OFF-RESET switch shall be a DPST toggle control mounted on the PDA #3 front panel. When placed in the OFF-RESET (down) position, a grounded input shall be presented at the monitor unit Pin 21 (resetting the WDT circuitry). The other side of the switch circuit bypasses the monitor unit.

7.4.2.5.6 Signal Bus Circuit Breakers:

7.4.2.5.6.1 Five single-pole, 15 amp circuit breakers with auxiliary switch feature and medium trip delay characteristic shall be provided.

7.4.2.5.6.2 The five breakers shall be wired and routed per the Circuit Breaker Line Diagram. The breaker auxiliary switch circuit shall be open when the breaker is in the ON position. The auxiliary circuits shall be wired in parallel so that any tripped breaker shall energize the mercury contactor coil, flash transfer relay coils, and the FLASH ON indicator (Section 7.4.2.5.2). The auxiliary contacts shall be rated at 5 amps, 120 VAC, minimum (fast-on type connection).

7.4.2.5.7 Model 206 Power Supply Module:

7.4.2.5.7.1 A power supply shall be provided to supply +24 VDC to the input and output files for use by their associated devices. The front panel shall include AC and DC fuses, "POWER ON" light, and test points for monitoring the output voltages. The power supply shall be of ferro-resonant design having no active components and will conform to the following requirements:

1. Line Regulation: 2% from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1% frequency change
2. Load Regulation: 5% from 1 amp to 5 amps with a maximum temperature rise of 30°C above ambient
3. Design Voltage: +24 (± 0.5) VDC at full load, 30°C, 115 VAC incoming after a 30 minute warm-up period
4. Full Load Current: 5 amps, minimum
5. Ripple Noise: 2 volts peak-to-peak and 500 mV RMS at full load
6. Line Voltage: 90 to 135 VAC
7. Efficiency: 70% minimum
8. Minimum Voltage: +22.8 VDC
9. Circuit capacitors shall be rated for 40 volts, minimum.

7.4.2.5.7.2 The module chassis shall be vented. Its top and side shall be open except for unit supports.

7.4.2.5.7.3 When resident in the PDA assembly, the module shall be held firmly in place by its stud screw, assembly connector support panel, and a wingnut.

7.4.2.5.7.4 Two 0.5 ohm, 10 watt minimum, wire-wound power resistors with a 0.2 μ H inductance shall be provided; 1 on the AC+ power line and 1 on the AC- line. Three MOV surge arrestors rated for 20 Joules minimum, shall be provided between AC+ and EG, AC- and EG, and between AC+ and AC-. A 0.68 μ F capacitor shall be placed across AC+ and AC- between the 2 power resistors and the MOV's.

7.4.2.5.7.5 Terminal screw size shall be 10-32 for TBK T1, T2, & T4 and 6-32 for TBK T3.

7.4.3 **Input File** (Model 336 and Model 336S Cabinets)

7.4.3.1 The file shall have a maximum depth of 215 mm and shall intermate with and support 14, 2-channel detector or isolator units.

7.4.3.2 The file shall provide a PCB 22/44S connector which shall be a DALE EB7CS22GY (or equal) and shall be centered vertically for each 2-channel detector. The associated number and letter side connectors shall be shorted internally. Pins D, E, F, J, K L, and W shall be brought out to an 8-position TBK on the back of the file. The output emitters shall be common grounded with the ground terminating at TB 15, position 4. Position 8 of the TBK is assigned to EG and is used to terminate lead-in shields.

7.4.3.3 The input file shall be provided with marker strips to identify isolators and detectors in the file.

7.4.3.4 TBK terminal screw size shall be 8-32.

7.4.4 **Output File** (Model 336 and Model 336S Cabinets)

7.4.4.1 General Requirements:

7.4.4.1.1 The output file shall be provided with marker strips to identify switch packs when mounted in the file.

7.4.4.1.2 Switch pack connectors, monitor unit connectors, flash transfer relay sockets, and flash programming connectors shall be accessible from the back of the output file without the use of tools or removal of any other equipment.

7.4.4.1.3 TBK 01 and 03 terminal positions shall be labeled functionally. Terminal screw size shall be 8-32.

7.4.4.1.4 Field wire TBKs shall be mounted vertically on the back of the assembly. The output file shall have 3 TBKs with 12 positions. Terminal position screw size shall be 10-32.

7.4.4.1.5 The depth of the file shall not exceed 368 mm.

7.4.4.1.6 The flash programming connectors shall be Molex Type 1375 (or equal). The receptacle shall be mounted on the file with a programmable plug connected. The plug connector, with programming jumpers, shall be furnished for each circuit to allow red or yellow flash programming. Plug pins shall be crimped and soldered.

7.4.4.1.7 TBK 02 and 04 terminal screw size shall be 6-32.

- 7.4.4.1.8 Output file connectors and sockets shall be hard wired and PCBs will not be allowed.
- 7.4.4.2 Output File #1:
 - 7.4.4.2.1 The output file shall be capable of containing 12 Model 200 switch packs, 4 Model 430 flash transfer relays, and the Model 210 monitor unit. A monitor unit shall be furnished with each output file. The construction plans shall determine the number of flash transfer relays and switch packs that will be furnished with the output file.
 - 7.4.4.2.2 The red and yellow output circuits of switch packs 1, 2, 4, 5, 7, 8, 10, and 11 shall be made available at a Molex receptacle/plug connection for flash selectability.
 - 7.4.4.2.3 It shall be possible to remove the Model 210 monitor unit without causing the intersection to go into flashing operation. The cabinet shall be wired so that, with the front cabinet door closed and with the monitor unit removed, the intersection shall go into flashing operation (see One Line Diagram). The cabinet shall contain a conspicuous warning against operation with the monitor unit removed.
 - 7.4.4.2.4 The monitor unit compartment including the housed monitor unit, exclusive of the handle, shall extend no farther than 32 mm in front of the rack front surface. The switch pack socket connector front surface shall be no more than 216 mm in depth from the front surface of the output file.
- 7.4.4.3 Auxiliary Output File (Model 420):
 - 7.4.4.3.1 The auxiliary output file shall be capable of containing 6 Model 200 switch packs and 2 Model 430 flash transfer relays. The construction plans shall determine the number of flash transfer relays and switch packs that will be furnished with the auxiliary output file.
 - 7.4.4.3.2 The red and yellow output circuits of switch packs A1, A2, A4, and A5 shall be made available at a Molex receptacle/plug connection for flash selectability.
- 7.4.5 **Side Panels** (Model 336 and Model 336S Cabinets)
 - 7.4.5.1 Two panels shall be provided and mounted on the cage parallel to the cabinet sides. In viewing from the back door, the left side panel shall be designated as the "Input Panel" and the right side panel shall be designated as the "Service Panel".
 - 7.4.5.2 Terminal blocks shall be mounted on the panel and wired to the designated terminations as per applicable cabinet diagrams. The use of raceways shall not be permitted. Terminal blocks and terminals shall be identified as shown on the cabinet wiring diagram. Input panel TBK screw size shall be 8-32.

7.4.6 **Cabinet Harnesses** (Model 336 and Model 336S Cabinets)

7.4.6.1 The C1 harness shall be a minimum of 1.2 m in length. The harness wire bundle shall be provided with external protection and routed on the input panel side of the cabinet. Adequate length shall be provided to allow the C1P connector to properly connect any STATE approved controller unit mounted in the cabinet.

7.4.6.2 One end of the C1 harness shall be the C1P connector with pin contacts wired per the detail assignment. The other ends of the harnesses shall terminate as follows:

- Harness #2 - C5S connector (connected to C5P on either the input panel or auxiliary output file)
C6S connector (connected to C6P on output/PDA assembly)
Assigned input file positions and logic ground bus
- Harness #3 - C4S connector (connected to C4P on output file)
Assigned input file positions
Input Panel TBK and logic ground bus

7.4.6.3 Conductors between the C1 connector and the input file shall be of adequate length to allow any conductor to be connected to any detector output terminal (positions S, F, or W).

7.4.7 **Pullout Drawer Assembly**

7.4.7.1 Pullout Drawer/Cabinet Print Holder: A pullout drawer shall be installed in the cabinet cage (see Equipment Mounting Drawing).

7.4.7.2 The drawer shall be 430 mm long by 430 mm wide by 44 mm deep. It shall have a hinged top that covers the storage box area and also provides a smooth surface to write on.

7.4.7.3 The drawer shall be General Devices D4080-19W (or equal).

SECTION 5 – CABINET WIRING REQUIREMENTS

7.5.1 Cabinet Wiring Diagram

7.5.1.1 The cabinet wiring diagram for Models 336 or 336S cabinets shall be furnished on current ODOT drawings for the appropriate cabinet model. One full-sized reproducible master copy of the drawing will be furnished, upon request. The drawings are available from the Traffic Signal Services Unit manager. A cabinet wiring diagram for Model 344 cabinet shall be furnished.

7.5.1.2 The Contractor shall add to the drawing all information and details required giving an accurate description of the wiring and operation of each individual cabinet. For Model 336 and Model 336S cabinets, the information required includes the following:

1. Software program number and C1 connector pin program assigned functions
2. Input file phase and loop number references
3. Output file phase references
4. Location and phase reference for all input/output devices furnished
5. Modifications made to standard cabinet wiring
6. Intersection layout
7. Phase sequence diagram
8. Preemption sequence diagram (if applicable)

7.5.1.2.1 For Model 336 and Model 336S Cabinets, the intersection layout shall include all vehicle signals, pedestrian signals, vehicle detectors, push buttons, lane usage arrows, and special devices located and identified as shown on the plans. A north arrow shall also be included and the intersecting streets shall be identified.

7.5.1.2.2 For Model 336 and Model 336S Cabinets, the phase and preemption sequence diagrams shall refer to the phase designations and sequence shown on the plans for both normal phase rotation and preemption.

7.5.1.3 Four OZALID-type (or equivalent) copies of the wiring diagram shall be furnished with each Model 336 or Model 336S controller cabinet. The copies shall not be reduced in size.

7.5.2 Conductors (Model 336 and Model 336S Cabinets)

7.5.2.1 All conductors used in cabinet wiring shall terminate with properly sized, insulated, spring spade type terminals except when soldered to a through-panel solder lug on the rear side of the TBK or as specified otherwise. All spade connectors on wires connecting the input panel to the input files shall be crimped and soldered to the wires.

7.5.2.1.1 All crimp-style connectors shall be applied with a tool that prevents opening of the handles until the crimp cycle is completed.

- 7.5.2.1.2 All conductor sizes shown are AWG.
- 7.5.2.2 Conductors between the service terminal AC- and EG and their associated bus, the EG bus conductor to power distribution assembly and cage rail, and the AC- bus to power distribution assembly shall be No. 8 (or larger).
- 7.5.2.3 All conductors, unless otherwise specified, shall be stranded No. 22 (or larger). Conductors shall be rated for 600 volts and shall conform to IMSA Specification 50-2 (or better). The insulation shall have a minimum thickness of 10 mils and shall be Nylon-jacketed polyvinyl chloride, except that conductors No. 14 and larger may have Type THHN/THWN insulation.
- 7.5.2.4 All conductors, except those that can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.
- 7.5.2.5 All conductors shall conform to the following color-code requirements:
1. The grounded conductors of AC circuits shall be identified by a continuous white or gray color.
 2. The equipment-grounding conductors shall be identified by a solid green color or by a continuous green color with one or more yellow stripes.
 3. The DC logic ground conductors shall be identified by a solid white color with a red stripe.
 4. The ungrounded conductors shall be identified by any color not specified in 1, 2, or 3 above.
- 7.5.2.6 All wiring harnesses shall be neat, firm, and routed to minimize crosstalk and electrical interference.
- 7.5.2.6.1 Wiring containing AC shall be routed and bundled separately or shielded separately from all logic voltage control circuits.
- 7.5.2.6.2 Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.
- 7.5.2.7 Within the cabinet, the DC logic ground and EG shall be electrically isolated from the AC grounded conductor and each other by 500 megohms when tested at 500 VAC, with the power line surge protector disconnected.
- 7.5.2.8 The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 6 mm shall be used for securing the bus to the service panel.
- 7.5.2.9 The cabinet power supply DC ground shall be connected to the DC logic ground bus using a No. 14 (or larger) stranded copper wire.

7.5.2.10 Each detector lead-in pair for input panels #1 and #3, from the field terminals to the input file terminals, shall be a cable of IMSA type 50-2 (or better). The stranded, tinned, copper drain wire shall be connected to the "L" terminal on the input file TBKs. This input terminal shall be connected to the equipment grounding bus through a single conductor. Each connection shall be made by using a crimp connector that is soldered after the connector is crimped to the wire. These cables shall be heat shrunk protected - both the drain wire and the foil shield, to prevent shorting against the contacts on the back of the input file.

7.5.3 **Conductors** (Model 344 Cabinet)

7.5.3.1 All conductors used in cabinet wiring shall terminate with properly sized, insulated, spring spade type terminals. All spade connectors on wires shall be crimped. Sensor and device wiring shall be terminated per manufacturer's instructions. In the absence of manufacturer termination instructions, the sensor and device wiring shall be terminated with a spade connector that has been crimped and soldered to the wire.

7.5.3.2 All crimp style connectors shall be applied with a tool that prevents openings of the handles until the crimp cycle is completed.

7.5.3.3 All conductors shall conform to the following color code requirements:

1. The grounded conductors of AC circuits shall be identified by a continuous white or gray color.
2. The equipment-grounding conductors shall be identified by a solid green color or by a continuous green color with one or more yellow stripes.
3. The ungrounded conductors shall be identified by any color not specified in 1 or 2 above.

7.5.3.3 Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

7.5.3.4 The AC copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 6 mm shall be used for securing the bus to the service panel. Maintenance personnel shall protect the bus from accidental contact.

7.5.4 **Terminal Blocks** (Model 336 and Model 336S Cabinets)

7.5.4.1 The TBKs shall be barrier type, rated at 20 amps, 600 volts RMS, minimum. The terminal screws shall be 7.9 mm minimum length, nickel-plated, brass binder head type with screw inserts of the same material. Screw size is called out under associated cabinet assembly, file or side panel.

- 7.5.4.2 The terminals of the power line service TBK shall be labeled “L1”, “AC-“, and “EG” and shall be covered with a clear insulating material to prevent inadvertent contact. Terminating lugs large enough to accommodate No. 2 conductors shall be furnished for the service TBK. The TBK shall be rated for 50 amps at 600 volts peak, minimum. The block shall be either a double row, three position screw/insert with shorting bar (screws, inserts, and shorting bars shall be nickel-plated brass) or a Marathon #1423552 (or equal). If the Marathon block is used, the surge protectors shall be terminated under a screw head (not common with AC+, AC-, or EG service conductors). The AC+, AC-, and EG conductors connecting to the service terminals and appropriate busses shall not be spade lugged.
- 7.5.5 **Terminal Blocks** (Model 344 Cabinet)
- 7.5.5.1 All terminal blocks shall comply with UL 1059 or NEMA ICS 4.
- 7.5.5.2 For No. 10 AWG conductors or smaller, one-piece double terminal, barrier type with binder screw terminals shall be used. Terminal ampacities shall be equal or greater than conductor ampacities.
- 7.5.5.3 For No. 8 AWG conductors or larger, use either one-piece or factory-assembled sectional barrier type with box-lug terminals having a pressure plate between screw and conductor. Use terminals of correct size for the conductors to be connected.
- 7.5.6 **Detector Test Buttons** (Model 336 and Model 336S Cabinets)
- 7.5.6.1 A detector test panel containing 12 normally open push buttons shall be furnished and installed on the inside front cabinet door or across the top front of the rack assembly. All push buttons shall be wired directly to the back of the input file.
- 7.5.6.1.1 There shall be a pushbutton for one detector input in a Model 336 or Model 336S Intersection Cabinet associated with each of the eight vehicle (count and extend) and four pedestrian phases, whether or not such phases are used at a particular location.
- 7.5.6.1.2 There shall be a pushbutton in a Model 336 or Model 336S Ramp Meter Cabinet for one detector input associated with the following C1 inputs: 39, 44, 45, 47, 48, 50, 52, 56, 57, 59, 61, and 81.
- 7.5.6.2 The panel shall have a connector for disconnecting all test panel wiring from the input file.
- 7.5.6.3 All pushbuttons shall be labeled by function. Pushbuttons in a Model 336 or Model 336S Intersection Cabinet shall also be labeled by phase.

SECTION 6 – CABINET TRANSIENT SURGE SUPPRESSION REQUIREMENTS

7.6.1 Power Line

7.6.1.1 The power line surge protector shall be metal oxide varistor (MOV). One shall be installed between AC+ and EG and the other between AC- and EG. The MOV shall have the following ratings:

Recurrent peak voltage:	212 volts
Energy rating:	50 Joules, maximum
Power dissipation:	0.85 watt, average
Peak current for pulses:	2,000 amps for less than 6 μ S
Standby current:	Less than 1 mA

7.6.2 Modem Interconnect Lines (Model 336 and Model 336S Cabinets)

7.6.2.1 General Requirements:

1. Shall be installed in all cabinets
2. Shall suppress bipolar and bi-directional transients
3. Shall fail in the open circuit configuration
4. Shall be of solid state design and contain no spark gap or gas tube
5. Leakage current to ground, maximum: 0.2 mA
6. Circuit impedance loading: $<25\Omega$

7.6.2.2 TVSS Performance:

1. Rated single transient energy: 75 (10 x 100 μ S, Joules)
2. Single pulse transient current: 2,000(8 x 20 μ S, amps peak)
3. Maximum clamping voltage: 36(1 kV, 200 A 8 x 50 μ S, V peak)

7.6.2.3 Physical Characteristics:

1. Operating temperature: -34°C to 74°C
2. Dimensions, maximum: L 125 mm x W 100 mm x D 50 mm

7.6.3 Telephone Line Protection (Model 344 Cabinet)

Protection Modes	Line-to-Line (L-L) and Line-to-Ground (L-G) Mode
Dynamic Response Time	1 nanosecond (maximum)
Max. Peak Signal Voltage	24
Nominal Breakdown Voltage	30
Max. Current (I_p 10x1000 μ S)	71 amps
Max. Clamp Voltage @ I_p	38
Capacitance	<1400 pf
Max. Continuous Current	150 mA
Nominal Series Resistance	8 ohms

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CHAPTER 8

SPECIFICATIONS FOR MODEM MODULES

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SECTION 1 – MODEL 400 MODEM MODULE GENERAL REQUIREMENTS

- 8.1.1 **The Modem shall provide** 4-wire full duplex communications.
- 8.1.2 **The Modem shall be compatible with** Bell Standard 202S and comply with the following requirements:
1. Data Rate: 300 to 1,200 baud modulation
 2. Modulation: Phase coherent frequency shift keying (FSK)
 3. Data Format: Asynchronous, serial by bit
 4. Line and Signal Requirements: Type 3002 voice-grade, unconditioned
 5. ACIA and Modem Interface: EIA-232-C standards
 6. Tone Carrier Frequencies (Transmit and Receive): 1200 Hz (MARK) and 2200 Hz (SPACE) with $\pm 1\%$ tolerance. The operating band shall be (half power, -3dB) between 1000 and 2400 Hz
 7. Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1700 Hz) continuous or switch selectable
 8. Receiver Input Sensitivity: 0 to -40 dB
 9. Receiver Bandpass Filter: Shall meet the error rate requirement specified in Paragraph 8.1.2.15 and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.
 10. Clear-to-Send (CTS) Delay: 12 (± 2) ms
 11. Receive Line Signal Detect Time: 8 (± 2) ms mark frequency
 12. Receive Line Squelch: 6.5 (± 1) ms, 0 ms (OUT)
 13. Soft Carrier (900 Hz) Turn Off Time: 10 (± 2) ms
 14. Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission
 15. Error Rate: Shall not exceed 1 bit in 100,000 bits, with a signal-to-noise ratio of 16 dB, measured with flat-weight over a 300 to 3,000 Hz band.
 16. Transmit Noise: less than -50 dB across 600 ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output
- 8.1.3 **The Modem power requirements** are as follows:
- | <u>Input Voltages</u> | <u>Maximum Current Consumption</u> |
|-----------------------|------------------------------------|
| +12 VDC | 75 mA |
| -12 VDC | 75 mA |
- 8.1.4 **Indicators** shall be provided on the front of the Modem to indicate Carrier Detect, Transmit Data, and Receive Data.

SECTION 2 – RADIO MODEM REQUIREMENTS

8.2.1 **General Requirements**

- 8.2.1.1 A Radio Modem shall be a stand-alone, data transceiver capable of direct line-of-sight, radio frequency (rf) transmission using spread spectrum technology compliant with FCC part 15.
- 8.2.1.2 For purposes of use with Model 170E microprocessor traffic signal controllers, a Radio Modem shall include the transceiver, antenna, in-line lightning arrestor (if required), power supply, and all cable and mounting hardware necessary for fulfilling the intended use stated herein and in applicable portions of Chapter 1 (including Section 8 testing requirements).

8.2.2 **Physical properties**

- 8.2.2.1 Exterior dimensions excluding antenna and power supply shall not exceed 1.97" H x 4.72" W x 5.12" D (50 mm x 120 mm x 130 mm)
- 8.2.2.2 Unit weight shall not exceed 0.5 kg.
- 8.2.2.3 The power supply shall not exceed 1.97" (50 mm) on any dimension and shall be of the type that plugs directly into an available duplex receptacle located in the controller cabinet.
- 8.2.2.4 Battery backup is not required, however any features stored in software shall be retained for no less than 30 days.
- 8.2.2.5 The antenna shall not exceed 4.72" (120 mm) in length if housed within the controller cabinet. The use of an external antenna is conditional, and if approved requires an in-line lightning arrestor suitable for the frequency in use. Such lightning arrestors shall be mounted external to the traffic signal controller cabinet. Lightning arrestors for pole-mounted antennas shall be connected to a ground rod at the pole base.

8.2.3 **Data transmission requirements between Model 170E controller and radio modem**

- 8.2.3.1 Baud Rate Asynchronous shall be selectable within the range of 1.2 to 38.4 Kbps using a standard EIA-232C (DB9F) serial data interface.
- 8.2.3.2 Transmission delay shall be less than or equal to 12 ms.
- 8.2.3.3 Signal acquisition time at the receiver shall be less than or equal to 8 ms.

8.2.4 Performance Requirements

- 8.2.4.1 The radio modem and supporting peripherals shall provide a signal strength at the receiving end of not less than -70db with a bit error rate (BER) less than 10^{-6} .
- 8.2.4.2 The radio modem must communicate or interface with all other equipment.
- 8.2.5 **Indicators:** The radio modem unit shall provide indicators showing power on (PWR), transmitted rf data, and received rf data.
- 8.2.6 **Types:** Radio modems may be either transparent (emulating an EIA-232 cable to a distant device) or packet. The allowable frequency ranges for either type shall be 915 ± 15 MHz or 2.44 ± 0.04 Ghz.
- 8.2.7 **Power:** The radio modem shall operate from 120 VAC (available in the traffic signal controller cabinet) and must provide conversion to the proper radio modem operating voltage. Spurious output shall meet the requirements of FCC Part 15.

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CHAPTER 9

SPECIFICATIONS FOR MODEL 2070 CONTROLLER UNIT

FUTURE CHAPTER

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CHAPTER 10

SPECIFICATION FOR MODEL 2070 PERIPHERAL EQUIPMENT

FUTURE CHAPTER

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CHAPTER 11

**SPECIFICATIONS FOR MODEL 170ATC CONTROLLER UNIT,
MODEL 170ATC-1 ENGINE BOARD MODULE,
MODEL 170ATC-2 INTERFACE MODULE,
MODEL 170ATC-3 FRONT PANEL ASSEMBLY,
MODEL 170ATC-4 UNIT POWER SUPPLY**

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SECTION 1 - MODEL 170ATC CONTROLLER UNIT REQUIREMENTS

11.1.1 Unit Composition

11.1.1.1 The Model 170ATC Controller Unit shall consist of the following components:

Unit Chassis Communications System Interface (per Model 170E)
Connectors C1S, C2S, C20S, C30S, C40S, and T-1 Engine Board Module (Model 170ATC-1) with MC68360 microcomputer
Interface Module (Model 170ATC-2) with Field I/O controller
Input/output Interface (per Model 170E)
Front Panel Assembly (Model 170ATC-3)
Unit Power Supply with external power connection (Model 170ATC-4)
Model 400 Modem

11.1.1.2 The composition weight shall not exceed 11.5 kg.

11.1.2 Unit Chassis

11.1.2.1 The controller shall be housed in a compact, portable, metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 483 mm rack. The enclosure shall be designed for convenient removal of PCBs without use of tools.

11.1.2.2 The Chassis Enclosure, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Cover Plates, Power Supply Enclosure, and Front Panel shall be made of 1.52 mm minimum Aluminum Sheet.

11.1.3 Special Connector Requirements - Daughterboard

The daughterboard shall intermate with the motherboard through the Motherboard Connector, JP1. The daughterboard shall also contain connectors, which will accept the Input and Output Modules, and the Front Panel connector, JP2. The 104 pin C1S connector shall also be mounted on the daughterboard. The C1S pin assignments are identified in Figure 17.

11.1.4 Input/Output Interface

11.1.4.1 Input/Output interface shall utilize a ground true Logic. The transfer of data between interface and working registers within the MPU shall be in 8-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of MPU read/write command at the time the given address is valid.

11.1.4.1.1 Output Interface: The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

11.1.4.1.2 Input Interface: The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each Logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC; shall be turned OFF (false) when the input current is less than 100 μ A or the input voltage exceeds 8.5 VDC; shall pull up to 12 VDC; and shall not deliver in excess of 20 mA to a short circuit to Logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

11.1.5 **Communication System Interface**

11.1.5.1 The communication system shall consist of the following:

1. CPU
2. ACIAs
3. Motherboard and daughterboard connectors and lines
4. Modem Module Connectors MC1, MC2, MC3 and MC4
5. Interface between ACIA and Modem
6. Interface between both the Modem and ACIA to C2S, C20S, C30S, C40S
7. Connector T-1 Terminal

11.1.5.1.1 The interface between the ACIA and Modem shall comply with EIA-232-C.

11.1.5.1.2 Standards and all functions under T-1, C2S, C20S, C30S, and C40S Connectors shall be referenced to the ACIA.

11.1.5.1.3 AUDIO IN and AUDIO OUT shall be referenced to the Modem.

11.1.5.1.4 The RTS and TX data lines to the Modem shall have MARK and SPACE voltages of -12 and 12 VDC respectively.

11.1.5.2 Two of the four modem slots shall be capable of supporting dual modem devices. When facing the controller front with the door open, the first and third slots from the right side of the controller shall be designated as dual modem slots. When dual modem devices are used, slots 2 and 4 cannot be used without conflict. A schematic diagram is provided in Drawing Number 16.

- 11.1.5.3 C20S, C30S, and C40S Connectors shall meet the requirements for the C2 Connector.
- 11.1.5.4 Five baud rate frequencies, 19.2 kHz (1.2 KBps), 38.4 kHz (2.4 KBps), 76.8 kHz (4.8 KBps), 153.6 kHz (9.6 KBps) and 307.2 kHz (19.2 KBps) shall be provided at the ACIA Rx/Tx Clock Inputs (pins 3 & 4). Each ACIA shall have independent baud rate selection available in software.
- 11.1.5.5 Communication from the user to the engine board shall be through SP4 (C50S connector) accessible on the FPA that shall support a baud rate of 38.4 KBps.
- 11.1.6 **Electrical Requirements**
- 11.1.6.1 The front panel and chassis shall be connected to EG.
- 11.1.6.2 A surge arrestor shall be provided between the AC+ and AC- for protection against power line noise transients. The surge arrestor shall meet the following requirements:

Recurrent peak voltage:	212 volts
Energy rating, maximum:	20 Joules
Power dissipation, average:	0.85 watt
Peak current for pulses less than 6 μ S:	2,000 amperes
Standby currents:	Less than 1 mA
- 11.1.6.3 Two 0.5 ohm, 10 watt wire-wound power resistors with a 0.2 μ H inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three surge arrestors rated for 20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68 μ F capacitor shall be added between AC+ and AC- coming off the 0.5 ohm resistor.
- 11.1.6.4 The AC power to the controller unit shall be supplied by a 3-conductor cable at least 1 m in length. The cable shall terminate in a NEMA Type 5-15P grounding-type plug.
- 11.1.6.5 Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the controller unit. The test points shall be post type, 1.6 mm diameter and 5 mm high, minimum. The clearance between test points and other components shall be 6.5 mm, minimum.

SECTION 2 - MODEL 170ATC-1 ENGINE BOARD MODULE

11.2.1 Engine Board Module

11.2.1.1 The Engine Board Module shall utilize the Motorola MC68360 microcomputer, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for State use only. The Interrupts shall be configured as follows:

Level 7 - IRQ7, ACFAIL

Level 6 - IRQ6

Level 5 - IRQ5, CPU Module Counters / Timers, LINESYNC
(auto vectored), Serial Interface Interrupts

Level 4 - IRQ4

Level 3 - IRQ3

Level 2 - IRQ2

Level 1 - IRQ1

11.2.1.2 Memory Address Organization
8000 0000 - 80FF FFFF Standard
9000 0000 - 9000 FFFF Short

11.2.1.3 Sixteen megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. A complete system memory map shall be developed by the manufacturer and provided with the documentation. (See also 11.2.2.1 - Operating System.)

11.2.1.4 When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state; and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. An on-board circuit shall sense the +5 VDC Standby Power and shift to an on-board CPU power source. The CPU on-board power shall be capable of holding the SRAM and TOD Clock up for 30 days. When the incoming +5 VDC rises to within its operating level, the Engine Board Module Circuitry shall shift from standby power to incoming +5 VDC.

11.2.1.5 Ram Memory

11.2.1.5.1 A minimum of 4 MB of DRAM, organized in 32 bit words shall be provided.

11.2.1.5.2 A minimum of 512 KB of SRAM, organized in 16 or 32 bit words shall be provided.

11.2.1.5.3 The SRAM shall draw no more than 50 μ A at +5 VDC in standby mode.

- 11.2.1.5.4 The time from the presentation of valid RAM address, select lines, and data lines to the RAM device - to the acceptance of data by the RAM device - shall not exceed 80 ns. This time shall also be less as required to fulfill "zero wait state RAM device write access" under all operational conditions.
- 11.2.1.6 Flash Memory
 - 11.2.1.6.1 A minimum of 4 MB of FLASH Memory, organized in 16 or 32 bit words, shall be provided.
 - 11.2.1.6.2 The Engine Board Module shall be equipped with all necessary circuitry for writing to the FLASH Memory under program control.
 - 11.2.1.6.3 No more than 1 MB of FLASH Memory shall be used for Boot Image (List) and a minimum of 3 MB shall be available for State use.
- 11.2.1.7 Time-of-Day Clock
 - 11.2.1.7.1 A software settable hardware Time of Day (TOD) clock shall be provided.
 - 11.2.1.7.2 Under standby power, the Time of Day Clock shall operate for a minimum of 30 days, while maintaining an accuracy of ± 1 minute per 30 days at 25 degrees C.
 - 11.2.1.7.3 The clock shall be aligned to a minimum fractional second resolution of 10 ms, and shall track fractional seconds, minutes, hours, day of month, month and year.
- 11.2.1.8 A software - driven CPU RESET signal (Active LOW) shall be provided to Reset other controller systems.
 - 11.2.1.8.1 The signal output shall be driver capable of sinking 30 mA at 30 VDC. Execution of the program module "CPURESET", in the boot image shall assert the CPU RESET signal once.
- 11.2.1.9 CPU Activity Indicator – An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU Activity Indicator
- 11.2.1.10 The Engine Board Module shall have two connectors containing 50 pins each and be equal to Samtec SSW-125-01-G-D. The dimensions of the Engine Board Module and connector layout shall be as shown in Drawing Number 15 in Appendix C.
- 11.2.1.11 The pin listing for this connector shall be as defined in Table B-4 "Engine Board Module Pin Listing".

- 11.2.1.12 The Engine Board Module shall support serial communication facilities utilizing SCC3 and SCC4 (serial port SP5 and serial port SP3 respectively).
- 11.2.1.13 Serial port SP5 and SP3 from the Engine Board Module shall intermate with connector C12S located on the front panel of the controller unit.
- 11.2.1.14 Each Serial Port with LINESYNC shall be isolated and meet EIA-485 requirements for external drivers/receivers.
- 11.2.1.15 SCC4 (serial port SP3 of the Engine Board Module) shall also be jumper selectable (at JH10 located on the Front Panel printed circuit board, hinge side) and routed to connector C40 on the rear panel as an EIA-232 port or to C12S on the front panel as an EIA-485 port.
- 11.2.1.16 Connector C12S shall be a DB-25, EIA-485 terminating plug (See Table B-5). Within the terminating plug, the Rx Data and Clock positive and negative signal lines shall be terminated through a 120-ohm, 5% resistor.
- 11.2.1.17 A dual auxiliary SCC Device (async/synch) and associated circuitry shall be furnished to provide two additional system serial ports.
- 11.2.1.18 The auxiliary SCC1 shall be assigned to the System Serial Port SP1 and be serially connected externally via the C2S Connector located on the rear panel of the controller unit.
- 11.2.1.19 The auxiliary SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68360 address and data structure and be serially connected externally via the C30S Connector located on the rear panel of the controller unit.
- 11.2.1.20 The 68360 SCC1 shall be assigned to ETHERNET (ENET) Network meeting ETHERNET 10 MBPS IEEE 802-3 (TP) 10 BASE T Standard Requirements, both hardware and software. DC Grounding plane around the network connectors and lines shall be provided. Network Lines shall be assigned as:
- Network 1 = ENET TX+
 - Network 2 = ENET TX-
 - Network 3 = ENET RX+
 - Network 4 = ENET RX-
- 11.2.1.21 The conditioned ETHERNET shall also be brought out on RJ 45 C14S Connector mounted on the Controller Front Panel (See Table B-6).

11.2.2 Engine Board Module Software

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Error Handler
5. Validation Suite
6. Deliverables

11.2.2.1 Operating System:

11.2.2.1.1 The Engine Board Module, when required by special provision, shall be supplied with Microware Embedded OS-9 Version 3.03 software and the following additional software:

1. Embedded OS-9 Real Time Kernel
2. Sequential Character File Manager (SCFMAN)
3. Sequential Protocol File Manager (SPFMAN)
4. Pipe File Manager (PIPEMAN)
5. Random Block File Manager (RBFMAN)
6. C Input Output Library (CIO)

11.2.2.1.2 Boot Image shall include the following utility modules:

break	data	deiniz	devs	free	copy
dir	tmode	edt	list	load	deldir
dump	del	ident	iniz	irqs	events
echo	kill	dcheck	cio	link	kermit
lmm	mdir	mfree	pd	mkdir	save
attr	rename	procs	unlink	sleep	xmode
shell	build	setime			

11.2.2.1.3 The OS-9 Operating System TICK Timer shall be derived from the edge transition of LINESYNC with a tick rate of 120 ticks per second.

11.2.2.1.4 The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's RBF Manager. The address of each memory block shall be specified by the manufacturer and provided with the documentation.

11.2.2.2 Drivers and Descriptors

11.2.2.2.1 Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

11.2.2.2.2 Drivers shall be provided to access the FLASH, SRAM, and DRAM memories through RBFMAN. The following RBFMAN descriptors shall apply:

/d0	Floppy Diskette Drive	Reserved name, no driver required.
/f0	FLASH Drive	Accessed as RAM disk, and OS9 /dd default device
/h0	Hard Disk Drive	Reserved name, no drive required.
/r0	SRAM Drive	Accessed as RAM disk.
/r1		Reserved name, no driver required.
/r2	Temporary DRAM Drive	Allows 1 MB DRAM, accessed as RAM disk; not initialized at boot time.

11.2.2.2.3 A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Access to the MC68360 internal timers shall be through SCFMAN using the following descriptors:

11.2.2.2.3.1 Descriptor names for each timer:

Timer1	= access to MC68360's internal timer #1
Timer2	= access to MC68360's internal timer #2
Timer3	= access to MC68360's internal timer #3
Timer4	= access to MC68360's internal timer #4
Timer12	= access to MC68360's internal timer #1 and #2 [cascaded]
Timer34	= access to MC68360's internal timer #3 and #4 [cascaded]

11.2.2.2.3.2 Timer descriptor option structure: The driver shall change appropriate timer functions only and ignore values that do not apply to a particular timer function. The data structure is as follows:

```
typedef struct {
    // Timer Global Configuration Register Related Options:
    rserveTGCR: 11; // Reserve bits (MSB)
    timerCAS: 1; // Cascade timers
    timerFRZ: 1; // Freeze
    timerSTP: 1; // Stop timer
    timerRST: 1; // Reset timer
    timerGM: 1; // Gate mode default = 0 (LSB)

    // Timer Mode Register Related Options:
    timerPS: 8; // Prescale value default = 0 (MSB)
    timerCE: 2; // Capture edge and default = 0
                // enable interrupts
    timerOM: 1; // Output mode default = 0
    timerORI: 1; // Output reference default = 0
                // interrupt enable
    timerFRR: 1; // Free Run or Restart default = 0
    timerICLK: 2; // Input Clock Source default = 1
    timerGE: 1; // Gate Enable; default = 0 (LSB)

    // Timer Reference Register
    U_INT16 timerTRR default = 0

    // Timer Capture Register
    U_INT16 timerTCR default = 0xFFFF

    // Timer Event Register
    reserveTER: 14; // Reserve (MSB)
    timerREF: 1; // Output reference event default = 1
    timerCAP: 1; // Capture event default = 1 (LSB)
} TTimer_opts;
```

11.2.2.2.3.3 Standard OS-9 SCFMAN Function Calls:

```
error_code _os_open (char *timer_desc_name, path_id *path);
error_code _os_close (path_id path);
error_code _os_gs_popt (path_id path, u_int32* sizeof(TTimer_opts), void *timer_opts);
error_code _os_ss_popt (path_id path, u_int32* sizeof(TTimer_opts), void *timer_opts);
error_code _os_write (path_id path, void *timer_value, 4);
error_code _os_read (path_id path, void *timer_value, 4)
```

11.2.2.2.3.4 The OS-9 SCFMAN shall provide access to the datakey and its control through the following descriptor name and OS-9 functions:

Descriptor name:

datakey = Interface Module Datakey

Function Calls:

```
error_code _os_open(char*datakey_desc_name, path_id*path);
error_code=E$NotRdy if Datakey is not installed
error_code _os_read(path_id path, void*control,128);
error_code=E$NotRdy if Datakey is not inserted
error_code _os_close(path_id path);
```

11.2.2.2.3.5 The async-communications serial device driver shall operate in six modes described below to accommodate communications network (EIA 232) and their associated flow control mode number (FCM #).

FCM#	Description
------	-------------

- 0) No Flow Control Mode: The CTS and CD signals are set asserted internally, so the serial device driver can receive data at all times. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. This is the default mode for the 170ATC controller. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode.
- 1) Manual Flow Control Mode: serial device driver transmits and receives data regardless the states of RTS, CTS, and CD. The user program has absolute control of the state of RTS and can inquire of the states of CTS and CD. The states of CTS and CD are set externally by a DCE. The device driver doesn't assert or de-assert the RTS.
- 2) Auto-CTS Flow Control Mode: The serial device driver transmits data when CTS is asserted. The state of CTS is controlled externally by a DCE. The user program has absolute control of the state of the RTS. The CD signal is set asserted internally. The device driver doesn't assert or de-assert the RTS.

- 3) Auto-RTS Flow Control Mode: The CTS and CD signals are set asserted internally, so the serial device driver can receive and transmit data at all time. Upon a write command, the serial device driver asserts RTS to start data transmission, and de-asserts RTS when data transmission is completed. If user program asserts the RTS, RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty. Parameters related to delays of the RTS turn-off after last character are user configurable.
- 4) Fully Automatic Flow Control Mode: The serial device driver receives data when CD is asserted. Upon a write command, the serial device driver asserts RTS and wait for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed. Parameters related to delays of RTS turn-off after last character are user configurable. If user program asserts the RTS, RTS remains to be on until user program de-asserts RTS. If user program de-asserts RTS before the transmitting buffer is empty, the driver holds RTS on until the transmitting buffer is empty.
- 5) Dynamic Flow Control Mode: The Serial device driver maintains a transmit buffer and a receive buffer with fixed sizes, controls the state of RTS and monitors the state of CTS. The transmission and reception of data are managed automatically by the serial device driver. The serial device driver transmits data when CTS is asserted. The serial device driver asserts RTS when its receiving buffer is filled below certain level (low watermark), and de-asserts RTS when its receiving buffer is filled above certain level (high watermark).

11.2.2.2.3.6 The serial device driver shall be able to accept user configuration commands to configure the device driver via OS9_os_ss_size() function call and to accept user request commands for status of serial port from the device driver via OS9_os_gs_size() function call.

The single 32-bit variable passed by _os_ss_size() is defined as follow:

a) Flow Control Code is SS_OFC (0x23):

<i>Bits</i>	<i>Description</i>
31-24	Auto RTS turn-off extension count in number of characters (range=0-255 1=default).
23-16	Reserved
15	Auto RTS turn-off extension timing (0=bps, 1=equivalent 1200 bps).
14-13	Reserve for Future Use (default=0).
12	Inhibit Change of SCC MRBLR for opened path (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR for opened path (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range=0-5).
7-0	Flow Control Code (FCC) =0x23

Note: The RTS turn-off extension can represent a bps rate independent time value rather a number of character times, (higher bps rates are normalized to equivalent 1200 bps characters) when selected by bit 15=1. Thus, a value of 4 represents the time of four characters at 1200 bps even when the actual rate is 9600. If bit 15=0, then an extension value = 4 represents 4 characters, which at a bps rate of 9600 would extend the RTS by approximately 3.3 ms.

b) Flow Control Code is SS_IFC (0x22):

<i>Bits</i>	<i>Description</i>
31-22	Flow Control Mode 5 high water mark value (range=1-1023; default=256).
21-12	Flow Control Mode 5 low water mark value (range=1-1023; default=256). Inhibit DCD activating control (default=0; 0=off; 1=on).
10	DCD flow control is active (default=0; 0=NO; 1=YES, changed by FCM#).
9-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC) = 0X22.

Note: The inhibit DCD selection has priority over the DCD ON request in the same access. Therefore, sending 0x000022 results in DCD inhibit and DCD Flow Control inactive for all Flow Modes. A new flow control mode number shall set DCD function to that required in the new mode unless DCD inhibit is ON.

c) Flow Control Code is SS-Ssig (0x1a):

<i>Bits</i>	<i>Description</i>
31-16	A signal number to be sent to calling process when the state of a pin is changed.
15-14	Reserved for Future Use (default=0).
13	Ring is asserted (capable hardware only).
12	CTS is de-asserted.
11	CTS is asserted.
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC) = 0x1a.

d) Flow Control Code is SS-DCmd (0x0d):

<i>Bits</i>	<i>Description</i>
31-15	Reserved for Future Use (default=0).
14	De-assert DTR (capable hardware only).
13	Assert DTR (capable hardware only).
12	De-assert RTS (duplicated function with <code>_os_ss_DsRTS()</code>);).
11	Assert RTS (duplicated function with <code>_os_ss_EnRTS()</code>);).
10-8	Reserved for Future Use (default=0).
7-0	Flow Control Code (FCC)=0x0d.

11.2.2.2.3.7 The single 32-bit variable returned by `_os_gs_size()` is defined as follows:

<i>Bits</i>	<i>Description</i>
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use (default=0).
10-8	Current Flow Control Mode Number (FCM#).
7	Reserved for Future Used (default=0).
6	Overrun error – 0=no error; 1=error on last received character.
5	Frame error – 0=no error; 1=error on last received character.
4	Parity error – 0=no error; 1=error on last received character.
3	Ring state – 0=de-asserted; 1=asserted (capable hardware only).
2	DSR state – 0=de-asserted; 1=asserted (capable hardware only).
1	DCD state – 0=de-asserted; 1=asserted.
0	CTS state – 0=de-asserted; 1=asserted.

11.2.2.2.3.8 Four input buffering modes shall be provided:

1. Line - characters are buffered up to and including a programmable termination character.
2. Fixed - a fixed specified number of characters are buffered by the driver.
3. Timed - characters are buffered until a programmable inter-character time-out occurs.
4. Raw - characters are unbuffered & delivered to the task as received.

- 11.2.2.2.3.9 Line, Fixed, and Timed Modes shall be capable of being used together. Raw mode shall disable all other buffering modes.
- 11.2.2.2.3.10 Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator
dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```
error_code _os_open (char *desc_name, path_id *path); //open descriptor for command
error_code _os_close (path_id path); //close descriptor
error_code _os_write (path_id path, void *value, 1); //set value or function
          *value = 1, turn led on or turn DLSclock feature on (default)
          *value = 0, turn led off or turn DLSclock feature off
error_code _os_read (path_id path, void *value, 1); //get current state
```

- 11.2.2.2.3.11 Time of Day (TOD) Clock -The OS-9 operating system's TOD Clock shall be driven by the LINESYNC derived OS-9 Operating System TICK Timer. The manufacturer shall provide the following features to support the TOD operation and synchronization.
 - 11.2.2.2.3.11.1 Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock/calendar shall automatically be adjusted to account for DST and leap years, tracking years 1997 through 2017. A SCFMAN driver shall be provided to enable/disable the automatic DST adjustment.
 - 11.2.2.2.3.11.2 Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be "ClockUpdate." Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.
 - 11.2.2.2.3.11.3 Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall by synchronized to a minimum of 10 ms resolution.

11.2.2.2.3.12 The FLASH RAM drive (/f0) shall be protected from corruption or re-initialization of the directory or data due to power failure during a SAVE or WRITE operation. The current sector of FLASH being written shall first be backed up (mirrored) in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy. A write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds. No more than 150 KB of SRAM shall be dedicated to this purpose.

11.2.2.3 Application Kernel

11.2.2.3.1 The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The initialization routines shall configure the serial port protocols as follows:

SP1 and SP2	1.2 Kbps, 8-bit word, 1 stop, no parity, no pause, no echo
SP3	153.6 Kbps
SP4	9.6 Kbps, 8-bit word, 1 stop, no parity, no pause
SP5	614.4 Kbps
SP6	38.4 Kbps, 8-bit word, 1 stop and no parity

11.2.2.3.2 Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 1.3 seconds.

11.2.2.3.3 A Trap Library routine, "Warmboot," shall be provided, which upon execution shall first shut down the OS-9 operating system, then jump to the start of the initialization routines executed on SYSRESET and proceed.

11.2.2.3.4 After initialization (boot up from SYSRESET), the program shall fork to the defined module in FLASH memory named OPEXEC preceded by a full path. If OPEXEC is not found or fails the program shall fork a shell. If OPEXEC is forked successfully, the program shall exit.

11.2.2.3.5 A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. A Short Out results in resumption of Application Software without an operating system reboot. The Contractor shall provide a documented method for the Application Software to recover from Level 7 IRQ (ACFAIL) without a SYSREST. A Long Out is defined as ACFAIL transition to LOW followed by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

11.2.2.4 Error Handler

11.2.2.4.1 Error handling routine to cope with initialization and power-up test anomalies shall be provided. Errors that occur during initialization and/or during power-up test shall produce a report.

11.2.2.4.2 The Error Handler shall respond to the following conditions and generate an Error Report (saved in Memory):

- 1 Timer initialization error
- 2 Timer power up test error
- 3 Serial communication port initialization error
- 4 Serial communication port power up test error
- 5 Peripheral component initialization error

11.2.2.4.3 The Error Handler error report shall contain, at a minimum, component identification and an error code to identify the form of the error. The error report shall be a file accessible through the Random Block File Manager and named "ErrorReport."

11.2.2.5 Validation Suite

11.2.2.5.1 A validation suite of software and associated documentation shall be provided. It shall include all diagnostic programs necessary to test all 170ATC Unit functions. The diagnostic programs shall demonstrate that all software and hardware functions operate in conformance to specified functionality. It shall provide a working example of how to program all functions

11.2.2.5.2 Validation suite software and associated documentation shall be segmented into individual test sequences. It shall be possible to separate out any one or group of these sequences and, with the addition of a general header file, execute it in isolation or in combination with application software.

11.2.2.5.3 When factory boot code is operating without the User "Opexec" started, the Validation Suite shall be invoked from the front panel keyboard, either as an execution in a continuous loop or by individual test selections.

- 11.2.2.5.4 The validation suite shall execute as a task of the OS-9 Shell Utilities and Commands module. Execution from the shell shall be by typing "Valsuite" from the prompt. If the User Program has been executed, the VALSUITE shall not execute any of its tests due to resource conflicts. It shall be possible to execute the following additional Engine Board Module specific commands while in the OS-9 Shell Utility:
1. Get/Set the hardware time of day clock
 2. Set OS-9 clock from hardware clock
 3. Read/write all I/O registers internal to the MC 68360
 4. Get/Set all programmable controls on serial ports
 5. Verify that the 120 Hz interrupt is functioning
 6. Set, configure, and read timers
 7. Observe time-out interrupts
- 11.2.2.5.5 The OS-9 Shell Utility shall communicate with the user through the SP4 Port (C50S Connector). When invoked, a low-priority task shall be executed for each SP port 1 and 2. Each task shall be configurable to use a different combination of input buffering options. The task shall open the port, configure it, and then enter a processing loop. In the loop, it shall wait for input and echo any input to the output. If no input is received for one second, an ASCII text string shall be sent out on the port. This text string shall be of the form "*port P hh:mm:ss.*" P is the port number and hh:mm:ss is the current OS-9 time stamp. The text shall be terminated with a carriage return followed by a line feed character.
- 11.2.2.6 Deliverables
- 11.2.2.6.1 A software package resident on the FLASH Memory shall be provided, including the Embedded OS-9 kernels, platform drivers, and a validation suite.
- 11.2.2.6.2 All software shall be delivered in the following forms:
1. Fully commented source code of contractor developed software (OS-9 not required)
 2. Microware Ultra-C Version 1.1 compatible linkable object code
 3. Memory map listing
- 11.2.2.6.3 Specific hardware memory addresses shall be specified and provided in a supplied INCLUDE FILE as defined constants. The INCLUDE FILE shall meet all applicable software delivery requirements.
- 11.2.2.6.4 Timer usage by drivers and their uninterrupted execution latencies, error values returned by driver calls, error codes, and a format of the error report file shall be documented.

- 11.2.2.6.5 Software to initialize and perform a power-up self-test of the Engine Board Module prior to the initialization of the OS-9 operating system shall be provided. All software components detailed in this specification or otherwise, and requiring initialization, shall be identified and the required initialization and nature of the test, documented. In addition, software provided to perform initialization and/or test shall be documented.
- 11.2.2.6.6 OS-9 compliant header files shall be provided with all Driver Modules.
- 11.2.2.7 Serial Communication Logic Circuitry
 - 11.2.2.7.1 System Serial Port 5 (SP5) EIA-485 signal lines shall be split into two multi-drop isolated ports. One shall be routed to the Interface Module's FIOC and the other routed to Connector C12S.
 - 11.2.2.7.2 System Serial Port 3 (SP3) signal lines shall be split into two multi-drop, isolated ports. One shall be routed to the C40 connector on the rear of the controller unit as an EIA-232, and the other routed to connector C12S as an EIA-485.
 - 11.2.2.7.3 LINE SYNC and POWER DOWN lines shall be split and isolated, one routed to the FIOC for shut down functions and the other changed to EIA-485; then routed to connector C12S for external module use.
 - 11.2.2.7.4 CPU RESET and POWER UP (SYSRESET) lines shall be isolated and "OR'd" to form NRESET. NRESET shall be used to reset FIOC and other module devices. NRESET shall also be converted to EIA-485 then routed to connector C12S.
 - 11.2.2.7.5 Isolation is between internal +5 VDC/Ground #1 and +12 VDC ISO/VDC Ground #2. +12 VDC ISO is for board power and external logic.
- 11.2.2.8 Buffers
 - 11.2.2.8.1 A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The Millisecond Counter (MC) shall be monitored for rollover. At each rollover transition (\$xxx FFFF - \$xxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the Engine Board Module upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer. The entry types are depicted as follows:

11.2.2.8.2 Input Transition Entry:

Description	msb							lsb	Byte Number
Transition Entry Identifier	S	Input Number							1
Timestamp NLSB	x	x	x	x	x	x	x	x	2
Timestamp LSB	x	x	x	x	x	x	x	x	3

11.2.2.8.3 Millisecond Counter Rollover Entry:

Description	msb							lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	3

11.2.2.9 I/O Functions

11.2.2.9.1 Inputs

11.2.2.9.1.1 Input scanning shall begin at I0 (bit 0) and proceed to the highest input, ascending from lsb to msb. Each complete input scan shall finish within 100 μ s. Once sampled, the logic state of an input shall be held until the next input scan.

11.2.2.9.1.2 Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1ms \pm 100 μ s. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 μ s of the completion of the input scan.

11.2.2.9.2 Data Filtering - If configured, the inputs shall be filtered by the FIOC to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	Enabled
On and off filter values shall be set to	5
Transition monitoring	Disabled (Timestamps are not logged)

11.2.2.9.3 Outputs - Simultaneous assertion of all outputs shall occur within 100 μ s. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FIOC continues to receive active communications from the Engine Board Module. If there is no valid communications with the Engine Board Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the FIOC status byte shall be updated to reflect the loss of communication from the Engine Board Module.

11.2.2.9.4 Standard Function - Each output shall be controlled by the data and control bits in the Engine Board Module-FIOC frame protocol as follows:

11.2.2.9.4.1 Output Bit Translation:

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

- 11.2.2.9.4.2 In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 μ s after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if previously OFF and if previously ON remain ON until otherwise configured. All outputs shall not glitch or change state unless configured to do so.
- 11.2.2.9.5 Interrupts
- 11.2.2.9.5.1 All interrupts shall be capable of asynchronous operation with respect to all processing and other interrupts.
- 11.2.2.9.5.2 Millisecond interrupt – This interrupt shall be activated by the 1 kHz reference once per millisecond. A timestamp rollover flag set by MC rollover shall be cleared only on command.
- 11.2.2.9.5.3 Linesync Interrupt - This interrupt shall be generated by both the 0-1 and 1-0 transitions of the LINESYNC signal. The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 kHz source for 0.5 seconds (≥ 60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 kHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥ 500 consecutive millisecond interrupts).
- 11.2.2.9.6 Communication Service Routine - A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically perform the following:
- 11.2.2.9.6.1 Transmitting:
1. Generate the opening and closing flags
 2. Generate the CRC value
 3. Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FIOC
 4. Provide zero bit insertion
- 11.2.2.9.6.2 Receiving:
1. Detect the opening and closing flags
 2. Provide address comparison, generating an interrupt for messages addressed to the I/O Module, and ignoring messages not addressed to the I/O Module
 3. Strip out inserted zeros
 4. Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
 5. Generate an interrupt if an abort sequence is received

- 11.2.2.9.7 Communication Processing - This task shall be to process the command messages received from the Engine Board Module, prepare, and start response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.
- 11.2.2.9.8 Input Processing - This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.
- 11.2.2.10 Data Communication Protocols
- 11.2.2.10.1 All communication with the Engine Board Module shall be SDLC-compatible command-response protocol, support 0-bit stuffing, and operate at a data rate of 614.4 Kbps.
- 11.2.2.10.1.1 The Engine Board Module shall always initiate the communication and should the command frame be incomplete or in error, no FIOC response shall be transmitted. The amount of bytes of a command or response is dependent upon the I/O Module identification.
- 11.2.2.10.1.2 The frame type shall be determined by the value of the first byte of the message. The command frames type values \$70 - \$7F and associated response frame type values \$F0 - \$FF are allocated to the Contractor diagnostics. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Module Command	I/O Module Response	Description	Minimum Message Time	Maximum Message Time
49	177	Request Module Status	250 μ s	275 μ s
50	178	MILLISECOND CTR. Mgmt.	222.5 μ s	237.5 μ s
51	179	Configure Inputs	344.5 μ s	6.8750 ms
52	180	Poll Raw Input Data	317.5 μ s	320 μ s
53	181	Poll Filtered Input Data	317.5 μ s	320 μ s
54	182	Poll Input Transition Buffer	300 μ s	10.25 ms
55	183	Command Outputs	405 μ s	410 μ s
56	184	Configure Input Tracking Functions	340 μ s	10.25 ms
57	185	Configure Complex Output Functions	340 μ s	6.875 ms
58	186	Configure Watchdog	222.5 μ s	222.5 μ s
59	187	Controller Identification	222.5 μ s	222.5 μ s
60	188	I/O Module Identification	222.5 μ s	222.5 μ s
61-62	189-190	Reserved (note below)		
63	191	Poll variable length raw input	317.5 μ s	320 μ s
64	192	Variable length command outputs	405 μ s	410 μ s

11.2.2.10.1.3 Notes for previous table - Messages 61/189 and 62/190 are for a future ITS Cabinet Monitor Unit and will be specified under ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (pending future Chapters 9 and 10). Message 63/191 shall be the same as Message 52/180 except Byte 2 of Message 180 response shall denote the following number of inputs bytes. Message 64/192 shall be the same as Message 55/183 except Byte 2 of the Message 55 Command shall denote the number of output data bytes along with the following output data.

11.2.2.10.2 Request Module Status – The command shall be used to request FIOC status information response. Command/response frames are as follows:

Request Module Status Command

Description	msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

11.2.2.10.2.1 The response status bits are defined as follows:

- P - Indicates FIOC hardware reset
- E - Indicates a communications loss of greater than 2 seconds
- M - Indicates an error with the MC interrupt
- L - Indicates an error in the LINESYNC
- W - Indicates that the FIOC has been reset by the Watchdog
- R - Indicates that the EIA-485 receive error count byte has rolled over
- T - Indicates that the EIA-485 transmit error count byte has rolled over
- K - Indicates the datakey has failed or is not present

11.2.2.10.2.2 Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When a count rolls over (255 - 0), its corresponding roll-over flag shall be set.

11.2.2.10.3

MC Management - This frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

Millisecond Counter Management Command

Description	msb								lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0	Byte 1	
New Timestamp MSB	x	X	x	X	x	x	x	x	Byte 2	
New Timestamp NMSB	x	X	x	X	x	x	x	x	Byte 3	
New Timestamp NLSB	x	X	x	X	x	x	x	x	Byte 4	
New Timestamp LSB	x	X	x	X	x	x	x	x	Byte 5	

Millisecond Counter Management Response

Description	msb								lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0	Byte 1	
Status	0	0	0	0	0	0	0	S	Byte 2	

11.2.2.10.4

Configure Inputs - The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb								lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1	Byte 1	
Number of Items (n)	n	N	n	N	n	n	n	n	Byte 2	
Item # - Byte 1	E	Input Number							Byte 3(l-1)+3	
Item # - Byte 2	Leading edge filter (e)								Byte 3(l-1)+4	
Item # - Byte 3	Trailing edge filter (r)								Byte 3(l-1)+5	

Configure Inputs Response

Description	msb								lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1	Byte 1	
Status	0	0	0	0	0	0	0	S	Byte 2	

Block field definitions shall be as follows:

- E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input
- e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)
- r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)
- S -return status S = '0' on completion or '1' on error

11.2.2.10.5 Poll Raw Input Data – The Poll Raw Input Data frame shall be used to poll the FIOC for the current unfiltered status of all inputs. The response frame shall contain 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	msb								lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0	Byte 1	

Poll Raw Input Data Response

Description	msb								lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0	Byte 1	
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2	
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16	
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17	
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18	
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19	
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20	

11.2.2.10.6 Poll Filtered Input Data – The Poll Filtered Input Data frame shall be used to poll the FIOC for the current filtered status of all inputs. The response frame shall contain 15 bytes of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	msb								lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1	Byte 1	

Poll Filter Input Data Response

Description	msb								lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1	Byte 1	
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x	Byte 2	
Inputs I8 to I119	x	x	x	x	x	x	x	x	Bytes 3 to 16	
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 17	
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 18	
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 19	
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 20	

11.2.2.10.7 Poll Input Transition Buffer – The Poll Input Transition Buffer frame shall poll the FIOC for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	msb								lsb	Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0		Byte 1
Block Number	x	x	x	X	x	X	x	x		Byte 2

Poll Input Transition Buffer Response

Description	msb								lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0		Byte 1
Block Number	x	x	x	X	x	X	x	x		Byte 2
Number of Entries	x	x	x	X	x	X	x	x		Byte 3
Item #	S	Input Number								Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	X	x	X	x	x		Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	X	x	X	x	x		Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G		Byte 3(I-1)+7
Timestamp MSB	x	x	x	X	x	X	x	X		Byte 3(I-1)+8
Timestamp NMSB	x	x	x	X	x	X	x	X		Byte 3(I-1)+9
Timestamp NLSB	x	x	x	X	x	X	x	X		Byte 3(I-1)+10
Timestamp LSB	x	x	x	X	x	X	x	X		Byte 3(I-1)+11

11.2.2.10.7.1 Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

- S - Indicates the state of the input after the transition
- C - Indicates the 255 entry buffer limit has been exceeded
- F - Indicates the 1024 buffer limit has been exceeded
- G - Indicates the requested block number is out of monotonic increment sequence
- E - Same block number requested, E is set in response

11.2.2.10.7.2 The Block Number byte is a monotonically increasing number incremented after each command issued by the Engine Board Module. When the FIOC receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the Engine Board Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

11.2.2.10.8 Set Outputs – The Set Outputs frame shall be used to command the FIOC to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the response frame shall be set to '1'. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set. Loss of LINESYNC reference shall also be indicated in system status information. The output bytes depend upon the FIOC. These command and response frames are as follows:

Set Outputs Command

Description	msb								lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1		Byte 1
Outputs O0 (lsb) to O7 (msb) Data	X	x	x	X	x	x	x	x		Byte 2
Outputs O8 to O103 Data	X	x	x	X	x	x	x	x		Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	X	x	x	X	x	x	x	x		Byte 15
Outputs O8 to O103 Control	X	x	x	X	x	x	x	x		Bytes 16 to 27

Set Outputs Response

Description	msb							lsb		Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1		Byte 1
Status	0	0	0	0	0	0	L	E		Byte 2

11.2.2.10.9 Configure Input Tracking Functions – The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to '1' and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb								lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0		Byte 1
Number of Items	Number of Items									Byte 2
Item # - Byte 1	E	Output Number								Byte 2(l-1)+3
Item # - Byte 2	I	Input Number								Byte 2(l-1)+4

Configure Input Tracking Functions Response

Description	msb								lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0		Byte 1
Status	0	0	0	0	0	0	0	V		Byte 2
Timestamp MSB	x	x	x	X	x	x	x	x		Byte 3
Timestamp NMSB	x	x	x	X	x	x	x	x		Byte 4
Timestamp NLSB	x	x	x	X	x	x	x	x		Byte 5
Timestamp LSB	x	x	x	X	x	x	x	x		Byte 6

11.2.2.10.9.1 Definitions are as follows:

- E = '1' - Enable input tracking functions for this output
- E = '0' - Disable input tracking functions for this output
- I = '1' - The output is OFF when input ON, ON when input OFF
- I = '0' - The output is ON when input ON, OFF when input is OFF
- V = '1' - The maximum number of 8 configurable outputs has been exceeded
- V = '0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

11.2.2.10.9.2 The timestamp value shall be sampled prior to the response frame. Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

- 11.2.2.10.9.3 The "Number of Item" field is valid from 0 to 16 (the maximum sent at one time is 8 'enables' and 8 'disables'). If processing a command results in more than 8 "Input Tracking functions" being enabled, none of the command shall be implemented and response message "V" bit will be set to '1'. If an invalid output or input number is specified for a function, the FIOC software shall take no action. The invalid number shall not be counted toward the maximum of 8 "Input Tracking functions" allowed. The rest of the message shall be processed. When an "Input Tracking function" is disabled, the output is set according to the most recently received "Set Outputs" command. When an "Input Tracking function" for an output is superseded (redefined as either another "Input Tracking function" or as a "Complex Output function") the output shall be ignored. The most recent value remains until changed by the new function.
- 11.2.2.10.10 Configure Complex Output Functions –This frame shall be used to specify a complex output from one to eight outputs. If a "Configure Complex Output Function" command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided: single pulse and continuous oscillation. These output forms shall be configurable to begin immediately or on a specified input trigger. In the case of continuous oscillation, the output form can be configured to continue until reconfigured or to oscillate only while 'gated active' by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	msb	lsb	Byte Number
(Type Number = 57)	0	0 1 1 1 0 0 1	Byte 1
Number of Items	Number of Items		Byte 2
Item # - Byte 1	0	Output Number	Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)		Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)		Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)		Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)		Byte 7(I-1)+7
Item # - Byte 6	0	Input Number	Byte 7(I-1)+8
Item # - Byte 7	P	W G E J F R L	Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb							lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp (MSB)	x	x	x	X	x	x	x	x	Byte 3
Timestamp (NMSB)	x	x	x	X	X	x	x	x	Byte 4
Timestamp (NLSB)	x	X	x	X	X	x	x	x	Byte 5
Timestamp (LSB)	x	X	x	X	X	x	x	x	Byte 6

11.2.2.10.10.1 The bit fields of the command frame are defined as follows:

- E = '1' - enable complex output function for this output
- E = '0' - disable complex output function for this output
- J = '1' - During the primary duration, the output shall be written as logic '1'.
During the secondary duration, the output shall be written as logic '0'.
- J = '0' - During the primary duration, the output shall be written as logic '0'.
During the secondary duration, the output shall be written as logic '1'.
- Output Number - 7-bit output number identifying outputs
- Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.
- Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.
- F = '1' - The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
- F = '0' - The trigger or gate shall be derived from the raw input.
- R = '1' - For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
- R = '0' - For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
- Input Number - 7-bit input number identifying inputs 0 Up.
- P = '1' - The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
- P = '0' - The output is configured for continuous oscillation.

W = '1' - It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
W = '0' - Operation shall begin within 2 ms of the command receipt.
G = '1' - Operation shall be gated active by the specified input.
G = '0' - Gating is inactive.
L = '1' - The LINESYNC based clock shall be used for the time ticks.
L = '0' - The MC shall be used for the time ticks.
V = '1' - Indicates the maximum number of configurable outputs is exceeded.
V = '0' - No error
Number of items - The number of entries in the frame. If 0, all outputs currently configured as "Complex Outputs" shall be disabled.

11.2.2.10.10.2 Controlling input signals shall be sampled at least once per millisecond.

11.2.2.10.10.3 The "Number of Items" field is valid from '0' (disable all "Complex Output functions") to '16' (maximum). The number of items sent at one time can be up to eight "enables" and eight "disables". If processing a command results in more than eight "Complex Output functions" being enabled, none of the command shall be implemented and the response message "V" bit shall be set to '1'. If an invalid output or invalid input number is specified for a function (the "G" or "W" bits being set to '1'), the FIOC software shall take no action. The invalid number shall not be counted towards the maximum of eight "Complex Output functions" allowed. The rest of the message shall be processed. When a "Complex Output function" is disabled, the output is set according to the most recently received "Set Outputs" command. When a "Complex Output function" for an output is superseded (redefined as either another "Complex Output function", or as an "Input Tracking function", the output shall be ignored. The most recent value remains until changed by the new function. The "G" bit (gating) set to '1' takes precedence over the "W" bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the "W" bit in the command message. If a "Complex Output function" is configured with the "G" bit set to 1 (gating) and the "P" bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state, thus terminating the oscillation (output inactive). For a single pulse operation ("G" bit set to '1'), after the secondary duration completes the "Complex Output function" shall be disabled, and the output shall be set according to the most recently received "Set Outputs" command.

- 11.2.2.10.11 Configure Watchdog – The Configure Watchdog frames shall be used to enable the software watchdog and to set its timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb								lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0	Byte 1	
Timeout Value	x	x	x	X	x	x	x	x	Byte 2	

Configure Watchdog Response

Description	msb								lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0	Byte 1	
Status	0	0	0	0	0	0	0	Y	Byte 2	

- 11.2.2.10.11.1 The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.
- 11.2.2.10.11.2 On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.
- 11.2.2.10.12 Controller Identification - This is a legacy message command/response for the FIOC with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FIOC shall test the presence of the Key. If absent, the FIOC Status Bit “K” shall be set and no interrogation shall take place. If an error occurs during the interrogation, bit “K” shall be set. If the “K” bit is set, only the first two bytes shall be returned. The command/response frames are as follows:

Controller Identification Command

Description	msb								lsb	Byte Number
(Type Number = 59)	0	0	1	1	1	0	1	1	Byte 1	

Controller Identification Response

Description	msb								lsb	Byte Number
(Type Number = 187)	1	0	1	1	1	0	1	1	Byte 1	
Status	0	0	0	0	0	0	0	K	Byte 2	
Datakey	x	x	x	x	x	x	x	x	Byte 3 to 130	

- 11.2.2.10.13 Module Identification – The FIOC identification command frame shall be used to request the FIOC identification value response of “1” for the 170ATC C1 and

“32 - 40” for future ITS cabinet SIUs and SMU/TMU. The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb								lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0	Byte 1	

I/O Module Identification Response

Description	msb								lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0	Byte 1	
FIOC Identification byte	x	x	x	X	X	x	x	x	Byte 2	

SECTION 3 - MODEL 170ATC-2 INTERFACE MODULE

- 11.3.1 **Interface Module Composition** - The Interface Module shall support the following electronics:
1. Communication system connection between the Engine Board Module and the Motherboard of the controller unit.
 2. Field I/O Interface between the Engine Board Module and the daughterboard via the Field I/O Controller (FIOC).
 3. +5VDC Standby Power.
 4. AC Power Line Monitor Circuitry.
- 11.3.2 **The physical size** of the Interface Module shall be equal to the Model 170 CPU Module. The pin out for the module shall be as called out in Table B-7, "Interface Module Pin Out".
- 11.3.3 **Datakey** - A Datakey Receptacle (KC4210, KC4210PCB or equal) with Key (DK1000 or equal) resident shall be provided and mounted on the Interface Module front plate.
- 11.3.3.1 Power shall not be applied to the Datakey receptacle if the Key is not resident.
- 11.3.3.2 The DATAKEY shall be tested, interrogated and all 128 addresses read using Software Interface.
- 11.3.4 **Field Input/Output Controller**
- 11.3.4.1 The Field Input/Output Controller (FIOC) shall be a microprocessor controller unit, together with all required clocking and support circuitry that will be capable of receiving control signals from the SCC3 of the MC68360 via the serial port of the FIOC. Input signals to the FIOC will be received from the Interface Module via the motherboard and daughterboard of the Model 170ATC Controller unit.
- 11.3.4.2 A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.
- 11.3.4.3 Upon NRESET going HIGH (FIOC active), the FIOC shall first read DATAKEY Address 128 DEC. If it reads "AA" Hex, the following is NOT required. If it reads NOT "AA", the FIOC shall output a state change on Output Port 5, bit 8 (Connector C1, pin 103 - Monitor Watchdog Timer Input) every 100 ms for 3.5 seconds or due to Engine Board Module Command.

- 11.3.4.4 A "ONE kHz REFERENCE" time reference capable of being synchronized shall be provided. It shall maintain a frequency accuracy of $\pm 0.01\%$ (± 0.1 counts per second).
- 11.3.4.5 A "32-bit MILLISECOND COUNTER" (MC) shall be provided for "timestamping". Each 1 kHz reference interrupt shall increment the MC.
- 11.3.4.6 At Power Up, the FIOC loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the "E" Bit and a subsequent set output command is processed.
- 11.3.4.7 A WATCHDOG Circuit shall be provided and shall be FIOC software enabled at power-up. Its enabled state shall be machine readable and reported in the FIOC status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FIOC. The watchdog circuit shall have a range of 100 ms to 1 second. Failure of the FIOC to reset the watchdog timer within the prescribed timeout shall result in hardware reset.
- 11.3.4.8 +5 VDC Standby Power - Standby power shall be provided to holdup system devices during Power Failure. It shall consist of the monitor circuitry, holdup capacitors, and charging circuitry. A charging circuit shall be provided that under normal operations, shall fully charge and float the capacitors consistent with manufacturer's recommendations. The capacitor power requirements are a minimum range of +5 to +2 VDC within 10 hours with a constant drain of 600 μ A. The associated CONTROL switch shall switch vertically with ON in UP position (when ON the +5 VDC is available to the load).
- 11.3.4.9 Monitor Circuitry - Monitor circuitry shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.
 - 11.3.4.9.1 The ACFAIL/POWER Output Lines shall go LOW (ground true) immediately upon Power Failure. The Lines shall transition to HIGH at Power Restoration. The lines shall be driven separately. The SYSRESET/POWERUP Output Lines shall transition to LOW 525 \pm 25 ms after ACFAIL/POWER DOWN transition to LOW. The Lines shall transition to HIGH 225 \pm 25 ms after Power Restoration and the supply is fully recovered. The Lines shall be driven separately.
 - 11.3.4.9.2 The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Restoration.

- 11.3.4.10 The 60 Hz Square Wave LINESYNC signal shall be generated by a crystal oscillator, which shall be synchronized to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal of +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and 50 \pm 1% duty cycle. The output shall have drive sink capability of 16 mA. A 2-Kohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line noise during normal operation.

SECTION 4 - MODEL 170ATC-3 FRONT PANEL ASSEMBLY

11.4.1 **The Model 170ATC-3 Front Panel Assembly (FPA)** shall consist of the following:

1. Metal Panel with latch assembly and two TSD #1 hinge attaching devices
2. FPA printed circuit board
3. FPA Controller
4. Keyboards
5. AUX and RESET switches
6. LCD Display
7. CPU Active LED Indicator
8. SP3 Active LED Indicator
9. External Serial Port SP3 Connector (Refer to Table B-5 for C12S Pin Assignment.)
10. External Serial Port SP4 Connector (Refer to Table B-8 for C50S Pin Assignment.)
11. Ethernet Serial Port SP1 Connector (Refer to Table B-6 C14S Pin Assignment and section 11.2.1.21 for Ethernet specification.)
12. Model 170ATC-1 Engine Board Module Connector (See Table B-11)

Four LED indicators labeled "TX", "RX", "COL (for TX Collision) and "LNK (for TX Status) shall also be provided. A Harness Interface and receptacle plug on the Engine Board Module shall be furnished with the FPA. (Refer to 11.2.1.22 and Table B-6.)

11.4.2 **Two Keyboards** shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 50 and 100 grams and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure. (See Table B-9 for Key Code.)

11.4.3 **The cathode** of the CPU Active Indicator shall be electrically connected to the CPU Activity LED signal and shall be pulled up to +5 VDC.

11.4.4 **The Display** shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control.

11.4.4.1 The LCD shall have eight lines of 40 characters each. Each character shall be composed of a 5 x 8 dot matrix and shall have minimum dimensions of 2.65 mm wide by 4.24 mm high. The viewing angle of the LCD shall be optimized for direct (90°) viewing, +35° vertical, ±45° horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

- 11.4.4.2 The Display shall have an electro-luminescent backlight. The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.
- 11.4.4.3 Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.
- 11.4.5 **The FPA Controller** shall function as the Front Panel Device controller interfacing with the CPU Module.
- 11.4.5.1 A FPA Reset Switch shall be provided on the Assembly PCB. The momentary Control switch shall be logic OR'd with the CPU Reset Line, producing a FPA Reset Output. Upon FPA Reset being active or receipt of a valid Soft Reset display command, the following shall occur:
1. Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.
 2. Each special character shall be set to ASCII SPC (space).
 3. The tab stops shall be set to columns 9, 17, 25, and 33.
 4. The backlight timeout value shall be set to 6 (60 seconds).
 5. The backlight shall be extinguished.
 6. The display shall be cleared (all ASCII SPC).
 7. The FPA module shall transmit the power up string "ESC [PU", hexadecimal value "1B 5B 50 55" through SP6 to the Engine Board Module once power is applied to the FPA or the FPA hardware "Reset" button is pushed.
- 11.4.5.2 When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.
- 11.4.5.3 Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 10 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.
- 11.4.5.4 When the AUX Switch is toggled, the appropriate AUX Switch code shown in Table B-10 shall be transmitted to the Engine Board Module.

- 11.4.5.5 The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the communication protocol in Section 9.3.10. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the lsb shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's is more than the number columns available on the LCD, the extra Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.
- 11.4.5.6 Character overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.
- 11.4.5.7 Auto-wrap shall turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.
- 11.4.5.8 Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.
- 11.4.5.9 Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 50% duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.
- 11.4.5.10 Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.
- 11.4.5.11 Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

- 11.4.5.12 Displayable characters shall be refreshed at least 20 times per second.
- 11.4.5.13 The Display backlight shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be selected by program command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.
- 11.4.5.14 When a display command code is received, the appropriate action shall be executed within 500 μ s.
- 11.4.5.15 The Command Codes shall use the following conventions:
1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:
 - Pn Value parameter, to be replaced by a value.
 - P1 An ordered and numbered parameter. One of a list of known parameters with a specified order and number. (Continues with P2, P3, etc.)
 - Px Display column number (1-40)
 - Py Display line (1-4)
 - ... Continue the list in the same fashion

Values of 'h' (\$68) and 'l' (\$6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).
 2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.
 3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).
- 11.4.5.16 The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.
- 11.4.5.17 The front panel printed circuit board shall house two Samtec SSW-125-01-G-D connectors, or equal, containing 50 pins each. The pin assignments shall be as listed in Table B-4.
- 11.4.6 **The Front Panel** shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output of 85 dB, for 250 ms upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

SECTION 5 - MODEL 170ATC-4 POWER SUPPLY MODULE

- 11.5.1 **General** - The Model 170ATC-4 Power Supply Module shall be an independent, self-contained module, vented, and cooled by convection only. The module shall slide into the Model 170ATC from the front of the controller chassis and be secured in place with appropriate hardware.
- 11.5.2 **Module Front** - An "On/Off" POWER Switch, +5VDC Standby Power CONTROL Switch, LED DC Power Indicator, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicator shall indicate that all required DC voltages meet the following conditions: the +5 VDC is within 5% and the 12 VDC is within 8% of their nominal levels.
- 11.5.3 **Input Protection** - Two 0.5 ohm, 10-watt wire-wound power resistors with a 0.2 μ H inductance shall be provided (one on the AC+ Line and one on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 μ F capacitor shall be placed between AC+ and AC- (between the resistor and arrestors).
- 11.5.4 **Power Supply Requirements**

Voltage	Tolerances	Minimum Current	Maximum Current
+5 VDC	± 0.25 VDC	1.0 AMP	2.0 AMP
+12 VDC Serial	± 0.5 VDC	0.1 AMP	1.5 AMP
-12 VDC Serial	± 0.5 VDC	0.1 AMP	0.5 AMP
+12 VDC	± 0.5 VDC	0.1 AMP	1.5 AMP

- 11.5.5 **Line Regulation** - Line regulation shall meet the above table tolerance values for a voltage range of 90 to 135 VAC rms at the stated maximum/minimum loads, including ripple noise.
- 11.5.6 **Load Regulation** - Load regulation shall meet the above table tolerance values for a voltage range of 90 to 135 VAC at 20 to 100% load for the +5 VDC or 50 to 100% load for +12 VDC Serial, -12 VDC Serial and +12 VDC, including ripple noise.
- 11.5.7 **Efficiency** - 70 % minimum
- 11.5.8 **Ripple & noise** - Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater.

- 11.5.9 **Voltage Overshoot** - no greater than 5%, all outputs
- 11.5.10 **Overvoltage Protection** - 130% of V_{out} for all outputs
- 11.5.11 **Overload** - Power foldback point 120% of maximum rated power.
- 11.5.12 **Short Circuit Protection** - Automatic recovery upon removal of fault.
- 11.5.13 **Inrush Current** - Cold Start Inrush shall be less than 25A at 115VAC.
- 11.5.14 **Transient response** - Output voltage back to within 1% in less than 500 μ s on a 50% load change. Peak transient not exceeding 5%.
- 11.5.15 **Holdup Time** - The power supply shall supply 30 watts minimum for 550 ms after ACFAIL transitions LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

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APPENDIX A

STATE TESTING PROCEDURES AND REQUIREMENTS

A.1 **Physical Testing**

- A.1.1 Evaluate capabilities of controller and auxiliary equipment for conformance to specifications.
- A.1.2 Visually inspect cabinet construction, size, and wire harnessing for conformance to specifications.
- A.1.3 Check equipment against physical inspection checklist for conformance to all requirements of specifications.

A.2 **Environmental Testing**

A.2.1 Equipment Required:

- A.2.1.1 Variable temperature chamber capable of simulating ambient temperatures of -34°C to 73°C, with recording temperature indicator
- A.2.1.2 Variable voltage source capable of supplying adequate AC power from 95 to 130 volts
- A.2.1.3 An electronic counter and recorder capable of accurately measuring and recording timed intervals
- A.2.1.4 A spike generator capable of producing positive and negative spikes with a peak amplitude of 300 volts (Spike characteristics shall consist of a fast-rising leading edge and a trailing edge decay time of 10 μ S.)
- A.2.1.5 A line voltage monitor for accurate indication of voltage settings
- A.2.1.6 A detector actuation simulator capable of developing vehicle and pedestrian actuations comparable to the requirements of intersection involved

A.2.2 Test Procedure:

- A.2.2.1 Place equipment, including cabinet, in test chambers and connect to power source.
- A.2.2.2 Connect detector simulator to phase inputs.
- A.2.2.3 Apply power and allow control to stabilize for 30 minutes.

- A.2.2.4 Connect recording voltmeter and spike generator to power source.
- A.2.2.5 Adjust detector simulator to correspond to traffic pattern.
- A.2.2.6 Check timing functions at extreme temperature and voltage limits and midpoints. Deviation for digital timing shall not be more than ± 100 ms from its set value at a power source frequency of 60 Hz.
- A.2.2.7 Test all auxiliary functions for proper operation.
- A.2.2.8 Test the signal conflict monitor for conformance to the monitor specifications and construction plans.
- A.2.2.9 Raise or lower temperature to extreme limits (-34°C to 73°C). Rate of temperature change will not exceed 16°C per hour.
- A.2.2.10 After reaching extreme temperatures, maintain operation for twelve hours with recording test equipment in operation.
- A.2.2.11 After 12 hours operation at each temperature extreme, remove equipment from chamber and analyze recordings.
- A.3 **Operational Testing**
- A.3.1 Equipment Required:
 - A.3.1.1 A load bank capable of developing load requirements of intersection involved
 - A.3.1.2 A detector simulator capable of simulating traffic patterns comparable to the intersection involved
- A.3.2 Test Procedure:
 - A.3.2.1 Set up controller in cabinet with all auxiliary equipment.
 - A.3.2.2 Connect detector simulator and pilot light monitors.
 - A.3.2.3 Connect load bank to all signal outputs.
 - A.3.2.4 Operate equipment under load, with detector actuations, for 72 hours. Visually monitor operation at random during test period.

APPENDIX B
TABLES

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Table B-1

**Model 208 Monitor
Connector Pin Assignments**

See 4.1.1.1

Connect Pin Number	Function	Termination
1	WDT LAMP (EXT)	
2	RELAY CIRCUIT COMMON	T2-4
3	N.C. RELAY CIRCUIT	
4	AC+	T2-4
5	Not used	
6	N.O. RELAY CIRCUIT	T2-5
7	Not used	
8	AC-	Internally wired in Output/PDA #3
9	Not used	
10	Not used	
11	Not used	
12	Not used	
13	+24 VDC	Internally wired in Output/PDA #3
14	Not used	
15	Not used	
16	Not used	
17	Not used	
18	WDT IN	C6-10
19	Not used	
20	Not used	
21	WDT EXT RESET	Internally wired in Output/PDA #3
22	DC GROUND	Internally wired in Output/PDA #3

Table B-2

**Model 210 Monitor
Connector Pin Assignments**

See 4.4.1

Pin	Function	Termination	Pin	Function	Termination
1	SP2 - Green	130	A	SP2 - Yellow	129
2	SP3 - Walk	115	B	SP8 - Green	136
3	SP8 - Yellow	135	C	SP9 - Walk	121
4	SP5 - Green	103	D	SP5 - Yellow	102
5	SP6 - Walk	106	E	SP11 - Green	109
6	SP11-Yellow	108	F	SP12 - Walk	112
7	SP7 - Green	133	H	SP7 - Yellow	132
8	T & B		J	SP1 - Green	127
9	SP1-Yellow	126	K	T & B	
10	SP10 - Green	124	L	SP10 - Yellow	123
11	T & B		M	SP4 - Green	118
12	SP4 - Yellow	117	N	T & B	
13	ASP1 - Green	A123	P	NC	-----
14	NC	-----	R	ASP2 - Green	A126
15	T & B		S	ASP4 - Green	A116
16	T & B		T	NC	-----
17	NC	-----	U	T & B	
18	T & B		V	ASP5 - Green	A103
19	NC	-----	W	NC	-----
20	EQ GND	TB 01-9	X	NC	-----
21	AC -	TB 01-10	Y	DC GND	TB 02-2
22	WATCHDOG	C 4-37	Z	EXT. RESET	TB 02-5
23	+ 24 VDC	TB 02-1	AA	T & B	
24	INTERLOCK	LR Coil	BB	STOP TIME	TB 02-3
25	INTERLOCK	TB 02-2	CC	NC	-----
26	NC	-----	DD	NC	-----
27	NC	-----	EE	CLAPPER	TB 01-12
28	NORM. CLOSED	TB 01-11	FF	AC +	TB01-11

ASP = Auxiliary Output File Switch Pack Position
 SP = Output File Switch Pack Position
 T & B = Connect conductor to pin 0.6 m in length with ring connector on free end.
 Bundle and tie conductors separately.

Table B-3

**Model 210 Monitor Program Card
Channel Assignments**

See 4.4.2

Program Card Channel	Monitor Connector Pin	Switch Pack Position	Program Card Channel	Monitor Connector Pin	Switch Pack Position
1	J	SP1 - Green	9	13	ASP1 - Green
1	9	SP1 - Yellow	9	16	T & B
2	1	SP2 - Green	10	R	ASP2 - Green
2	A	SP2 - Yellow	10	U	T & B
3	M	SP4 - Green	11	S	ASP4 - Green
3	12	SP4 - Yellow	11	15	T & B
4	4	SP5 - Green	12	V	ASP5 - Green
4	D	SP5 - Yellow	12	18	T & B
5	7	SP7 - Green	13	2	SP3 - Walk/Green
5	H	SP7 - Yellow	13	8	T & B
6	B	SP8 - Green	14	5	SP6 - Walk/Green
6	3	SP8 - Yellow	14	11	T & B
7	10	SP10 - Green	15	C	SP9 - Walk/Green
7	L	SP10 - Yellow	15	K	T & B
8	E	SP11 - Green	16	F	SP12 - Walk/Green
8	6	SP11 - Yellow	16	N	T & B

ASP = Auxiliary Output File Switch Pack Position
 SP = Output File Switch Pack Position
 T & B = Connect conductor to pin 0.6 m in length with ring connector on free end. Bundle and tie conductors separately.

Table B-4

Model 170ATC-1 Engine Board Module
Samtec SSW-125-01-G-D Connector Pin Assignment
 See 11.2.1.11 and 11.4.5.17

Pins	Functions	Pins	Functions	Pins	Functions	Pins	Functions
J1-1	0 VCC	J1-26	SMC2_SP4_RXD	J2-1	VSTDBY_5.0V_IN	J2-26	SP8_TXC_INT
J1-2	0 VCC	J1-27	SMC1_SP6_TXD	J2-2	VSTDBY_3.3V_IN	J2-27	SP8_RXC_EXT
J1-3	0 VCC	J1-28	SMC1_SP6_RXD	J2-3	RESERVED	J2-28	CPURESET
J1-4	0 VCC	J1-29	CPU ACTIVE LED	J2-4	RESERVED	J2-29	LINESYNC
J1-5	GND	J1-30	10BASET_P	J2-5	SCC2_SP2_TXD	J2-30	PWRDWN/ACFAIL
J1-6	GND	J1-31	10BASET_TN	J2-6	SCC2_SP2_RXD	J2-31	PWRUP/SYSRESET
J1-7	GND	J1-32	10BASET_RP	J2-7	SCC2_SP2_RTS	J2-32	SP1_MDSI
J1-8	GND	J1-33	10BASET_RN	J2-8	SCC2_SP2_CTS	J2-33	SP1_MISD
J1-9	SP1_TXD	J1-34	ETHERNET_LED_TXD	J2-9	SCC2_SP2_CD	J2-34	SP1_CLK
J1-10	SP1_RXD	J1-35	ETHERNET_LED_RXD	J2-10	SCC2_SP2_TXC_INT	J2-35	SP1_SEL
J1-11	SP1_RTS	J1-36	ETHERNET_LED_CLSN	J2-11	SCC2_SP2_RXC_EXT	J2-36	RESERVED
J1-12	SP1_CTS	J1-37	ETHERNET_LED_LINK	J2-12	SCC2_SP2_RXC_EXT	J2-37	RESERVED
J1-13	SP1_CD	J1-38	SYSCLK_DIV_4	J2-13	SCC3_SP5_TXD	J2-38	RESERVED
J1-14	SP1_TXC_INT	J1-39	RESERVED	J2-14	SCC3_SP5_RXD	J2-39	RESERVED
J1-15	SP1_TXC_EXT	J1-40	RESERVED	J2-15	SCC3_SP5_TXC_INT	J2-40	RESERVED
J1-16	SP1_RXC_EXT	J1-41	RESERVED	J2-16	SCC3_SP5_RXC_EXT	J2-41	RESERVED
J1-17	SCC4_SP3_TXD	J1-42	RESERVED	J2-17	RESERVED	J2-42	RESERVED
J1-18	SCC4_SP3_RXD	J1-43	RESERVED	J2-18	RESERVED	J2-43	RESERVED
J1-19	SCC4_SP3_RTS	J1-44	RESERVED	J2-19	RESERVED	J2-44	BDMDS
J1-20	SCC4_SP3_CTS	J1-45	RESERVED	J2-20	RESERVED	J2-45	BDMBERR
J1-21	SCC4_SP3_CD	J1-46	RESERVED	J2-21	SP8_TXD	J2-46	BDMBKPT
J1-22	SCC4_SP3_TXC_INT	J1-47	BRG_MDSI	J2-22	SP8_RXD	J2-47	BDMFRZ
J1-23	SCC4_SP3_TXC_EXT	J1-48	BRG_MISD	J2-23	SP8_RTS	J2-48	BDMRST
J1-24	SCC4_SP3_RXC_EXT	J1-49	BRG_SCK	J2-24	SP8_CTS	J2-49	BDMIFTC
J1-25	SMC2_SP4_TXD	J1-50	VCC_REST	J2-25	SP8_CD	J2-50	BDMIPED

Table B-5

**Model 170ATC-3 Front Panel Assembly
C12S Pin Assignment**

See 11.2.1.16

Pin	Function	Pin	Function
1	TX5 DATA +	14	TX5 DATA -
2	RX5 DATA +	15	RX5 DATA -
3	TX5 CLOCK +	16	TX5 CLOCK -
4	RX5 CLOCK +	17	RX5 CLOCK -
5	TX3 DATA +	18	TX3 DATA -
6	RX3 DATA +	19	RX3 DATA -
7	TX3 CLOCK +	20	TX3 CLOCK -
8	RX3 CLOCK +	21	RX3 CLOCK -
9	LINE SYNC +	22	LINE SYNC -
10	NRESET +	23	NRESET -
11	POWER DOWN +	24	POWER DOWN -
12	+5 VDC	25	Equipment GND
13	DC GND #2	26	FUNCTION

Table B-6

**Model 170ATC-3 Front Panel Assembly
C14S Pin Assignment (Ethernet)**

See 11.2.1.21

Pin	Function	Pin	Function
1	TX +	5	NA
2	TX -	6	RX-
3	RX +	7	NA
4	NA	8	NA

Table B-7 – Model 170ATC-2 Interface Module Pin Assignment See 11.3.2

Pin Number	Description	Pin Number	Description
1	DOUT2	2	DOUT3
3	CTS2	4	CTS3
5	DIN2	6	DIN3
7	RTS2	8	RTS3
9	CD2	10	CE3
11	CD1	12	CD4
13	ATS1	14	ATS4
15	DIN1	16	DIN4
17	CTS1	18	CTS4
19	DOUT1	20	DOUT4
21	SPR	22	LSYNC
23	PDN	24	PUP
25	VSB	26	VSB
57	ISO 5V	27	SPR
58	ISO 5V	28	SPR
59	ISO GND	29	SPR
60	ISO GND	30	SPR
61	+12 V ISO	31	SPR
62	+12 V ISO	32	SPR
63	32 kHz	33	SPR
64	60 Hz	34	SPR
65	RSTT	35	SPR
66	DTA/T-0	36	SPR
67	NMI RST	37	SPR
68	TSTCMP	38	SPR
69	CS4	39	SPR
70	CS3	40	SPR
71	IRQ	41	SPR
72	IO/RW	42	SPR
73	IO/1-A	43	SPR
74	I/O RESET 1	44	SPR
75	AA3	45	SPR
76	AA2	46	SPR
77	AA1	47	SPR
78	AA0	48	SPR
79	D107	49	SPR
80	D106	50	SPR
81	D105	51	SPR
82	D104	52	SPR
83	D103	53	SPR
84	D102	54	SPR
85	D101	55	RESET
86	D100	56	R/W-
87	+12 V	88	+12 V
89	-12 V	90	-12 V
91	SPR	92	SPR
93	+5 V	94	+5 V
95	+5 V	96	+5 V
97	GND	98	GND
99	GND	100	GND

Table B-8

**Model 170ATC-3 Front Panel Assembly
C50 Pin Assignment**

See 11.4.1

Pin	Function
1	NA
2	SP4 RX
3	SP4 TX
4	NA
5	DC GROUND #1
6	NA
7	NA
8	NA
9	NA

Table B-9

Model 170ATC-3 Front Panel Assembly

Key Code

See 11.4.2

Key	ASCII Data (Text)	ASCII Data (Hex)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
(UP ARROW)	ESC [A	1B 5B 41
(DOWN ARROW)	ESC [B	1B 5B 42
(RIGHT ARROW)	ESC [C	1B 5B 43
(LEFT ARROW)	ESC [D	1B 5B 44
ESC	ESC O S	1B 5B 53
NEXT	ESC O P	1B 5B 50
YES	ESC O Q	1B 5B 51
NO	ESC O R	1B 5B 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

Table B-10

Model 170ATC Auxiliary Switch

See 11.4.5.4

Switch	ASCII Data (Text)	ASCII Data (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

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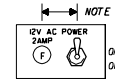
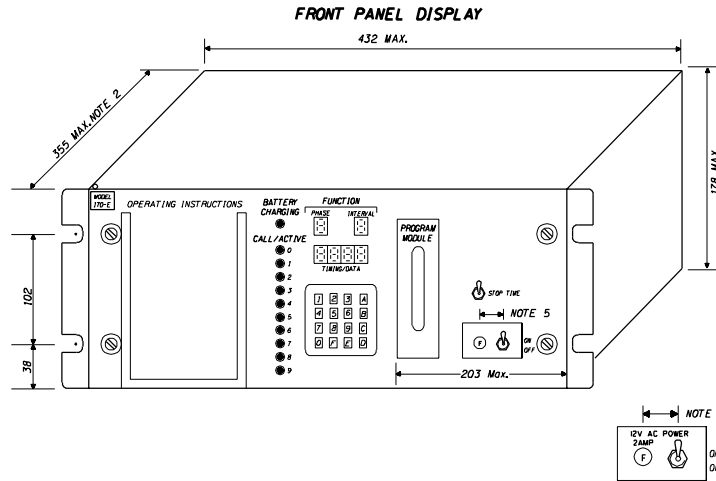
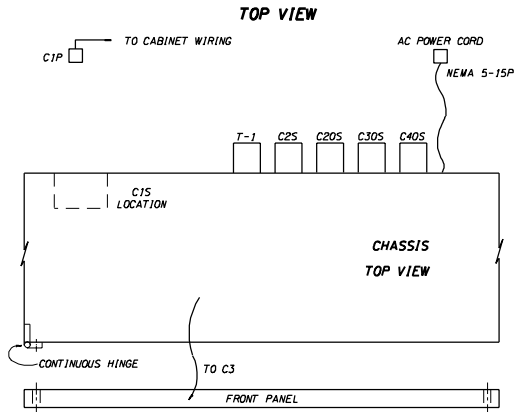


APPENDIX C
PLANS

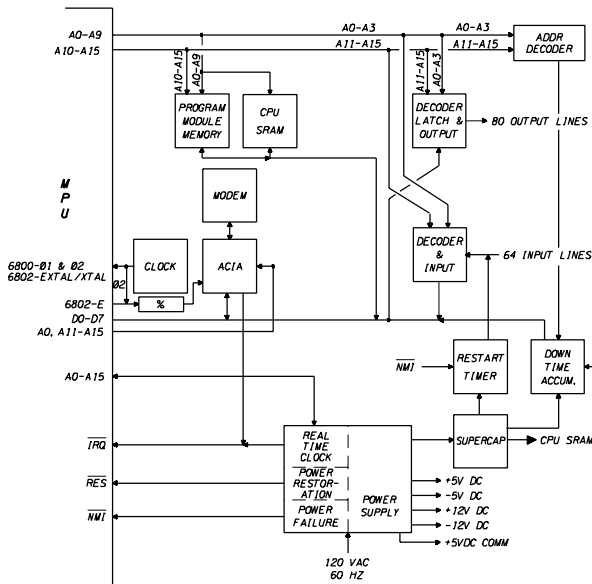
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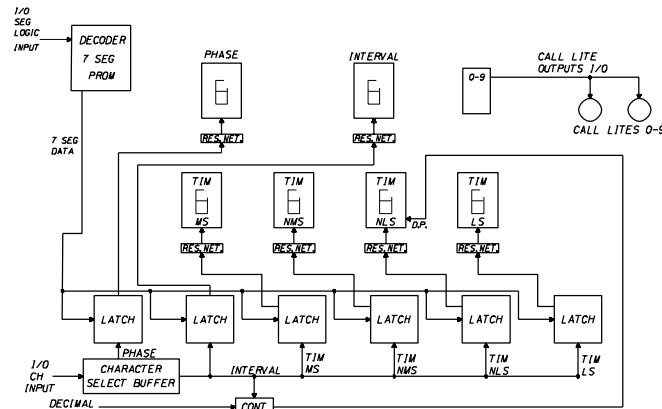
TYPICAL MODEL 170-E CONTROLLER UNIT



ORGANIZATION OF MODEL 170-E CONTROLLER UNIT BLOCK DIAGRAM



FRONT PANEL DISPLAY BLOCK DIAGRAM



NOTES:

1. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (mm).
2. CONNECTOR C1S SHALL BE MOUNTED ON THE RIGHT REAR OF THE CHASSIS. THE 35 mm DEPTH AND 178 mm HEIGHT MAXIMUM DIMENSIONS SHALL INCLUDE THE MALE CONNECTOR CIP WITH "T" HANDLE AND THE C2 CONNECTOR.
3. THE PROGRAM MODULE OPENING ON FRONT PANEL SHALL BE A MINIMUM OF 38.6 mm HORIZONTALLY AND 127.5 mm VERTICALLY FOR MODULE CLEARANCE.
4. THE TYPICAL FRONT PANEL LABELING SHALL BE AS SHOWN.
5. THE FUSE HOLDER AND ON/OFF SWITCH SHALL BE A MINIMUM OF 25 mm FROM CENTER TO CENTER.

MODEL 170-E CONTROLLER UNIT

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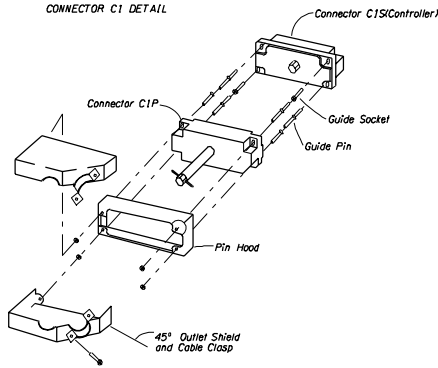
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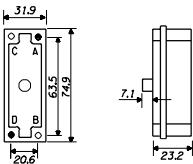
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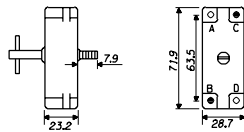
CONNECTOR C1 DETAIL



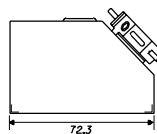
CONNECTOR C1S



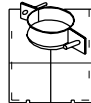
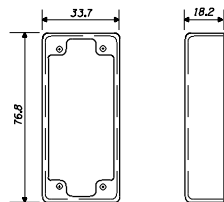
CONNECTOR C1P



SHIELD FOR C1P



HOOD FOR C1P



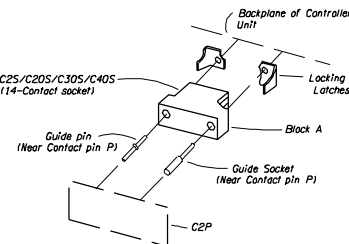
OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

OUTPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	OUTPUT PORT ADDRESS	BIT	CONNECTOR C3 SOCKET CONTACTS
5001	1	2	5006	1	83
5001	2	3	5006	2	84
5001	3	4	5006	3	85
5001	4	5	5006	4	86
5001	5	6	5006	5	87
5001	6	7	5006	6	88
5001	7	8	5006	7	89
5001	8	9	5006	8	90
5002	1	10	5007	1	91
5002	2	11	5007	2	93
5002	3	12	5007	3	94
5002	4	13	5007	4	95
5002	5	15	5007	5	96
5002	6	16	5007	6	97
5002	7	17	5007	7	98
5002	8	18	5007	8	99
5003	1	19	5008	1	CC-PHASE
5003	2	20	5008	2	CC-INTERVAL
5003	3	21	5008	3	CC-TIMING LS
5003	4	22	5008	4	CC-TIMING NLS
5003	5	23	5008	5	CC-TIMING MWS
5003	6	24	5008	6	CC-TIMING MS
5003	7	25	5008	7	CALL LT8
5003	8	26	5008	8	CALL LT9
5004	1	27	5009	1	CH-LS
5004	2	28	5009	2	CH-NLS
5004	3	29	5009	3	CH-MWS
5004	4	30	5009	4	CH-MS
5004	5	31	5009	5	DP
5004	6	32	5009	6	BL-P&I
5004	7	33	5009	7	BL-TIMING
5004	8	34	5009	8	NA
5005	1	35	500A	1	CALL LT0
5005	2	36	500A	2	CALL LT1
5005	3	37	500A	3	CALL LT2
5005	4	38	500A	4	CALL LT3
5005	5	100	500A	5	CALL LT4
5005	6	101	500A	6	CALL LT5
5005	7	102	500A	7	CALL LT6
5005	8	103	500A	8	CALL LT7

CONNECTOR C2/C20/C30/C40 SOCKET ASSIGNMENT

Socket Contacts	Function	Socket Contacts	Function
A	Audio IN	J	RTS
B	Audio IN	K	Data IN
C	Audio OUT	L	Data Out
D	+5VDC	M	CTS
E	Audio OUT	N	DC GND.
F	-5VDC	P	NA
H	CD	R	NA

CONNECTOR C2/C20/C30/C40 DETAIL



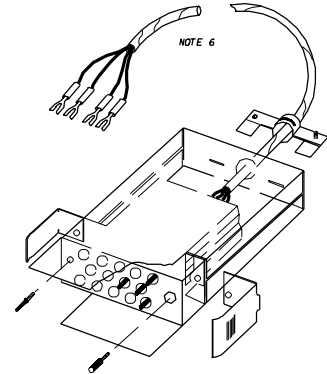
INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

INPUT PORT ADDRESS	BIT	CONNECTOR C1 SOCKET CONTACTS	INPUT PORT ADDRESS	BIT	CONNECTOR C3 SOCKET CONTACTS
5001	1	39	5005	1	67
5001	2	40	5005	2	68
5001	3	41	5005	3	69
5001	4	42	5005	4	70
5001	5	43	5005	5	71
5001	6	44	5005	6	72
5001	7	45	5005	7	73
5001	8	46	5005	8	74
5002	1	47	5006	1	75
5002	2	48	5006	2	76
5002	3	49	5006	3	77
5002	4	50	5006	4	78
5002	5	51	5006	5	79
5002	6	52	5006	6	80
5002	7	53	5006	7	81
5002	8	54	5006	8	82
5003	1	55	5007	1	NA
5003	2	56	5007	2	NA
5003	3	57	5007	3	NA
5003	4	58	5007	4	NA
5003	5	59	5007	5	NA
5003	6	60	5007	6	NA
5003	7	61	5007	7	NA
5003	8	62	5007	8	NA
5004	1	NA	5008	1	NA
5004	2	NA	5008	2	NA
5004	3	NA	5008	3	NA
5004	4	NA	5008	4	NA
5004	5	63	5008	5	NA
5004	6	64	5008	6	NA
5004	7	65	5008	7	NA
5004	8	66	5008	8	NA

TERMINAL BLOCK T-1 ASSIGNMENT

1. Audio IN	6. CTS
2. Audio IN	7. Data Out
3. CD	8. Audio Out
4. RTS	9. Audio Out
5. Data IN	10. DC GND.

C2P MODEM INTERCONNECT HARNESS



C2P CONNECTOR ASSIGNMENT

PIN	FUNCTION	WIRE COLOR
A	AUDIO IN	WHITE
B	AUDIO IN	BLACK
C	AUDIO OUT	RED
E	AUDIO OUT	GREEN

NOTES:

- ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).
- C1 CONNECTOR PINS 1, 14, 92, AND 104 SHALL BE CONNECTED TO THE CONTROLLER UNIT DC LOGIC GROUND.
- PROVIDE CLEARANCE FOR C1P WITH HOOD WHEN MOUNTING TO CONNECTOR C1S ON THE I70 CONTROLLER UNIT.
- THE DARKER CIRCLES IN THE C1S AND C1P CONNECTOR DETAILS DENOTE GUIDE PIN LOCATIONS AND THE OPEN CIRCLES DENOTE GUIDE SOCKET LOCATIONS ON THE MATING SURFACES OF THE C1S AND C1P. CORNER GUIDES FOR THE C1S, PINS A AND D, SOCKETS B AND C, CORNER GUIDES FOR THE C1P, PINS B AND C, SOCKETS A AND D.
- ALL FUNCTIONS UNDER CONNECTOR C2 AND TERMINAL BLOCK T-1 ARE IN REFERENCE TO THE MODEM.
- CABLE LENGTH SHALL BE 1 METER MINIMUM.
- SHEET DEFINITIONS.

- BL = BLANKING
- CC = CHARACTER CONTROL OR STROBE
- CD = CARRIER DETECT
- CH = CHARACTER
- CTS = CLEAR TO SEND
- DP = DECIMAL POINT
- LS = LEAST SIGNIFICANT
- MS = MOST SIGNIFICANT
- NA = PRESENTLY NOT ASSIGNED, CANNOT BE USED BY THE CONTRACTOR FOR OTHER PURPOSES.
- NLS = NEXT LEAST SIGNIFICANT
- NWS = NEXT MOST SIGNIFICANT
- P&I = PHASE AND INTERVAL
- RTS = REQUEST TO SEND

MODEL 170-E CONTROLLER UNIT

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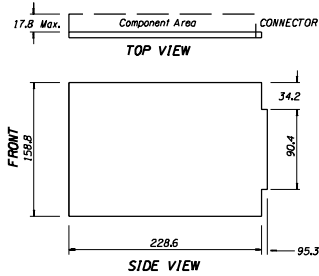
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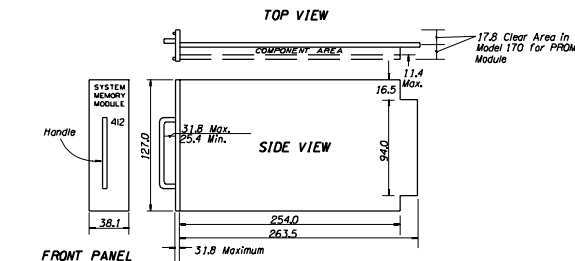
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MODEL 400 MODEM



MODEL 412 PROM MODULE

COMPONENT SIDE		CIRCUIT SIDE	
CONTACT	MODEL 400 FUNCTION	CONTACT	MODEL 400 FUNCTION
1	NA	A	DC GROUND
2	AUDIO INPUT	B	DC GROUND
3	AUDIO INPUT	C	12 VDC
4	NA	D	12 VDC
5	NA	E	-12 VDC
6	NA	F	-12 VDC
7	NA	H	NA
8	NA	J	NA
9	NA	K	CARRIER DETECT
10	NA	L	REQUEST TO SEND
11	NA	M	DATA INPUT
12	NA	N	CLEAR TO SEND
13	NA	P	DATA OUTPUT
14	NA	R	NA
15	NA	S	NA
16	NA	T	NA
17	NA	U	NA
18	NA	V	NA
19	NA	W	NA
20	NA	X	AUDIO OUTPUT
21	NA	Y	AUDIO OUTPUT
22	NA	Z	NA

MODEL 400 MODEM CONNECTOR ASSIGNMENT

NOTES:

1. ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).
2. PROGRAM MODULE'S HEIGHT AND WIDTH DIMENSIONS ARE MAXIMUM.

CIRCUIT ASSIGNMENTS FOR MODEL 412 PROM MODULE CONNECTOR

CIRCUIT SIDE		COMPONENT SIDE	
A0	1	2	A1
A2	3	4	A3
A4	5	6	A5
A6	7	8	A7
A8	9	10	A9
A10	11	12	A11
A12	13	14	A13
A14	15	16	A15
DD	17	18	DT
D2	19	20	D3
DF	21	22	DS
DS	23	24	DT
VMA/02	25	26	RST
Read/Write	27	28	Unassigned
Unassigned	29	30	Unassigned
Unassigned	31	32	Unassigned
Unassigned	33	34	Equipment Ground
Unassigned	35	36	Unassigned
Unassigned	37	38	Unassigned
Unassigned	39	40	Unassigned
Unassigned	41	42	Unassigned
Unassigned	43	44	Unassigned
Unassigned	45	46	Unassigned
Unassigned	47	48	Unassigned
Unassigned	49	50	Unassigned
Unassigned	51	52	Unassigned
Unassigned	53	54	Unassigned
Unassigned	55	56	Unassigned
Unassigned	57	58	Unassigned
+12VDC	59	60	+15VDC
-12VDC	61	62	-12VDC
-5VDC	63	64	-5VDC
+5VDC	65	66	+5VDC
+5VDC	67	68	+5VDC
GND	69	70	GND
GND	71	72	GND

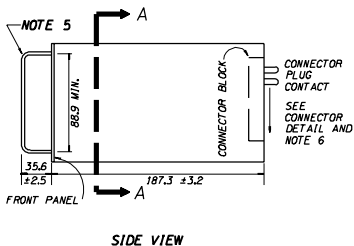
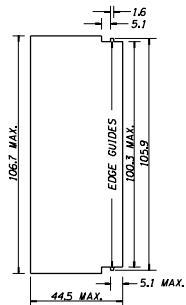
MODEL 400 MODEM AND 412 PROM MODULE CONNECTOR ASSIGNMENTS

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MODEL 200 AND 204 PHYSICAL DETAILS

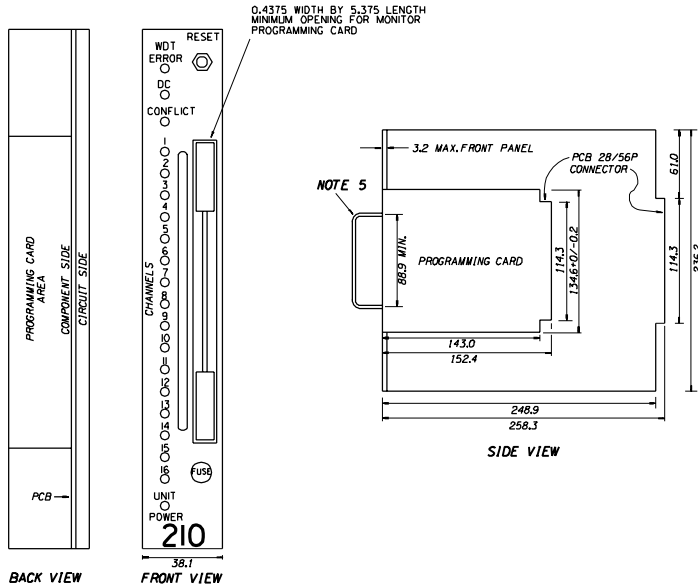


CROSS SECTION A-A

MODEL 200 AND 204 CONNECTOR DETAIL

MODEL 200		MODEL 204	
PIN	FUNCTION	PIN	FUNCTION
1	AC+	7	Load Circuit #1
2	Equip. Ground	8	Load Circuit #2
3	Red Output	9	Equip. Ground
4	Not Assigned	10	AC-
5	Yellow Output	11	AC+
6	Red Input	12	Not Assigned
7	Green Output		
8	Yellow Input		
9	+ 24VDC		
10	Green Input		
11	Not Assigned		
12	Not Assigned		

TYPICAL MODEL 210 MONITOR UNIT



MODEL 210 CONFLICT MONITOR CONNECTOR PIN ASSIGNMENTS

Connector Pin No.	Termination	Connector Pin No.	Termination
1	SP2-Green	A	SP2-Yellow
2	SP3-Walk	B	SP8-Green
3	SP8-Yellow	C	SP9-Walk
4	SP5-Green	D	SP5-Yellow
5	SP6-Walk	E	SP11-Green
6	SP11-Yellow	F	SP12-Walk
7	SP1-Green	H	SP7-Yellow
8	T & B	J	SP1-Green
9	SP1-Yellow	K	T & B
10	SP10-Green	L	SP10-Yellow
11	T & B	M	SP4-Green
12	SP4-Yellow	N	T & B
13	ASP1-Green	P	NA
14	NA	R	ASP2-Green
15	T & B	S	ASP4-Green
16	T & B	T	NA
17	NA	U	T & B
18	T & B	V	ASP5-Green
19	NA	W	ASP5-Green
20	Equip Grd (TB01-9)	X	NA
21	AC- (TB01-10)	Y	DC Ground (TB02-2)
22	Watchdog Timer (C4-37)	Z	Equip Riser (TB02-5)
23	+24 VDC (TB02-1)		T & B
24	Interlock Circuit (Logic Relay Coil)	BB	Slop Time (TB02-3)
25	Interlock Circuit-DC Grd (TB02-2)	CC	NA
26	NA	DD	NA
27	NA	EE	Output-MC2 Coil (TB01-12)
28	Output-AC+ (TB01-11)	FF	AC+ (TB01-11)

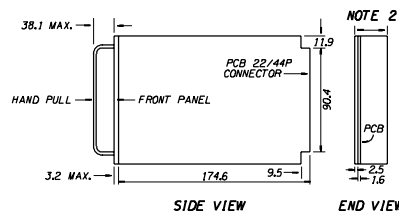
ASP = Auxiliary Output File Switch Pack Position
 SP = Output File Switch Pack Position
 T & B = Connect conductor to pin two feet in length with ring connector on free end. Bundle and the conductors separately.

MODEL 210 CONFLICT MONITOR CHANNEL ASSIGNMENTS

Program Card Channel	Monitor Connector Pin	Switch Pack Position	Program Card Channel	Monitor Connector Pin	Switch Pack Position
1	J	SP1 - Green	9	13	ASP1 - Green
1	J	SP1 - Yellow	9	16	T & B
2	A	SP2 - Green	10	R	ASP2 - Green
2	A	SP2 - Yellow	10	U	T & B
3	M	SP4 - Green	11	S	ASP4 - Green
3	M	SP4 - Yellow	11	15	T & B
4	D	SP5 - Green	12	V	ASP5 - Green
4	D	SP5 - Yellow	12	18	T & B
5	7	SP7 - Green	13	2	SP3 - Walk
5	H	SP7 - Yellow	13	8	T & B
6	B	SP8 - Green	14	5	SP6 - Walk
6	3	SP8 - Yellow	14	11	T & B
7	10	SP10 - Green	15	C	SP9 - Walk
7	L	SP10 - Yellow	15	K	T & B
8	E	SP11 - Green	16	F	SP12 - Walk
8	6	SP11 - Yellow	16	N	T & B

ASP = Auxiliary Output File Switch Pack Position
 SP = Output File Switch Pack Position
 T & B = Connect conductor to pin two feet in length with ring connector on free end. Bundle and the conductors separately.

DETAIL FOR MODELS 222, 222T, 242 AND 252



MODELS 222 & 222T CONNECTOR ASSIGNMENTS

PIN	FUNCTION
A	DC Ground
B	+24 VDC
---	---
*C	Detector Reset
D	#1 Input
E	#1 Input
F	#1 Output (C)
H	#1 Output (E)
J	#2 Input
K	#2 Input
L	Equipment Ground
M	AC-
N	AC+
P	#3 Input
R	#3 Input
S	#3 Output (C)
T	#3 Output (E)
U	#4 Input
V	#4 Input
W	#2 Output (C)
X	#2 Output (E)
Y	#4 Output (C)
Z	#4 Output (E)

MODELS 242 & 252 CONNECTOR ASSIGNMENTS

PIN	FUNCTION
*A	DC Ground
*B	+24 VDC
---	---
C	NA
D	#1 Input
E	#1 Input Common
F	#1 Output (C)
H	#1 Output (E)
J	#2 Input
K	#2 Input Common
L	Equipment Ground
M	AC-
N	AC+
P	NA
R	NA
S	NA
T	NA
U	NA
V	NA
W	#2 Output (C)
X	#2 Output (E)
Y	Y Output
Z	NA

- ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).
- MODELS 222, 222T, 242 AND 252 SHALL HAVE A WIDTH OF 28.4 mm
- MODEL 210 TOLERANCE DIMENSIONS ARE ±0.5 mm EXCEPT AS NOTED
- SHEET DEFINITIONS:
 --- SLOTTED FOR KEYING
 (C) = COLLECTOR
 (E) = EMITTER
 * = NA FOR THESE CONNECTIONS ON MODEL 242
- 'U' SHAPE ROD HANDLE SHALL BE FABRICATED OF 5 TO 10 mm DIAMETER STOCK TO FORM A HANDLE.
- THE MODEL 200 CONNECTOR SHALL BE BEAU P-5412-LAB (OR EQUAL). THE MODEL 204 CONNECTOR SHALL BE BEAU P-5406-LAB (OR EQUAL).

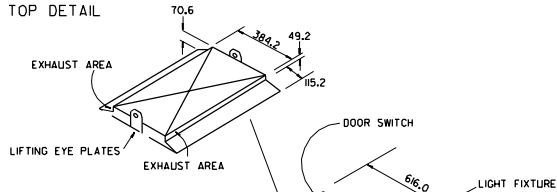
MODELS 200, 204, 210, 222, 222T, 242 AND 252

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CABINET HOUSING I
TOP DETAIL

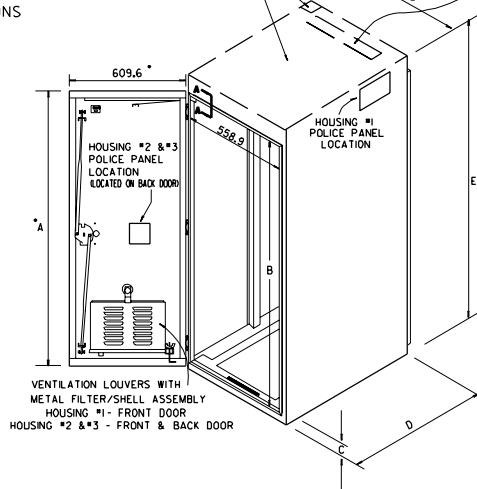
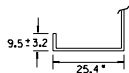


CABINET HOUSING DIMENSIONS

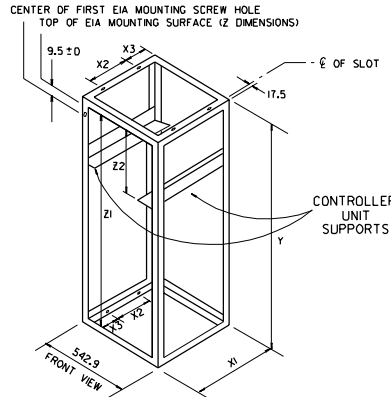
	1	2	3
A*	1483	889	1080
B	1435	838	1029
C	102	51	51
D	768	514	514
E	1626	914	1105

* TOLERANCE +1.6, -0

SECTION A-A
FLANGE AROUND DOOR OPENING



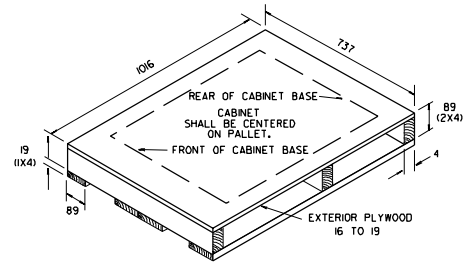
CAGE SUPPORT DETAIL



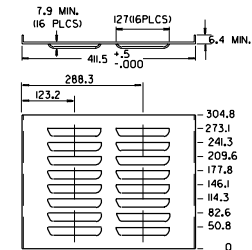
CABINET CAGE DIMENSIONS

CAGE #1	CAGE #2	CAGE #3
X1	542.9	406.4
X2	400	304.8
X3	80.9	50.8
Y	1409.7	825.5
Z1	1346.2 MIN.	787.4 MIN.
Z2	400.1	184.2

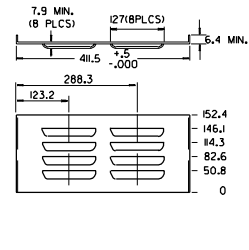
CABINET PALLET



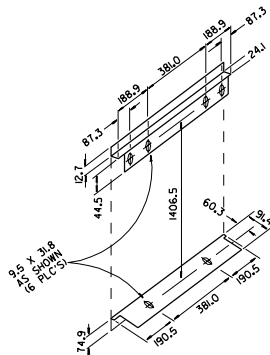
LOUVERED FILTER SHELL DETAIL HOUSING #1



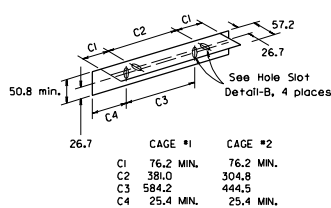
LOUVERED FILTER SHELL DETAIL HOUSING #2 & #3



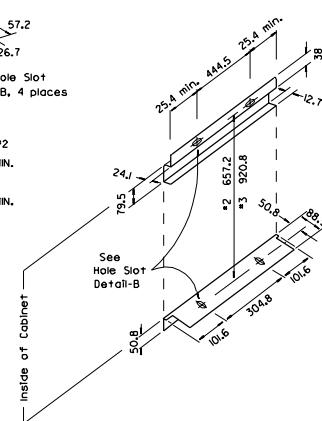
CABINET HOUSING #1
CAGE SUPPORT DETAIL



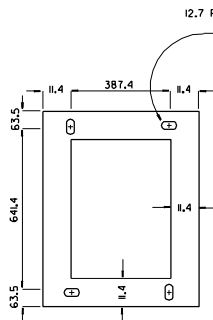
SPACER BRACKET DETAIL



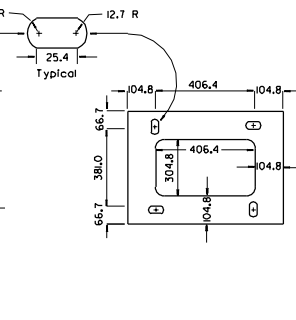
CABINET HOUSING #2 & #3
CAGE SUPPORT DETAIL



CABINET HOUSING #1
BOTTOM DETAIL



CABINET HOUSING #2
BOTTOM DETAIL



NOTE:

- DASHED LINES ON CABINET CAGE SUPPORT DETAIL DELINEATES THE CABINET SIDE WALL.
- THE BOTTOM CABINET CAGE SUPPORTS SHALL BE CONTINUOUSLY WELDED ALONG THE SIDES OF THE CABINET AND EXTENDED TO THE INSIDE CORNER OF DOOR OPENINGS. THE TOP CABINET CAGE SUPPORTS SHALL BE CONTINUOUSLY WELDED ALONG THE SIDES OF THE CABINET. THE TOP CABINET CAGE SUPPORTS SHALL BE A MINIMUM OF 552.5 mm APART.
- THE "X" DIMENSION SIDE OF THE MOUNTING CAGE SHALL BE BOLTED TO THE CABINET CAGE SUPPORTS.
- EXCEPT WHERE SPECIALLY CALLED OUT, ALL DIMENSIONS SHALL HAVE A ± 1.6 mm TOLERANCE.
- ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).

CABINET DETAILS

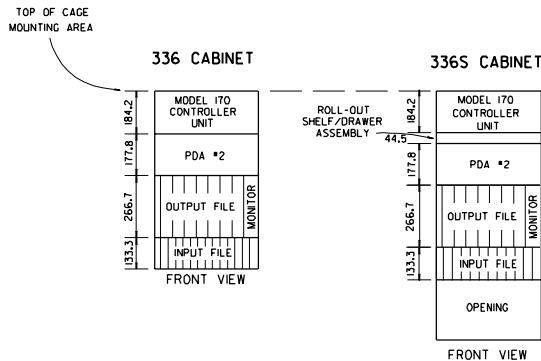
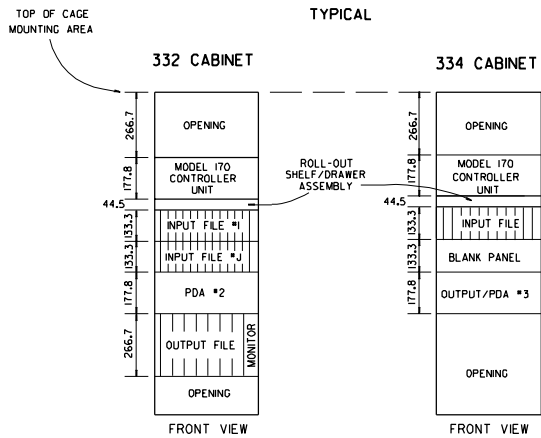
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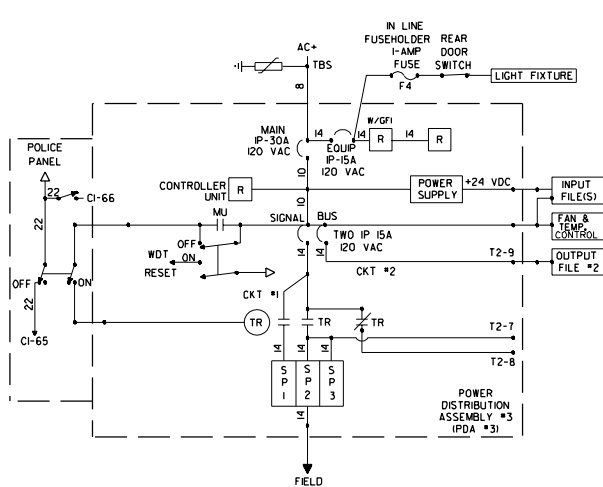
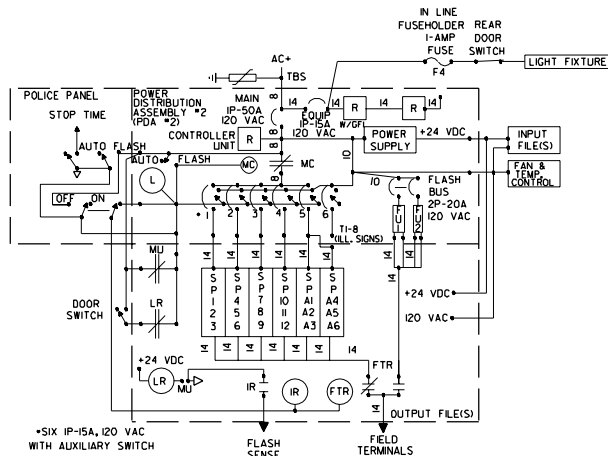
STANDARD.F.1.9

Drwg. No. 5

CABINET EQUIPMENT MOUNTING DETAIL



332, 336, & 336S CABINET ONE LINE DIAGRAM



334 CABINET ONE LINE DIAGRAM

SHEET DEFINITION

	SURGE PROTECTORS
	TERMINAL BLOCK-SERVICE
	EQUIPMENT GROUND
	POWER DISTRIBUTION ASSEMBLY
	WIRE SIZE, IF NOT INDICATED SHALL BE # 14 AWG
	CIRCUIT BREAKER
	DUPLEX RECEPTACLE
	WITH GROUND FAULT INTERRUPTER
	RELAY CONTACT, NORMALLY CLOSED
	RELAY CONTACT, NORMALLY OPEN
	MERCURY CONTACTOR
	RELAY COIL - RELAY NAME
	DC GROUND
	FLASHER UNIT ONE
	FLASH RELAY
	WATCHDOG TIMER
	FLASH TRANSFER RELAY
	PDA FLASH ON DISPLAY LAMP
	DOOR SWITCH, SHOWN WITH DOOR OPEN
	SIGNAL CIRCUIT BREAKER (SECONDARY)
	TRANSFER RELAY
	ISOLATION RELAY
	LOGIC RELAY
	INPUT FILE I, TERM BLOCK 14, POSITION D

NOTE:
1. ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).

ONE LINE DIAGRAMS & EQUIP. MOUNTING

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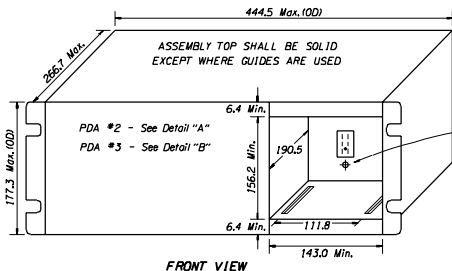
September 11, 2001

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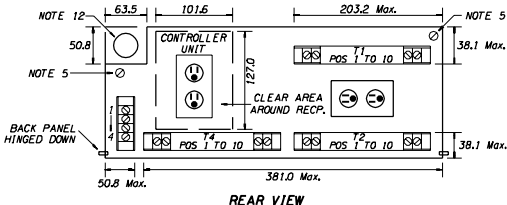
STANDARD.FL9

Drwg. No. 6

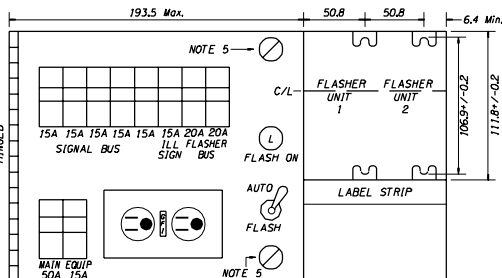
POWER DISTRIBUTION ASSEMBLIES #2 & 3



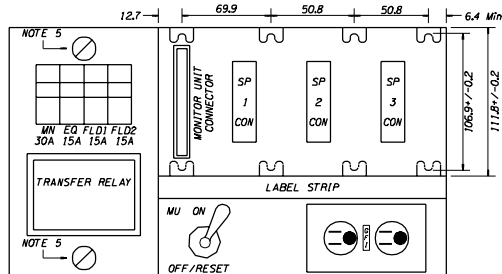
FRONT VIEW



REAR VIEW

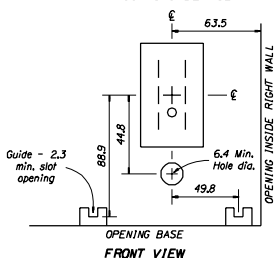


DETAIL A



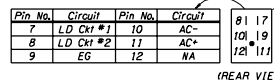
DETAIL B

POWER SUPPLY CONNECTOR/STUD MOUNTING DETAIL



FRONT VIEW

FLASHER UNIT CONNECTOR SOCKET WIRING DETAIL



POWER SUPPLY MODULE WIRING DETAIL

Pin No.	Circuit	Pin No.	Circuit
7	+24 VDC	10	NA
8	DC GND	11	AC+
9	EG	12	AC+

POWER DISTRIBUTION ASSEMBLY TERMINAL BLOCK ASSIGNMENT DETAIL

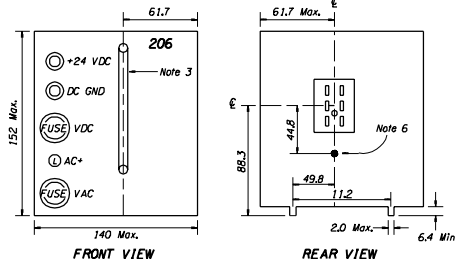
BLOCK	T1	T2	T3	T4
PDA'S	2A/B (3-NA)	2A/B	3A/B	2 & 3A/B
POS	2A/B	2A/B	3A/B	2A/B
1.	EG BUS/EG AC	/ER AC- 01-5/FUI-7	EG BUS/EQ GND AC- BUS/AC	+24 VDC BUS/PS-7 NA /NA
2.	AC BUS/AC-	01-6/FUI-8	/WCB(SEC) DC GND BUS/PS-8	NA /NA
3.	AC BUS/AC-	01-7/FUS-6	/WCB(SEC) NA /NA	NA /NA
4.	03-5 /WCB(SEC) 01-8/FUS-6	NA	/WCB(SEC) NA /NA	NA /NA
5.	NA	NA	TR NC CKT NA /NA	NA /NA
6.	NA	NA	TR COIL NA /NA	NA /NA
7.	MC COIL 01-1/SCB CKT 1	NA	/TRCND NA /NA	NA /NA
8.	/SCB CKT 2 01-2/SCB CKT 2	NA	NA /NA	NA /NA
9.	/WCB(SEC) 01-3/SCB CKT 3	03-5 /FLD2	NA /NA	NA /NA
10.	/ER AC+ 01-4/SCB CKT 4	NA	NA /NA	NA /NA

A = EXTERNAL SIDE B = INTERNAL SIDE * = WIRE PER ONE LINE DIAGRAM

NOTES:

- ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).
- SHEET DEFINITIONS:
 - EG = EQUIPMENT GROUND
 - CKT = CIRCUIT
 - FLD1 = FIELD 1 CIRCUIT BREAKER
 - FUI-7 = FLASHER UNIT #1, PIN 7
 - L = LAMP
 - WC = MERCURY CONTACTOR
 - MN = MAIN
 - OD = OUTSIDE DIMENSION
 - PS-7 = POWER SUPPLY PIN 7
 - SP 3-3 = SWITCH PACK 3, PIN 3
 - ER = EQUIPMENT RECEPTACLE
 - FL1 = FIELD LOAD 1
 - LD CKT #1 = LOAD CIRCUIT 1
 - MCB = MAIN CIRCUIT BREAKER
 - MU-22 = MONITOR UNIT - PIN 22
 - POS = POSITION
 - SCB = SIGNAL CIRCUIT BREAKER
 - TR = TRANSFER RELAY
 - 01-8 = OUTPUT FILE TB 01, POSITION B
- "U" SHAPED ROD HANDLE FABRICATED OF 6.4 ± 0.3 DIAMETER ALUMINUM STOCK, WITH 1.8 ± 0.2 LENGTH TO OD. HANDLE SHALL BE PROVIDED THE HANDLE SHALL BE VERTICALLY CENTERED THE DEPTH FROM THE VERTICAL CENTERLINE OF THE HANDLE ROD TO THE MODULE FRONT PANEL SHALL BE 31.8 ± 0.2
- THE POWER SUPPLY MODULE DIMENSION FROM FRONT PANEL TO CONNECTOR PLUG, SHALL BE 187.3 ± 0.0, ± 0.2.
- THUMB SCREW DEVICE.
- A STANDARD 8-32 METAL STUD RETAINING SCREW SHALL PROVIDE PROPER SECURING OF THE POWER SUPPLY WHEN INSTALLED IN THE PDA USING WASHERS AND A WINGNUT WHEN TORQUED IN THE LOCKING POSITION NO STRESS SHALL BE APPLIED ON THE MATING SOCKET/PLUG CONNECTOR SURFACE, NO MOUNTING OF CHASSIS SUPPORT SCREWS SHALL PROTRUDE BEYOND THE MATING SURFACE OF THE POWER SUPPLY CONNECTOR.
- TOP OF THE TRANSFER RELAY SHALL EXTEND NO MORE THAN 25.4 mm OUT FROM THE ASSEMBLY FRONT FACE.
- SLACK SHALL BE PROVIDED IN THE WIRING FOR THE CIRCUIT BREAKERS AND GFI RECEPTACLE TO ALLOW FOR THE REMOVAL AND REPAIR. EXCESS BENDS AND STRESS ON THE WIRING SHALL BE MINIMIZED.
- SEE OUTPUT FILE PLAN SHEET FOR HEAVY DUTY RELAY AND SWITCH PACK WIRING ASSIGNMENTS AND CONNECTOR MOUNTING LOCATION.
- WIRING SHALL BE ROUTED WITH EXTRA LENGTH TO MINIMIZE MOVEMENT WHEN FRONT PANEL DOOR IS OPENED. THE WIRING GOING TO THE FRONT PANEL SHALL BE ROUTED SUCH THAT IT DOES NOT CAUSE UNDUE TWISTING OR BENDING OF THE WIRES.
- NO VENTILATION HOLE SHALL BE LARGE ENOUGH TO PLACE A 9.5 mm DIAMETER OBJECT THROUGH.
- THE CSP SUPPORT CONNECTOR AND SUPPORT BRACKET SHALL BE INSTALLED WIRING HAIN IN THE PDA #2 IF THE PDA #2 IS USED. THE INPUT PANEL CSP CONNECTOR IS NOT REQUIRED AND HARNESS #2 CSP CONNECTOR SHALL BE CONNECTED TO PDA #2 CSP. THE CSP CONNECTOR AND SUPPORT BRACKET SHALL BE INSTALLED IN PDA #3.

MODEL 206 POWER SUPPLY MODULE



FRONT VIEW

REAR VIEW

POWER DISTRIBUTION

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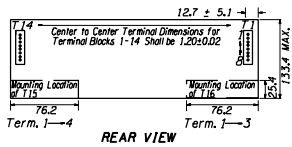
September 11, 2001

DATE

STANDARDS.F10

Drwg. No. 7

INPUT FILE DETAIL

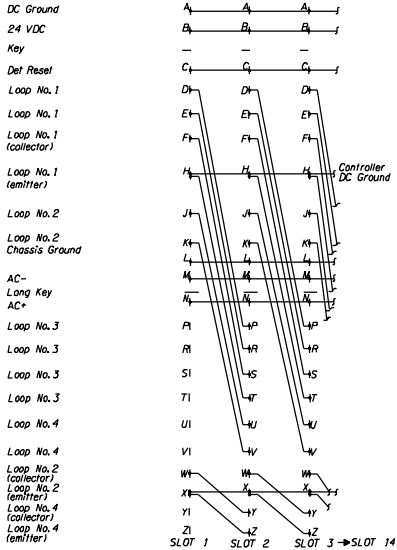


REAR VIEW

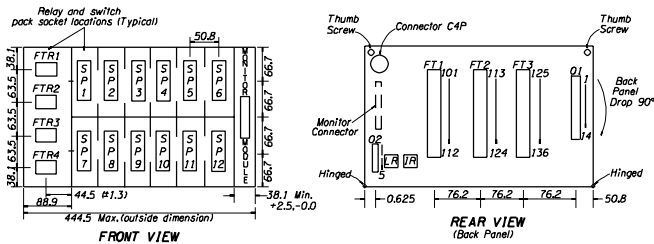
INPUT FILE TERMINAL ASSIGNMENT DETAIL

Term.	Pin-Function	Term.	Function	Term.	Function
1	SP-Spare	1	+24 VDC	1	AC*
2	F-Channel 1 Output	2	DC Ground	2	AC*
3	W-Channel 2 Output	3	Del. Reset	3	Equip. Ground
4	D-Channel 1 Input	4	C1 Harness		
5	E-Channel 1 Input		DC Ground		
6	J-Channel 2 Input				
7	K-Channel 2 Input				
8	L-Equip. Ground				

INPUT FILE WIRING DIAGRAM



OUTPUT FILE DETAIL



REAR VIEW (Back Panel)

FRONT VIEW

OUTPUT FILE TERMINAL ASSIGNMENT DETAIL

01 Term.	FUNCTION	02 Term.	FUNCTION	FT1 Term.	FUNCTION	FT2 Term.	FUNCTION	FT3 Term.	FUNCTION
1	PDA CKT1/SWPKS 1,2,3	1	+24 VDC	101	SWPK 5-RED	126	SWPK 3-RED	126	SWPK 1-RED
2	PDA CKT2/SWPKS 4,5,6	2	DC GROUND	102	SWPK 5-YEL	114	SWPK 3-YEL	126	SWPK 1-YEL
3	PDA CKT3/SWPKS 7,8,9	3	IF1-14J, STOP TIME (FROM MU)	103	SWPK 5-GRN	115	SWPK 3-GRN	127	SWPK 1-GRN
4	PDA CKT4/SWPKS 10,11,12	4	IF1-14D, FLASH SENSE (FROM IR)	104	SWPK 6-RED	116	SWPK 4-RED	128	SWPK 2-RED
5	PDA FU1 CKT1/FFTR1	5	EXTERNAL RESET (TO MU)	105	SWPK 6-TEL	117	SWPK 4-YEL	129	SWPK 2-YEL
6	PDA FU1 CKT2/FFTR2	10	SWPK 6-GRN	118	SWPK 4-GRN	130	SWPK 4-GRN	130	SWPK 2-GRN
7	PDA FU2 CKT1/FFTR3	107	SWPK 11-RED	119	SWPK 9-RED	131	SWPK 9-RED	131	SWPK 7-RED
8	PDA FU2 CKT2/FFTR4	108	SWPK 11-YEL	120	SWPK 9-YEL	132	SWPK 9-YEL	132	SWPK 7-YEL
9	EQUIP. GROUND	109	SWPK 11-GRN	121	SWPK 9-GRN	133	SWPK 9-GRN	133	SWPK 7-GRN
10	AC*	110	SWPK 12-RED	122	SWPK 10-RED	134	SWPK 10-RED	134	SWPK 8-RED
11	AC* (FROM PDA)	111	SWPK 12-YEL	123	SWPK 10-YEL	135	SWPK 10-YEL	135	SWPK 8-YEL
12	MC COIL (TO PDA)	112	SWPK 12-GRN	124	SWPK 10-GRN	136	SWPK 10-GRN	136	SWPK 8-GRN
13	DOOR SW								
14	FFR COIL CONTROL (FROM P.P. SW1)								

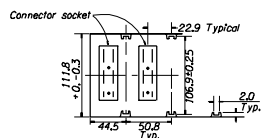
FRONT VIEW

REAR VIEW (Back Panel)

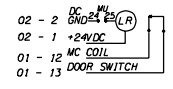
AUXILIARY OUTPUT FILE TERMINAL ASSIGNMENT DETAIL

03 Term.	FUNCTION	04 Term.	FUNCTION
1	PDA FU1 CKT 1/FFTR5	1	+24 VDC
2	PDA FU2 CKT 2/FFTR6	2	DC GROUND
3	FFR COIL CONTROL	3	STOP TIME
4	AC*	4	FLASH SENSE
5	PDA CKT 2/SWPKS 1, 2, 3-1	5	EXTERNAL RESET
6	PDA CKT 4/SWPKS 4, 5, 6-1	6	WOT INPUT
7	EQUIPMENT GROUND	7	LR COIL (UNIT IN)
8	MC COIL (PDA)	8	MC COIL (PDA)
9	DOOR SW	9	DOOR SW
10	AC* (FROM PDA)	10	+24 VDC

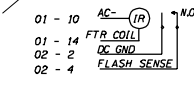
SWITCH PACK MOUNTING DETAIL



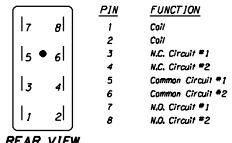
LOGIC RELAY (LR) DETAIL



ISOLATION RELAY (IR) DETAIL

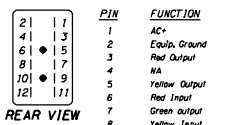


HEAVY DUTY FLASH RELAY SOCKET DETAIL



REAR VIEW

SWITCH PACK SOCKET DETAIL



REAR VIEW

MODEL 210 MONITOR UNIT PIN ASSIGNMENT

CONNECTOR	MONITOR	TERMINATION	CONNECTOR	MONITOR	TERMINATION
1	SWPK 2 GRN	130	A	SWPK 2 YEL	129
2	SWPK 3 GRN	115	B	SWPK 8 GRN	136
3	SWPK 4 YEL	135	C	SWPK 9 GRN	121
4	SWPK 5 GRN	103	D	SWPK 5 YEL	102
5	SWPK 6 GRN	106	E	SWPK 11 GRN	109
6	SWPK 11 YEL	108	F	SWPK 12 GRN	112
7	SWPK 7 GRN	133	H	SWPK 7 YEL	132
8	T & B		J	SWPK 1 GRN	127
9	SWPK 1 YEL	126	K	T & B	
10	SWPK 10 GRN	124	L	SWPK 10 YEL	123
11	T & B		M	SWPK 4 GRN	118
12	SWPK 4 YEL	117	N	T & B	
13	ASPI - GRN	A123	P	NA	
14	NA		R	ASPI - GRN	A126
15	T & B		S	ASPI - GRN	A116
16	T & B		T	NA	
17	NA		U	T & B	
18	T & B		V	ASPS - GRN	A103
19	NA		W	NA	
20	EQ GND	01 - 9	X	NA	
21	AC	01 - 10	Y	DC GROUND	02 - 2
22	WATCHDOG TIMER	04-37	Z	EXTERNAL RESET	02 - 5
23	+24 VDC	02 - 1	AA	T & B	
24	INTERLOCK	LOGIC RELAY COIL	BB	STOP TIME	02 - 3
25	INTERLOCK	02 - 2	CC	NA	
26	NA		DD	NA	
27	NA		EE	OUT.RELAY - COMMON	01 - 12
28	OUT.RELAY - N.C.	01 - 11	FF	AC*	01 - 11

NOTES:

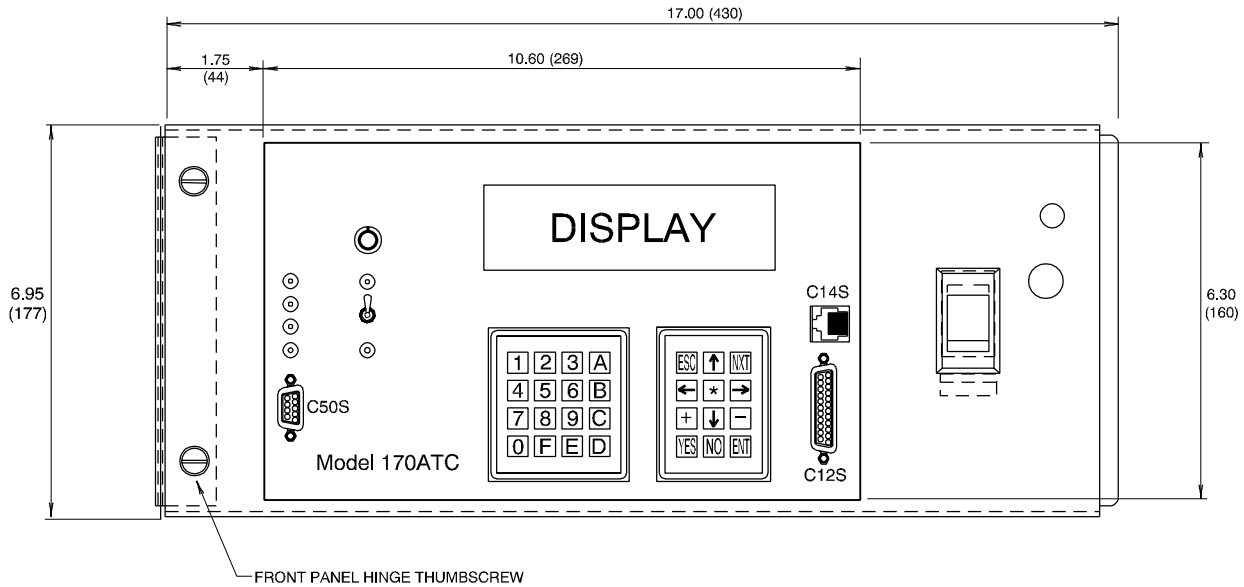
- ALL DIMENSIONS SHOWN ARE IN MILLIMETERS (mm).
- TOP OF RELAYS SHALL BE FLUSH WITH FACE OF FILE.
- THE ISOLATION RELAY SHALL BE POTTER & BRUMFIELD R10-E1-X2-115 (OR EQUAL). THE LOGIC RELAY SHALL BE A POTTER & BRUMFIELD KUP11 (O11, D15, OR EQUAL).
- SEE CONNECTORS C4 & C5 WIRING LISTS FOR CONNECTOR/FILE INTERFACE.
- SHEET DEFINITIONS:
 CKT = CIRCUIT
 FU = FLASHER UNIT
 FTR = FLASH TRANSFER RELAY
 IF1-14D = INPUT FILE #1; TB 14, TERMINAL D
 MC = MERCURY CONTACT (PDA)
 MU = MONITOR UNIT
 N.C. = NORMALLY CLOSED RELAY CIRCUIT
 N.O. = NORMALLY OPEN RELAY CIRCUIT
 PDA FU1 CKT 1 = PDA FLASHER UNIT 1, OUTPUT CIRCUIT 1
 POL. PAN = POLICE PANEL
 SW = SWITCH
 SWPK = SWITCH PACK
 T & B = CONDUCTORS CONNECTED TO PIN. 6 METERS IN LENGTH WITH RING LUG ON UNCONNECTED END, TIED AND BUNDLED SEPARATELY.

INPUT & OUTPUT FILES

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 Dwg. No. 8

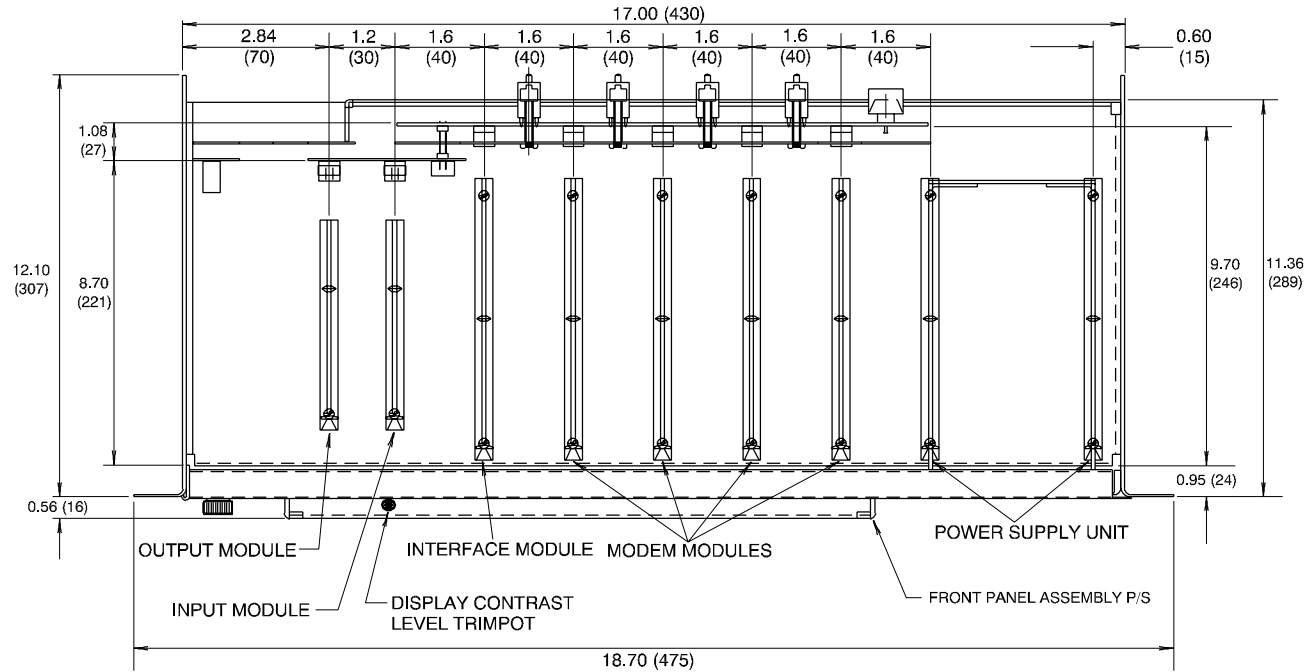


FRONT PANEL ASSEMBLY (FPA)
(SHOWN REMOVED FROM CONTROLLER)

DIMENSIONS IN () ARE METRIC MEASUREMENTS IN MM'S

MODEL 170ATC CONTROLLER

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DATE <u>September 11, 2001</u>	Drwg. No. 11

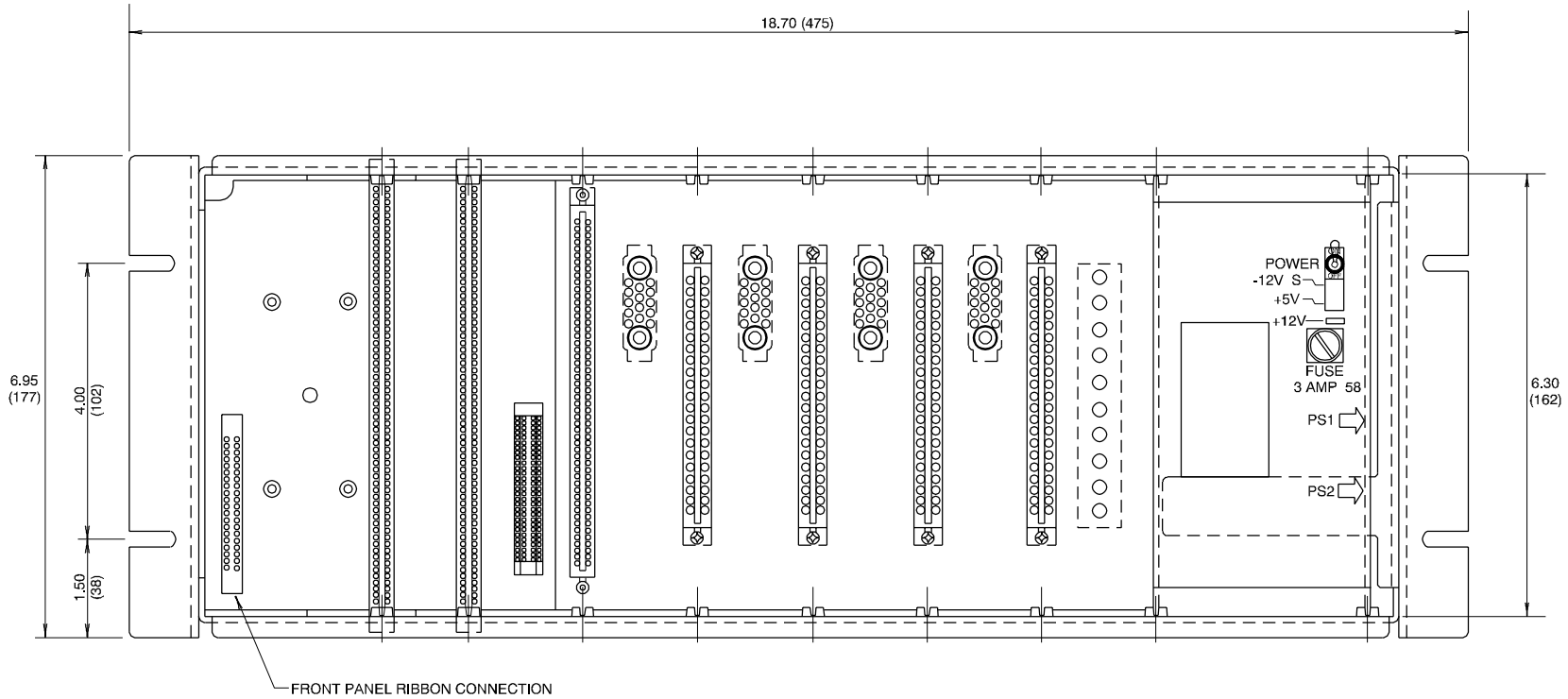


TOP VIEW
(SHOWN WITH TOP PANEL REMOVED)

DIMENSIONS IN () ARE METRIC MEASUREMENTS IN MM'S

MODEL 170ATC CONTROLLER

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6.95
(177)

4.00
(102)

1.50
(38)

18.70 (475)

6.30
(162)

FRONT PANEL RIBBON CONNECTION

POWER
-12V S
+5V
+12V
FUSE
3 AMP 58
PS1
PS2

FRONT VIEW

(SHOWN WITH FRONT PANEL ASSEMBLY REMOVED)

DIMENSIONS IN () ARE METRIC MEASUREMENTS IN MM'S

MODEL 170ATC CONTROLLER

MODEL 170ATC CONTROLLER

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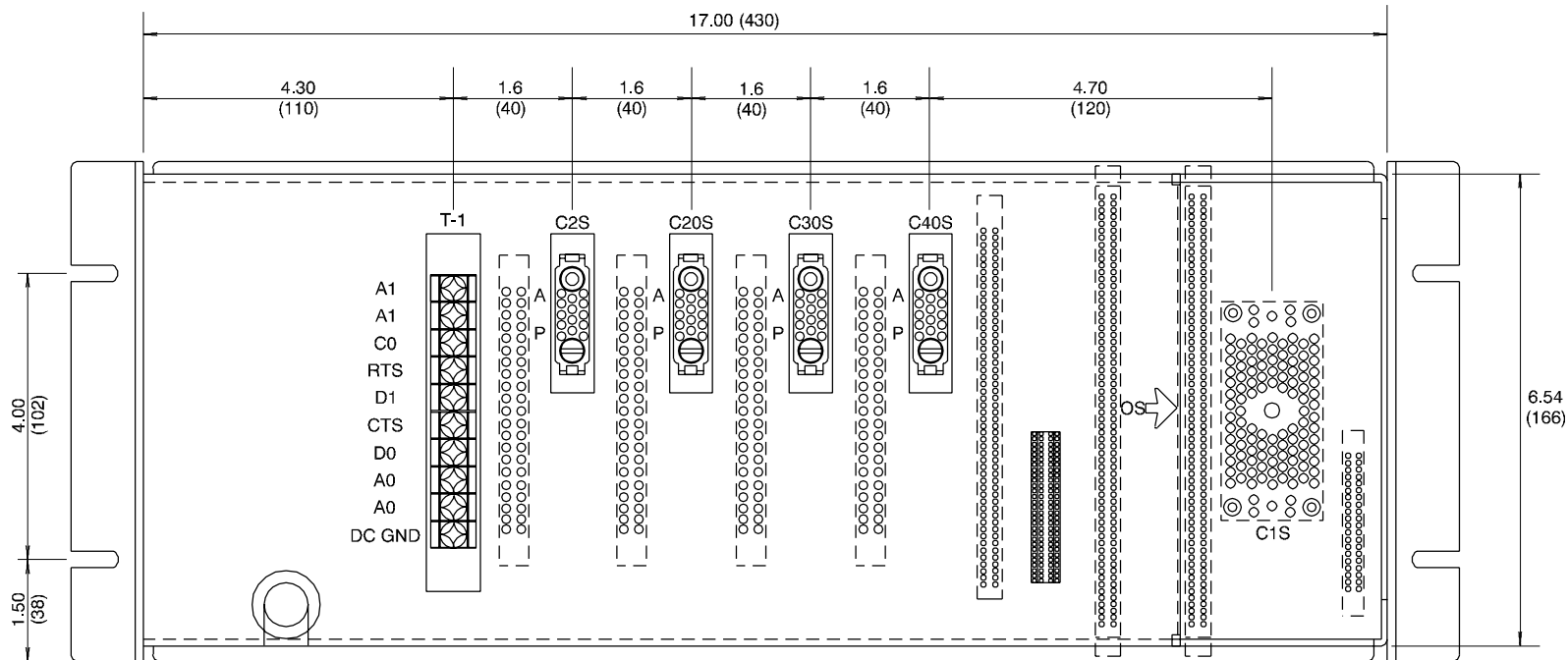
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DRWG13.DWG

Drwg. No. 13



REAR VIEW

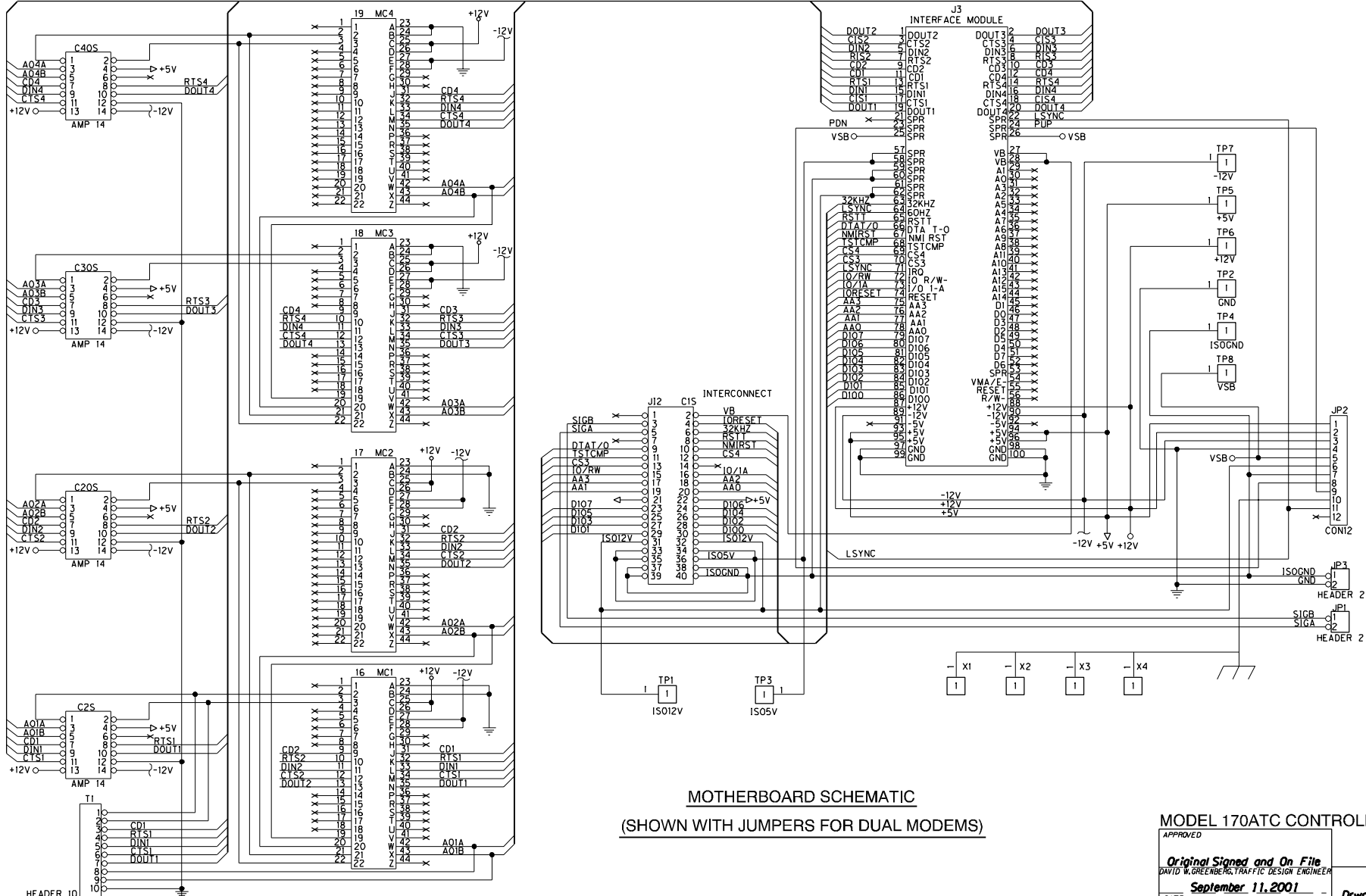
DIMENSIONS IN () ARE METRIC MEASUREMENTS IN MM'S

MODEL 170ATC CONTROLLER

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 DATE September 11, 2001

DPWG14.DGN

Drwg. No. 14



MOTHERBOARD SCHEMATIC
(SHOWN WITH JUMPERS FOR DUAL MODEMS)

MODEL 170ATC CONTROLLER

APPROVED

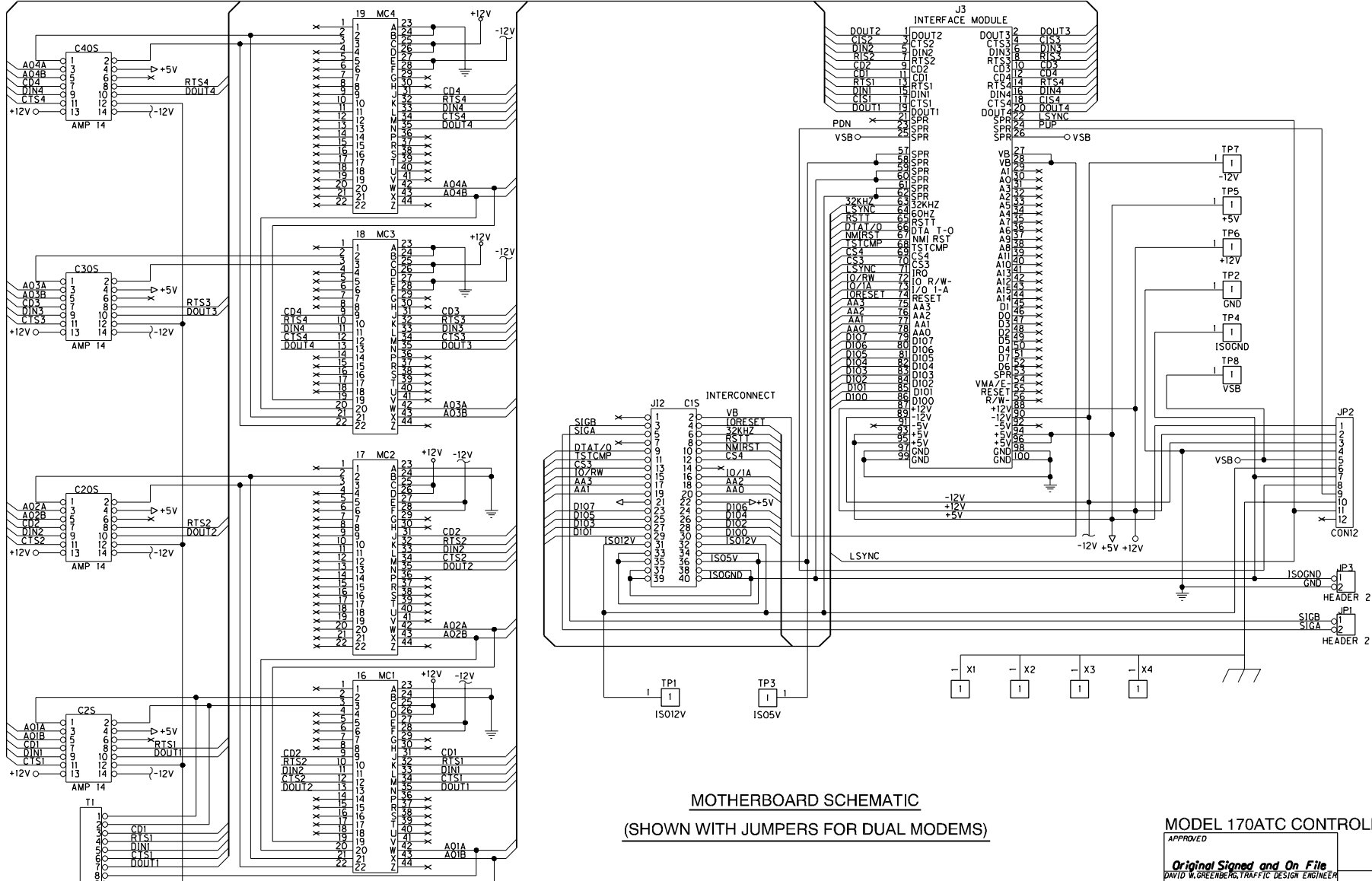
Original Signed and On File
DAVID W. GREENBERG, TRAFFIC DESIGN ENGINEER

September 11, 2001

DATE

DRWG 16.DGM

Drwg. No. 16



MOTHERBOARD SCHEMATIC
(SHOWN WITH JUMPERS FOR DUAL MODEMS)

MODEL 170ATC CONTROLLER

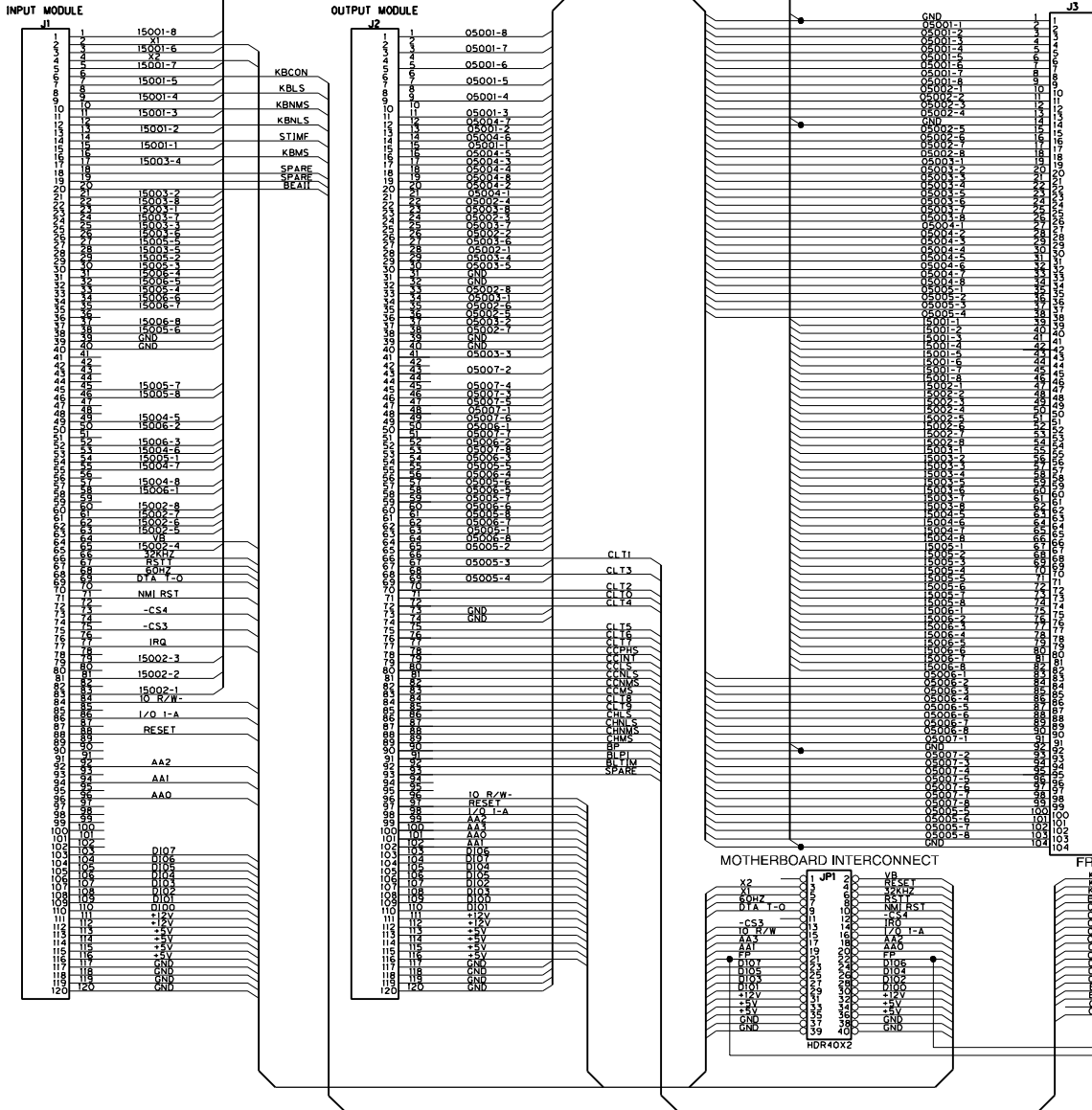
APPROVED

Original Signed and On File
DAVID W. GREENBERG, TRAFFIC DESIGN ENGINEER

DATE September 11, 2001

DRWG 16.DGM

Drwg. No. 14



DAUGHTERBOARD SCHEMATIC

Appendix D



TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS

TEES 2009 ERRATA No.1



January 21st, 2010

**STATE OF CALIFORNIA
DEPARTMENT OF TRANSPORTATION**



Arnold Schwarzenegger
Governor

Dale Bonner
Secretary
Business, Transportation & Housing
Agency

Will Kempton
Director
Department of Transportation

Michael Miles
Deputy Director
Maintenance and Operations

Robert Copp
Program Manager
Traffic Operations

Jeff McRae
Chief, Office ITS Projects and Standards

Herasmo Iñiguez
Sr. TEE, Office ITS Projects and Standards

The following TEES dated March 12th, 2009 and Chapter 4 dated July 7, 2009 plans and sections should be modified or added.

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Errata No. 1

1.3.10 Fuses

All Fuses shall be [3.15 Amp Glass Slow Blow type](#) and resident in a holder. Fuse size rating shall be labeled on the chassis, PCB or beside the holder. Fuses shall be easily accessible and removable without use of tools.

2.5.1 Mechanical/Electrical Requirements

The [Model 400N Ethernet Module](#) shall be dimensionally and electrically designed to fit in a single slot of a standard 170 controller.

2.5.5 Data Interfaces

Main Data Port Model 170 male 44 pin Edge Connector

User Serial Port EIA-232 (DB9 Female); [Optional](#)

Ethernet Data Port RJ45 EIA 568B Pin Out

3.4.2.11 Output Turn-on Delay

The [Model 206L](#) shall have an [Output Turn-On Delay](#) of less than 200mSec from AC turn-on.

4.2.10.1 AC Connection

The AC input and output shall be [quick disconnect](#) plug / receptacles that allow no possibility of accidental exposure to dangerous voltages (male receptacle for AC Input and female receptacle for AC Output). The receptacles shall utilize some form of locking mechanism or hold down clamps to in order to prevent any accidental disconnects.

6.4.3.1.1 PDA #2L

- 1 -- Duplex NEMA 5-15R Controller Receptacle
- 2 -- Duplex NEMA 5-15R Equipment Receptacle (one with GFCI)
- 1 -- 1 Pole 15 Amperes minimum, 120 VAC Signal Bus Circuit Breaker
- 1 -- 1 Pole 15 Amperes minimum, 120 VAC Clean Power Circuit Breaker
- 6 -- 1 Pole Ganged, 10 Amperes, 120 VAC Signal Bus Circuit Breaker with Auxiliary Switch
- 1 -- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
- 1 -- 2 Pole Ganged, 10 Amperes, 120 VAC Flash Bus Circuit Breaker
- 1 -- Solid State Relay (Normally Closed) - rated minimum 50 Amperes, 120 VAC, [Crydom A2450-B](#) or equal.
- 2 -- Model 204 Flasher Unit and Socket
- 1 -- Model 206L Power Supply Module and Socket
- 1 -- AUTO/FLASH Control Switch
- 1 -- Flash On Indicator Light
- 3 -- 10 Position TBK T1, T2 & T4
- 1 -- 4 Position TBK T3
- 1 -- SSR Fault Indicator Light
- 1 -- [HI Health Indicator Relay](#)
- 1 -- [K24 24VDC Controlled Relay](#)

9.1.1 Controller Unit

The Controller Unit shall be composed of the Unit Chassis, modules and assemblies per their version. The following is a list of 2070 Versions, their interface rolls and composition:

UNIT VERSION	DESCRIPTION
2070V UNIT	Provides directly driven VME and mates to 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1A TB, 2070-1A MCB, 2070-2A FI/O, 2070-3A FRONT PANEL, 2070-4 POWER SUPPLY, and 2070-5 VME CAGE ASSEMBLY.
2070E UNIT	LITE Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY
2070EC UNIT	LITE unit mates to ITS cabinets only. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2B FI/O, 2070-3C FRONT PANEL and 2070-4 POWER SUPPLY
2070LX UNIT	LX Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1C CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY
Note: See Chapter 11 for 2070 NEMA Versions	

9.2.2.1 Dual SCC Device

A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1 except where noted.

The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68EN360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. The SP8 shall meet all SP2 Port requirements except where noted, including EIA 485 drivers / receivers and synchronous data rate of 153.3 Kbps.

9.2.7.2.3 MC68360 Internal Timers

A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. Timer resolution shall be one count equals 100 μ S and all timer periods shall be specified in units of hundreds of microseconds (μ S).

A signal of "0" shall be an invalid signal and the driver shall return an E\$PARAM error if received.

Access to the MC68360 internal timers shall be through the descriptors as listed under Descriptor.

The timers should be set to the SS2070_Timer_Null Mode upon initialization.

9.2.7.2.5 Flow Control Modes

The asynchronous serial communications device drivers shall support the six flow control modes (FCM#) described below:

FCM#	Description
0.	No Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed. This is the default mode. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode (FCM# 1).

1. Manual Flow Control Mode: The driver transmits data regardless of the state of CTS. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
2. Auto-CTS Flow Control Mode: The driver transmits data only when CTS is externally asserted. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
3. Auto-RTS Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If the user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
4. Fully Automatic Flow Control Mode: The driver transmits data only when CTS is externally asserted. Upon a write command, the driver asserts RTS and waits for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
5. Dynamic Flow Control Mode: The driver transmits data only when CTS is externally asserted. The driver controls RTS based on the status of its receiving buffer. The driver asserts RTS continuously as long as its receiving buffer has sufficient capacity to store incoming data. If the receiving buffer approaches full, the driver de-asserts RTS until enough data has been read from the buffer to create sufficient receive capacity.

9.2.7.3.1 Startup Procedure

The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo shall operate as follows:

1. Sysgo shall set the execution directory to /f0wp/CMDS
2. Sysgo shall check if the backspace key (0x08) is being received on /sp4 (c50j). If received, Sysgo shall:
 - a. Fork a shell with no arguments on /sp4 using the current directory.
 - b. Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo shall fork another shell with no arguments on /sp4. Unless Sysgo dies, a shell shall always be provided on /sp4.

3. If the backspace key was not received, Sysgo shall check for the presence of a Datakey. If present and valid (Datakey Header Version 2 or greater), Sysgo shall check the Startup Override Byte in the Datakey header.

If Startup Override is 0x01, Sysgo shall:

- a. Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header shall be the size of the script in bytes. The script shall immediately follow the size value, and shall be stored as ASCII text.
- b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

If Startup Override is 0x02, Sysgo shall:

- a. Fork an executable module stored on the Datakey immediately following the header.
- b. If there is any error loading or forking the module, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking the module, Sysgo shall then exit without forking a shell.

4. If the backspace key was not received and Startup Override Byte is 0xFF:

- a. Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.
- b. If there is any error loading or forking OPEXEC, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking OPEXEC, Sysgo shall then exit without forking a shell.

5. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC file:

- a. Sysgo shall fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.
- b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.

6. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC and no startup file:

- a. Sysgo shall fork a shell as described in step 2.

9.2.7.5.1 CMDS

The following Network utilities shall be included and shall reside in the /f0/CMDS directory as identified in this specification.

arp, dhcp, ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetdc, hostname, nfsc, mount, rpcdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, nfsd, mountd, and showmount.

9.2.7.6.1 Ver

A Ver utility shall be provided as part of the OS-9 Image and shall allow access to Controller's Manufacturer Name, Image Build Number, TEES Version, Image Build Date and CPU Module Type. Ver should display the contents of a data module named "bootid" which contains in it's data area the following structure:

```
/* bootid_body*/
Struct bootid_body {

char *mfgrname;           /* Manufacturer Name */
char *cpumoduletype;     /* CPU Module Type */
char *teesrelease;       /* TEES Release */
char *imagebuilddate;    /* Image Build Date */
u_int 16 majv;           /* Major Version*/
u_int 16 minv;          /* Minor Version */
u_int 16 sv1;           /* Sub-Version 1 */
u_int 16 sv2;           /* Sub-Version 2 */
u_int 16 sv3;           /* Sub-Version 3 */
u_int 16 dv;            /* Development Version */
};
```

Os9 Edimod shall be used to generate the heater file and the "bootid" module using the following config.des file:

```
#cinclude "defines.h" /*this file contains customization for the module */
#include <module.des> /* required for module definitions in modhcom */

struct bootid_body /* this is the bootid module structure */
{
    pointer u_int32 mfgrname = mn, "Manufacturer Name";
    pointer u_int32 cpumoduletype = cmt, "CPU Module Type";
    pointer u_int32 teesrelease = tr, "TEES Release";
```

```

    pointer u_int32 imagebuilddate = ibd, "Image Build Date ";
    u_int16 majv, "Major Version";
    u_int16 minv, "Minor Version";
        u_int16 sv1, "Sub-Version 1";
        u_int16 sv2, "Sub-Version 2";
        u_int16 sv3, "Sub-Version 3";
        u_int16 dv, "Development Version";
}, "bootid_body";

string mn = MfgName;
string cmt = CPUModuleType;
string tr = TEESRelease;
string ibd = ImageBuildDate;
string mod_name = "bootid";

init bootid_body
{
    majv = MajorVer;
    minv = MinorVer;
    sv1 = SubVer1;
    sv2 = SubVer2;
    sv3 = SubVer3;
};

init modhcom
{
    _maccess = 0x555;
    _mtype = MT_DATA;
    _mlang = 0;
    _mattr = 0x80;
    _mrev = 1;
    _medit = 1;
};

module
{
    modhcom,
    bootid_body
};

```

9.2.8.2.1 Datakey

This driver provides full capability for manipulating Datakey devices. [Datakeys of size 2Mbit and above](#) as listed in Section 9.2.6 of these specifications shall be supported.

10.6.2.1 Modem default configuration

The Modem shall contain the following default configurations:

ACTIVE PROFILE:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5
&X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:138
S08:002	S48:007
S09:006	S95:000
S10:014	

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Lock
2	“SMART Modem DB-9 Aux” Sel	DTE	DCE
3	RTS Override	Normal	RTS High
4	“Modem /DB9 DTE Serial” Sel	Modem	DB9-DTE

All switches shall be in the OPEN position as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity.

10.8.2.1 Modem default configuration

The Modem shall contain the following default configurations:

ACTIVE PROFILE:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5
&X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:138
S08:002	S48:007
S09:006	S95:000
S10:014	

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Lock
2	“SMART Modem DB-9 Aux” Sel	DTE	DCE
3	RTS Override	Normal	RTS High
4	“Modem /DB9 DTE Serial” Sel	Modem	DB9-DTE

All switches shall be in the OPEN position as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity.

CHAPTER 10-SECTION 9
MODEL 2070-7G UNIVERSAL TIME BASE MODULE

10.9.1 Model 2070-7G Universal Time Base Module

The Model 2070-7G Universal Time Base Module shall consist of a GPS receiver with antenna and a microprocessor-based circuit. It shall read raw GPS time data and accept user commands via Com 2 as defined elsewhere in these specifications. The Model 2070-7G Universal Time Base Module shall be a Plug-in Style Card version for the Model 2070 Controller. The Model 2070-7G shall be provided with two communications channels Com 1 and Com 2. Com 1 shall be use to establish serial communications between the Model 2070 Controller and a GPS receiver resident in the Model 2070-7G Universal Time Base Module. Com 2 shall be switch selectable between a Config Mode to the GPS receiver and a straight serial port for the Model 2070 Controller.

10.9.2 GPS Receiver/Antenna

The Model 2070-7G shall be provided with a Land-Based L1, C/A code GPS Receiver operating at a frequency of 1575.42MHz. The GPS Receiver shall contain a minimum of 20 Channels. The receiver shall have a tracking sensitivity level greater than -159dBm at the receiver input.

The Model 2070-7G shall be provided with an active permanently mount GPS Antenna. The Antenna mount shall consist of GPS roof-mount antenna with double threaded bolt, through hole, wing nut fastener, and locking nuts. The mounting shall consist of a Bulkhead mount with 0.8 inch threaded wing nut.

The Antenna System shall be comprised of an Antenna Element, Cable and Connector, and Low Noise Amplifier (LNA).

The Cable and Connector shall consist of a 2 Meter RG174/U Coaxial cable terminated at the non-antenna end with an SMA male straight connector.

The Antenna Element shall use Right Handed Circular Polarization (R.H.C.P) and shall have a minimum Gain of +5 dBi. The antenna shall have a VSWR of 1.5:1 max. and an output impedance of 50 Ohms.

The Low Noise Amplifier shall operate from a 3.3 to 5.5 V DC source and shall provide an Outer Band Attenuation of 20dB min. at $F_o \pm 50$ MHz and a Gain of 31dB min.

The Overall Performance of the Antenna System including Antenna Element, LNA and Coax Cable shall be a follows:

Center Frequency: 1575	1575.42 MHz
Gain	27dB min.
Noise Figure	2.0 dB max.
Axial Ratio	3.0 dB max.
Bandwidth	2 MHz min.
VSWR	2.0:1 max.
Output Impedance	50 Ohms

10.9.3 Default Configurations

The Model 2070-7G Universal Time Base Module shall have the following default configuration parameters:

Baud Rate	1200 bps
Time Zone	8, Pacific Time Zone
New Line Character	ASCII Carriage Return, Except QC, which CR+LF
Hour Format	24 hour (Military Time)
Daylight Savings Time	Enabled
Begin DST Clock Correction	March, Second Sunday at 02:00AM
End DST Clock Correction	November, First Sunday at 2:00 AM

These parameters shall configurable using the QS Command Set as defined in Section 10.9.4 of these specifications.

10.9.4 QS Command Set

The “Q” Commands

“Q” commands shall be used to request information from the Model 2070-7G, such as global position, date and time. The Model 207-7G shall support the “Q” commands as listed in the following table.

Model 2070-7G "Q" COMMANDS			
COMMAND	RETURNS	FORMAT	EXAMPLES
QA n1 n2 0 0	Status, DOY, time	13 byte Binary string	See detail comments below
QD	Date and Day of year	YY/MM/DD/day {newline}	02/02/05/036
QT	TIME	mHH:MM:SS:Thtd {newline}	A10:51:21:697 17:45:05:489D
QC	Date, time status and day of week	YYMMDDHHmmSSThLW {cr+lf}	020821231706945Y6
QD, QT, QL & QC	Message	ASCII string “NOT LOCKED ON”	NOT LOCKED ON
QM	Data stored in ROM	Bw:Dx:My:Ncr:Oz Baud: DST: 12/24: new line: TimeZone	B7:D0:M1:Ncr:O6 {newline}
QV	Firmware version	ASCII version number	v1.2
QI	Get Daylight saving time configuration	bMbsbhbmeMesehem {newline}	0302020011010200 {newline}
QL	Get Position (latitude and longitude)	DD.MM.SS.THTA ddd.mm.ss.thtO	38.53.23.123N 077.00.27.123W

“Q” Commands

QD When the “QD” command is received by the Model 2070-7G it shall respond with either the ASCII message “NOT LOCKED ON” or with the date in the format YY/MM/DD/day followed by the new line character. “doy” is the day of the year in a 3 digit format, January 1 being 001. If the Model 2070-7G has not yet found at least one satellite to insure correct data, the response shall be “NOT LOCKED ON”.

An example of a normal response from the Model 2070-7G to a “QD” command sent to it would be “02/02/05/036(new line character)”. This sample data stream would represent February 5, 2002 and that date would be the 36th day of the year 2002.

Note: If the device is configured for a time zone other than the local time zone, the date and “doy” shown could differ from the local date, depending on the time of day.

QT When the “QT” command is received by the Model 2070-7G it shall respond with either the ASCII message “NOT LOCKED ON” or with the time of day in the format of an A or a P or an ASCII space (to signify A.M. or P.M. or 24 hour time format) immediately followed by “HH:MM:SS:Tht” and a “D”, if Daylight Savings Time function is “Enabled” and ending with the new line character.

Two sample “QT” responses are:

“A10:51:21:697{NEW LINE}”, which could be interpreted as 10:51 A.M. plus 21.697 seconds and not corrected for daylight savings time.

“_17:45:05:489D{new line}”, which could be interpreted as 1745 plus 5.489 seconds (using the 24 hour format), with Daylight Savings Time Enabled. The “_” represents an ASCII “space” character and signifies that the output is in 24 hour format.

As with the “QD” command, if the Model 2070-7G is not receiving a valid signal from at least one satellite, the response to a “QT” command shall be the ASCII message “NOT LOCKED ON”.

QC This command reply shall provide a combination of the information found in the “QT” and “QD” commands but in slightly different format and with some additional information.

As with the “QT”, “QL” and “QD” commands, the message “NOT LOCKED ON” shall be the reply if the Model 2070-7G does not have at least one satellite in view to determine the precise time and date.

A special synchronization character in the data stream (either Y or N) shall signify whether or not the date and time data are synchronized with UTC (Universal Coordinated Time).

In order for the Model 2070-7G to report fully synchronized data with the special character changed to “Y”, the unit must be tracking at least 4 satellites. If the synchronization character is “N” the time reported will be less precise but still within a few milliseconds of the UTC synchronized time. The “QC” command hour format is always 24 hour (military time) since there is no character in the data stream to indicate A.M. or P.M. An additional bit of information included in the “QC” data stream is a “day of the week” number. The number 0 (zero) indicates Sunday, 1 indicates Monday and so on through 6, which indicates Saturday. Unlike the “QT” and “QD” commands, the “new line” character shall not be changed. It shall always be ASCII “carriage return

+ line feed”. The format of the “QC” data stream shall be YYMMDDHHmmSSThtLW followed by an ASCII carriage return and line feed.

A sample “QC” data steam generated by the Model 2070-7G would be:

“02032123176945Y6{cr+lf}”. This data stream would be interpreted as March 21, 2002, the time, in 24 hour format, would be 2317 plus 6.945 seconds, the time is synchronized to UTC (Y) and the day of the week is Saturday (6). Note that the data stream does not indicate whether or not Daylight savings time is “Enabled or Disabled”.

QM The “QM” command shall reply with the parameters stored in non-volatile memory, which shall be the baud rate, daylight savings time enable-disable, time format, new line character and time zone. Parameters shall be separated by a colon and the data stream shall be terminated with the new line character. The data stream B7:DO:M1:Ncr:O6{newline} would represent a baud rate = 19200 bps, Daylight savings time = disabled, 12 hour time reporting format, new line character = carriage return and Time Zone = Central. This command shall be used to determine the current configuration.

QV When the “QV” command is received by the Model 2070-7G it shall reply with the firmware version number. The format for the firmware version shall be as VX.X where X.X shall digits from 0 to9. An example of a response to the QV command would be “V1.2” without the quotation marks. The “NOT LOCKED ON” message shall never reply to this query command.

QI The “QI” command shall replay the currently loaded Daylight saving time parameters; these shall be stored in the non-volatile memory. A total of 8 parameters are shall be sent. The data stream is bMbsbhbmMesehem{newline} and the parameters are as follow:

- Begin Month (bM). The month when starts to observe the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
- Begin Sunday (bs). The Sunday number of “begin month (bM)”. This value shall be a two digits number.
- Begin Hour (bh) and Begin Minutes (bm). The time when starts to observe the DST. This time shall be expressed in a 24 hour format.
- End Month (eM). The month when ends the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
- End Sunday (es). The Sunday number of “end month (eM)”. This value shall be a two digits number.
- End Hour (eh) and End Minutes (em). The time when the DST observation ends. This time shall be expressed in a 24 hour format.

An example data stream 0302020011010200{newline} would represent DST clock adjust will begin at second Sunday of March at 02:00 AM and DST will end at first Sunday of November at 02:00 AM.

When the Model 2070-7G module detects any of both DST conditions, either Begin or End, it corrects the time by adding or subtracting one hour to local time. Once “begin DST” conditions met (Month, Sunday and time) it adds one hour to local time. When “end DST” conditions met (Month, Sunday and time) it subtracts one hour to local time. The Model 2070-7G shall always respond to this command.

QL The “QL” command will replay the latitude and longitude of the current Global Position expressed in degrees, minutes, seconds and milliseconds, north (N) or south(S) for Latitude, east (E) or west (W) for longitude. The data stream shall be expressed as follows, DD.MM.SS.THTA_ddd.mm.ss.thtO{newline}.

- DD = latitude degrees
- MM = latitude minutes
- SS = latitude seconds
- THT = latitude milliseconds
- A = latitude, North or South
- ddd = longitude degrees
- mm = longitude minutes
- ss = longitude seconds
- tht = longitude milliseconds
- O = longitude, East or West

An example data stream 38.53.23.123N_077.00.27.123W{newline} would represent 38 degrees latitude north, with 53 minutes, 23 seconds and 123 milliseconds and 077 degrees longitude west with 00 minutes, 27 seconds and 123 milliseconds. As with the “QT”, “QC” and “QD” commands, the message “NOT LOCKED ON” shall be the response if the Model 2070-7G does not have at least one satellite in view to determine the precise position.

Please note: the “_” represent an ASCII space.

QA The “QA” command differs from the other Q commands in that it must include two additional user selected variables n1 and n2, and two fixed variables n3 and n4, which are always zero. The output from the QA command depends on the variables sent with the command. It also differs from the other Q commands in that the information returned is not ASCII but rather binary. A list of the user defined variables and the information returned follows.

User defined variables

n1– Time zone. The variable entered must be the sum of an ASCII 0 + (0 – 11) depending on the time zone desired. For example ASCII 38 signifies time zone 8, Pacific.
n2 – Daylight savings time correction, 0 = disabled, 1 = enabled.

Possible replies from the Model 2070-7G to a QA command

Byte 0

Bits 1-3 are not used.

Bit 4 is 0 if valid time is not currently available and 1 if time is valid.

Bit 5 is 1 during the initialization phase only (before first lock on, i.e. LED changes to green for the first time. This bit changes to 0 at the first lock on and never changes even in subsequent amber conditions.

Bit 6 is always 0.

Bit 7 is normally 0 but if no satellite information is received for 24 hours, this bit will be 1.

Bit 8 is not used.

Byte 1

Bits 1-4 are not used, always zero.

Bits 5-6 are always 0 indicating that the time is in 24-hour format.

Bit 7, Daylight Savings Time indicator is 1 when DST is enabled and the date is within the DST period. This bit is 0 if DST correction is disabled or the date is outside of the DST period.

Bit 8 is not used, always zero.

Bytes 2 and 3

Milliseconds portion of current time, the Hex equivalent of BCD.

Byte 4

Seconds portion of current time, the Hex equivalent of BCD.

Byte 5

Minutes portion of current time, the Hex equivalent of BCD.

Byte 6

Hours portion of current time, the Hex equivalent of BCD.

Bytes 7 and 8

Day of Year, the Hex equivalent of BCD.

Byte 9

Year (this byte is actually the offset from 1986) i.e. 18 = 2004, the Hex equivalent of BCD.

Bytes 10 and 11

Always zero.

Byte 12

Always a new line character (CR).

The "S" Commands

The Model 2070-7G shall accept instructions from the user in the form of “S” (Set) commands. The “S” commands, their variables, and their meanings that shall be supported shall consist of the following:

Model 2070-7G "S" COMMANDS				
COMMAND	NAME OF COMMAND	"n" variable	SETTING (default)	(Notes)
SB_n	SET BAUD RATE	0	Reserved	
		1	Reserved	
		2	Reserved	
		3	(1200)	
		4	2400	
		5	4800	
		6	9600	
		7	19200	
		8	38400	
SD_n	SET DAYLIGHT SAVINGS TIME	0	Disabled	
		1	(Enabled)	
SM_n	SET 12 OR 24 HOUR TIME FORMAT	0	(24 Hour)	
		1	12 Hour (AM/PM)	
SN_n	SET NEW LINE CHARACTER	ASCII characters except colon and /	(carriage return)	
SO_n	SET TIME ZONE	0	Time zone 0	UTC
		1	Time zone 1	
		2	Time zone 2	
		3	Time zone 3	
		4	Time zone 4	
		5	Time zone 5	Eastern
		6	Time zone 6	Central
		7	Time zone 7	Mountain
		8	(Time zone 8)	Pacific
		9	Time zone 9	Alaska
		: (colon)	Time zone 10	Hawaii
		; (semi-colon)	Time zone 11	
SI1bMbsbhbmeMesehem	SET DAYLIGHT SAVING TIME	bM	03	

(Begin

		month)		
	CONFIGURATION	bs (Begin Sunday)	02	
		bh (Begin hour)	02	
		bm (Begin minutes)	00	
		eM (End month)	11	
		es (end Sunday)	01	
		eh (end hour)	02	
		em (End minutes)	00	

“S” Commands

“S” Commands shall be sent to the Model 2070-7G without an “end of line” character.

The Model 2070-7G shall not send any acknowledgement when it receives an “S” command however the QM command can be used to confirm the change was made. All setting changes shall be stored in non-volatile memory and used in place of the factory default settings.

The following describes the “S” commands that shall be supported by Model 2070-7G:

SBn (Set Baud Rate). This command shall be used to change the Model 2070-7G’s serial communication speed. The baud rate of the controller and the Model 2070-7G must be the same. When the unit is first powered up it shall be configured with the factory default baud rate of 1200.

When communications between the Model 2070-7G and the controller is established, the SB command can be used to change the baud rate to the preferred speed. The available baud rates are shown in "S" Commands table. Generally the highest baud rate, that provides reliable communication, should be used. For example, to change the unit’s default baud rate to 4800 baud, the proper “S” command to send would be “SB5” (without quotation marks). Any baud rate changes will go onto effect immediately.

SDn (Enable/Disable Daylight Savings Time). This command shall be used to enable or disable the device’s one hour offset to accommodate Daylight Savings Time rules. If the

unit is to be used to output local time in an area that observes Daylight Savings Time rules, the “SD1” command should be used. The factory default setting is “Enabled”, which means the Model 2070-7G will automatically adjust the local time output by one hour at the beginning and end of the Daylight Savings Time period. Users can change the configuration when these changes must occur with the S11 command. If the unit will be used in areas that do not observe Daylight Savings Time, the appropriate “S” command to use would be “SD0”.

SMn (Set time output format). This command shall be used to specify how the time of day data will be formatted. The factory default setting is the 24 hour, Military Time, format. If the user prefers to have the data output in a 12 hour format, (with A.M. or P.M. noted) the “SM1” (without the quotation marks) command must be sent once to change the format setting.

SNn (Set new line character). The Model 2070-7G’s response to a valid “Q” command shall be a data stream that ends with a “new line” character. The default new line character is an ASCII carriage return. If the user prefers to have the data stream end in different ASCII character it can be changed using the “SN” command. Any ASCII character except the “/” (slash) and the “:” (colon) characters may be used as the variable. For example to use “#” as the new line character the proper command to send would be “SN#” (without the quotation marks). Only one “new line character” is permitted.

SO n (Set time zone). This command allows the user to set the Model 2070-7G’s output to reflect the local time. Each time zone is assigned a number or ASCII character that is used as the variable for the “SO” command. The Model 2070-7G firmware shall accommodate time zones 0 through 11. Time zone 0 shall be used to output UTC (Universal Coordinated Time) or GMT (Greenwich Mean Time) if the user prefers that reference instead of local time. The default factory value shall be 8, as listed under default configurations, which shall represent Pacific Standard Time in the United States.

S11bMbsbhbmeMesehem (Set daylight saving time parameters). This command shall allow the user to set the Model 2070-7G’s daylight saving time settings. The modification of these parameters will determine when DST begin & end:

- **Begin Month(bM)**. The month when starts to observe the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
- **Begin Sunday(bs)**. The Sunday number of “begin month (bM)”. This value shall be a two digits number.
- **Begin Hour(bh) and Begin Minutes(bm)**. The time when starts to observe the DST. This time shall be expressed in a 24 hour format.
- **End Month(eM)**. The month when ends the DST changes. This value shall be a two digits number. 01 means January, 02 February, 03 March and so on.
- **End Sunday(es)**. The Sunday number of “end month(eM)”. This value shall be a two digits number.

- End Hour(eh) and End Minutes(em). The time when the DST observation ends. This time shall be expressed in a 24 hour format.

These parameters shall be set in the Non-Volatile memory.

10.9.5 Config Mode

The Model 2070-7G Module shall be provided with a switch allowing the user to switch Com 2 into Config Mode. In Config Mode, Com 2 loops back to the GPS Receiver and provides the user with a communications port to run Q and S Commands to configure the GPS receiver or query it for data. During Config Mode, the Config Mode LED indicator shall be turn ON to indicate configuration mode. When the Config Model is OFF, Com 2 shall consist of a serial port (serial pass through) to the Model 2070 Controller.

10.9.6 Connectors

The Model 2070-7G Universal Time Base Module shall contain the following connectors in the Faceplate:

Antenna	SMA Connector
Com 2 Port (C22S)	DB9 Female Connector

10.9.7 Data Output

When communicating to the GPS Receiver, the Date, Time, Day of Week, Signal Status, and Global Position shall be available. Data format shall be as defined in Section 10.9.4 of these specifications and the NMEA 0183 Standard. Serial Communications shall be software selectable at 1200, 2400, 4800, 9600, 19200 or 38400 bps.

10.9.8 Protocols

The Model 2070-7G shall support the NMEA 0183 Standard, Version 2.1 or later, as defined by the National Marine Electronics Association and the QC Command Set as defined in Section 10.9.4 of these specifications. A dipswitch marked "CMode" shall be provided which allows for the selection of one of three modes. The communication modes shall consist of a "NORM" (Normal Mode), "NB" (Normal Broadcast Mode) and GPS. When the CMode is in the "NORM" (Normal Mode) ON position, the Model 2070-7G shall respond to the QS command set as defined elsewhere in these specifications. When the dipswitch CMode is in the "NB", (Normal Broadcast Mode) ON Position, and the Model 2070-7G shall operate in a broadcast mode and shall not

respond to the QS command set. When operating in the NB mode, the Model 2070-7G shall use the default settings as defined in section 10.9.2.

When the CMode is in the "GPS", (GPS pass through mode) ON position, the Model 2070-7G shall act like a standard NMEA 0183 compliant GPS receiver. As a minimum, when set on GPS mode, the Model 2070-7G shall support the following NMEA 2.0 Standard sentences: RMC, GGA, GSA, GSV, GLL and ZDA. The sentences shall be preceded by the standard generic Global Positioning System (GPS) talker ID "GP".

=== GLL - Geographic Position - Latitude/Longitude ===

	1	2	3	4	5	6	7	8
\$-- GLL	,lll.ll	,a	,yyyy.yy	,a	,hhmmss.ss	,a	,m	,*hh

\$--GLL,lll.ll,a,yyyy.yy,a,hhmmss.ss,a,m,*hh<CR><LF>

Field Number:

1. Latitude
2. N or S (North or South)
3. Longitude
4. E or W (East or West)
5. Universal Time Coordinated (UTC)
6. Status A - Data Valid, V - Data Invalid
7. FAA mode indicator (NMEA 2.3 and later)
8. Checksum

=== GGA - Global Positioning System Fix Data ===

Time, Position and fix related data for a GPS receiver.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
--	---	---	---	---	---	---	---	---	---	----	----	----	----	----	----

\$-- GGA	,hhmmss.ss	,llll.ll	,a	,yyyyy.yy	,a	,x	,xx	,x.x	,x.x	,M	,x.x	,M	,x.x	,xxxx	*hh
-------------	------------	----------	----	-----------	----	----	-----	------	------	----	------	----	------	-------	-----

\$--GGA,hhmmss.ss,llll.ll,a,yyyyy.yy,a,x,xx,x.x,x.x,M,x.x,M,x.x,xxxx*hh<CR><LF>

Field Number:

1. Universal Time Coordinated (UTC)
2. Latitude
3. N or S (North or South)
4. Longitude
5. E or W (East or West)
6. GPS Quality Indicator,
 - 0 - fix not available,
 - 1 - GPS fix,
 - 2 - Differential GPS fix
(values above 2 are 2.3 features)
 - 3 = PPS fix
 - 4 = Real Time Kinematic
 - 5 = Float RTK
 - 6 = estimated (dead reckoning)
 - 7 = Manual input mode
 - 8 = Simulation mode
7. Number of satellites in view, 00 - 12
8. Horizontal Dilution of precision (meters)
9. Antenna Altitude above/below mean-sea-level (geoid) (in meters)
10. Units of antenna altitude, meters
11. Geoidal separation, the difference between the WGS-84 earth ellipsoid and mean-sea-level (geoid), "-" means mean-sea-level below ellipsoid
12. Units of geoidal separation, meters
13. Age of differential GPS data, time in seconds since last SC104 type 1 or 9 update, null field when DGPS is not used
14. Differential reference station ID, 0000-1023
15. Checksum

Example:

\$GPGGA,180844.000,3211.10532,N,11055.20380,W,0,00,99.0,779.59,M,-27.7,M, ,*69

=== RMC - Recommended Minimum Navigation Information ===

	1	2	3	4	5	6	7	8	9	10	11	12	13
\$-- RMC	,hhmmss.ss	,A	,llll.ll	,a	,yyyy.yy	,a	,x.x	,x.x	,xxxx	,x.x	,a	,m	*hh

\$--RMC,hhmmss.ss,A,llll.ll,a,yyyy.yy,a,x.x,x.x,xxxx,x.x,a,m*hh<CR><LF>

Field Number:

1. UTC Time
2. Status, V=Navigation receiver warning A=Valid
3. Latitude
4. N or S
5. Longitude
6. E or W
7. Speed over ground, knots
8. Track made good, degrees true
9. Date, ddmmyy
10. Magnetic Variation, degrees
11. E or W
12. FAA mode indicator (NMEA 2.3 and later)
13. Checksum

A status of V means the GPS has a valid fix that is below an internal quality threshold, e.g. because the dilution of precision is too high or an elevation mask test failed.

Example:

\$GPRMC,180845.000,V,3211.105,N,11055.204,W,0.0,0.0,271009,9.4,E*6E

=== ZDA - Time & Date - UTC, day, month, year and local time zone ===

	1	2	3	4	5	6	7
\$-- ZDA	,hhmmss.ss	,xx	,xx	,xxxx	,xx	,xx	*hh

\$--ZDA,hhmmss.ss,xx,xx,xxxx,xx,xx*hh<CR><LF>

Field Number:

1. UTC time (hours, minutes, seconds, may have fractional subsecond)
2. Day, 01 to 31
3. Month, 01 to 12
4. Year (4 digits)
5. Local zone description, 00 to +- 13 hours
6. Local zone minutes description, apply same sign as local hours
7. Checksum

Example: \$GPZDA,160012.71,11,03,2004,-1,00*7D

10.9.9 LED Indicators

Function	LEDs
Com 1	TxD RxD
Com 2	TxD RxD
Config Mode	Green or Red
Tracking	Tri-Color

10.9.10 Model 2070-7G Tracking

The Model 2070-7G Universal Time Base Module shall be provided with the following tracking functionality:

The Model 2070-7G shall be equipped with a tri-color LED (Light Emitting Diode) to indicate the unit's status during operation; the LED shall be located at the faceplate and labeled as TRACKING as shown in detail A10-9.

The various states of the TRACKING LED indicator and their meanings shall be as described in the section below.

Power up phase: At power up, the 2070-7G's microprocessor shall read the five parameters stored in the unit's non-volatile memory. These parameters are Baud Rate, Daylight Savings Time mode and configuration, Time Zone, Military Time format and new line character. The default values shall be read from memory if they have not been modified. Next, the communications port shall be initialized and the speed set to the stored baud rate parameter. The remaining three communications parameters shall be fixed at 8 data bits, no parity and 1 stop bit.

The power up process shall take approximately 200 milliseconds. During this period the unit may not respond to any "S" or "Q" commands and the LED will **start flashing green**.

GPS initialization phase: After the power up phase is complete the unit will query the GPS receiver to see if it is already initialized. This is usually the case when the unit is powered up. If there is not data output, the GPS receiver will be initialized by the firmware program, using initialization commands and known variables.

This process shall take approximately 1 second. During this period, the Model 2070-7G may not respond to any "Q" or "S" commands and the LED shall **flash red**, once per second.

Signal acquisition phase: Once the GPS initialization phase is complete, it shall take from 3 to 180 seconds for the unit to acquire and process the first satellite's signal. When the Model 2070-7G has received and processed the first satellite's information, unsynchronized time/date information shall be available using the "QC" data stream and the synchronization character shall be "N". When the synchronization character is "N", the "QC", and "QT" and "QD" replies will be complete but time is not fully synchronized to UTC.

When unsynchronized data is available, the LED shall **flash green and red**.

Fully synchronized phase: When the 2070-7G has acquired information from 4 satellites its output will be synchronized to UTC (Universal Coordinated Time). When the unit is synchronized to UTC it is said to be "LOCKED ON". At this point the "QT", "QD", "QL" and "QC" replies will contain the most accurate information (time and location) possible.

When the unit is fully synchronized (LOCKED ON), the synchronization character shall the letter "Y" in the "QC" data stream and the LED indicator shall be **solid green and red flashing** once per second.

10.9.11 Power Requirements

The power requirements of the Model 2070-7G Universal Time Base Module shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.9.12 Environmental

The Model 2070-7G Universal Time Base Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.9.13 Form Factor

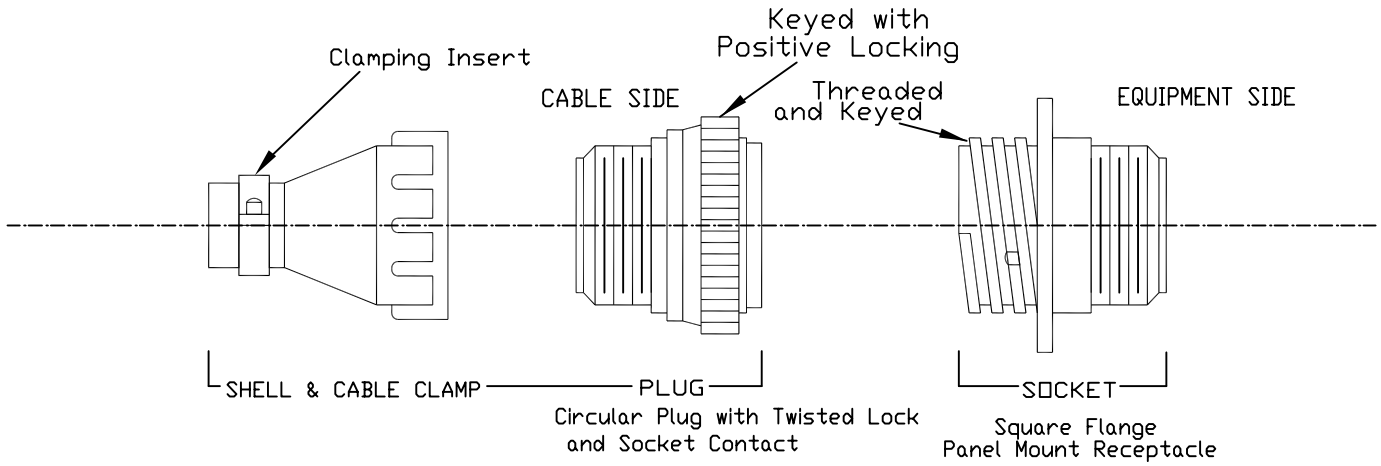
See A10-9 for Details

APPENDIX A
CHAPTER DETAILS

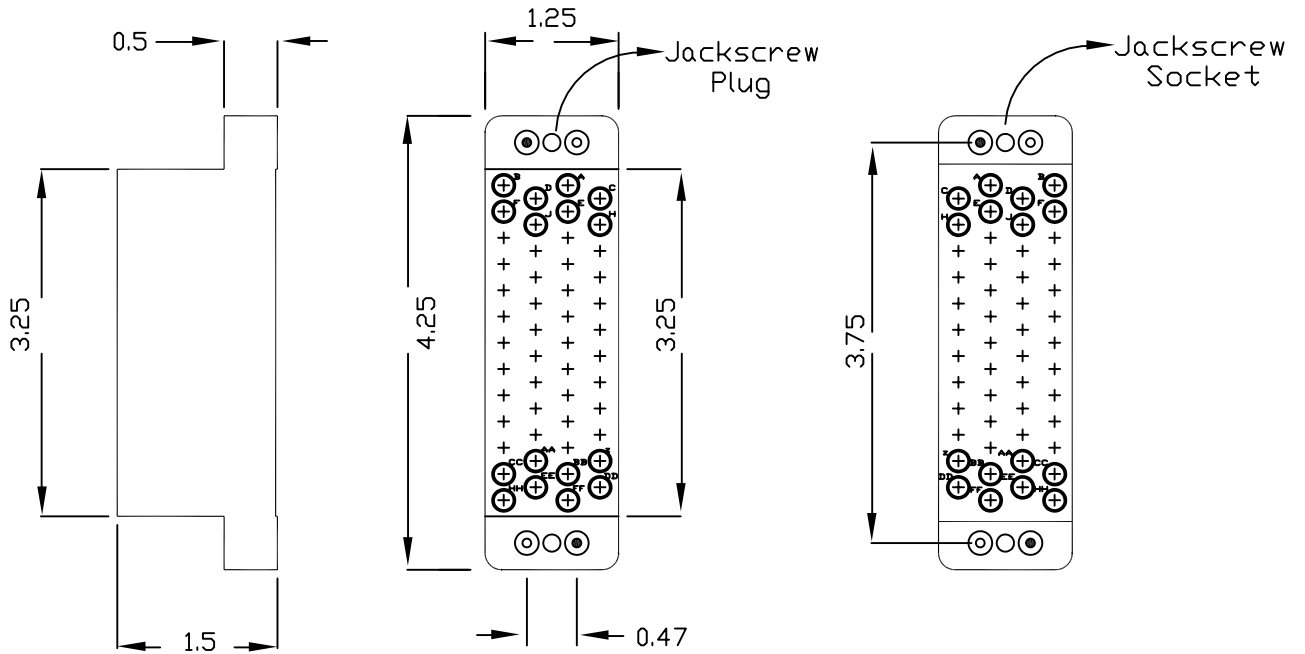
**APPENDIX A1
CHAPTER 1 DETAILS**

M104 – Connector
M50 & Circular Plastic Connectors

A1-1
A1-2



PLASTIC CIRCULAR PLUG AND SOCKET CONNECTOR



CONNECTOR PIN ARRANGEMENT

NOTES:

1. Guide Pins & Sockets, and Jackscrews are centered symmetrical to connector.
2. Key: - socket
- plug
3. All dimensions shown are in inches.

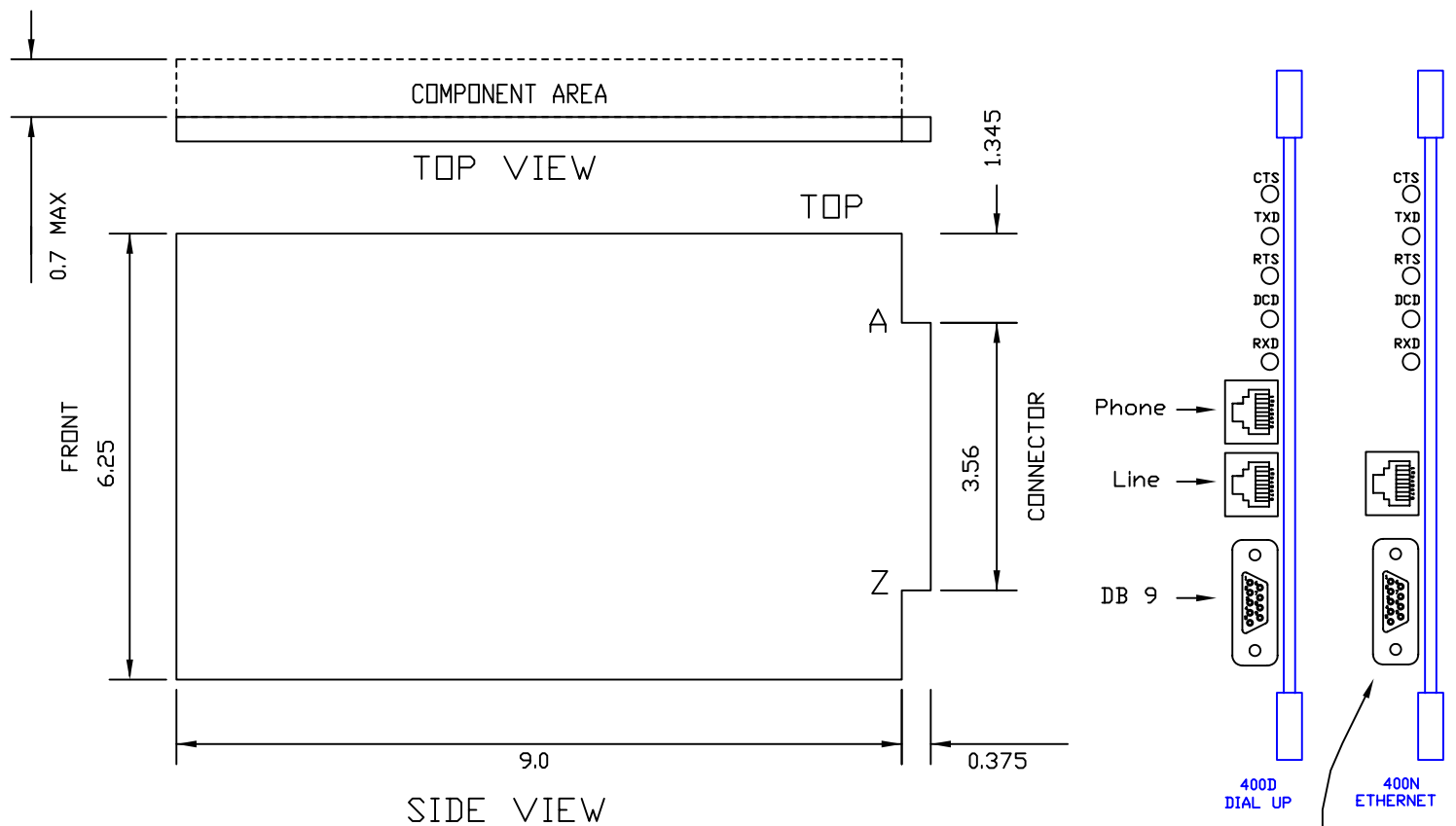
TITLE: CONNECTOR DETAIL M50 & CIRCULAR PLASTIC CONNECTOR	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A1-2

APPENDIX A2
CHAPTER 2 DETAILS

Model 170E Controller Unit Diagram	A2-1
Model 170E Controller Unit Block Diagrams	A2-2
Model 170E Input Port Address	A2-3
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Model 400, 400B and 400BE Modem	A2-5
Model 412C Program Module & Connectors M170 & M170E	A2-6
Model 400D Dial-Up and 400N Ethernet Module	A2-7
Model 400F Fiber Module	A2-8

NOTES:

1. Program module' height and width dimensions are maximum.
2. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.
3. All function under connector C2 & the terminal block T-1 are in reference to the MODEM
4. Detail Definitions:
 - BL** = BLANKING
 - CC** = CHARACTER CONTROL OR STROBE
 - CD** = CARRIER DETECT
 - CH** = CHARACTER
 - CTS** = CLEAR TO SEND
 - DP** = DECIMAL POINT
 - LS** = LEAST SIGNIFICANT
 - MS** = MOST SIGNIFICANT
 - NA** = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
 - NLS** = NEXT LEAST SIGNIFICANT
 - NMS** = NEST MOST SIGNIFICANT
 - P&I** = PHASE AND INTERVAL
 - RTS** = REQUEST TO SEND



CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA

DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

RJ45 ETHERNET PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	NA
3	RX +	7	NA
4	RX-	8	NA

NOTE:

All dimensions shown are in inches.

TITLE:

MODEL 400D & 400N

1-21-2010, ERRATA 1

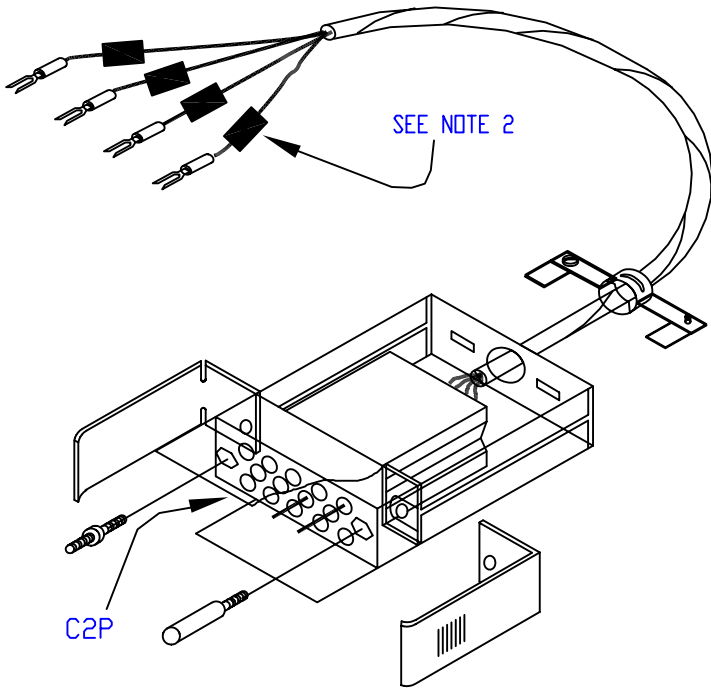
NO SCALE

TEES 2009

A2-7

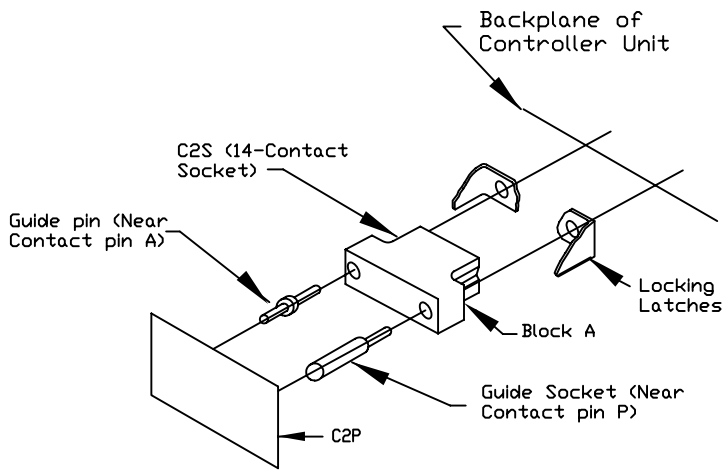
**APPENDIX A3
CHAPTER 3 DETAILS**

Model 200 Switch Pack, 204 & 205 CONNECTOR DETAILS	A3-1
Model 208 T170 Monitor Units	A3-2
Model 210 T170 Monitor Unit	A3-3
Model 210 T170 Monitor Unit	A3-4
Programming Card Connector & Wiring Assignments	
C2 Modem Harness	A3-5
Model 206L Power Supply	A3-6
C11 Harness	A3-7
C2 Serial Harness	A3-8

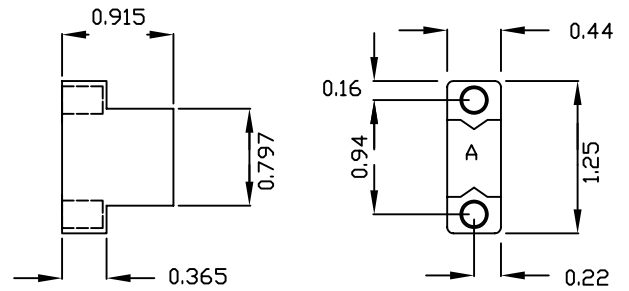


C2 MODEM HARNESS

C2P CONNECTOR ASSIGNMENT			
PIN	FUNCTION	PAIR	WIRE COLOR
A	AUDIO IN	PAIR 2	WHITE
B	AUDIO IN		GREEN
C	AUDIO OUT	PAIR 1	RED
E	AUDIO OUT		BLACK



CONNECTOR C2 DETAIL



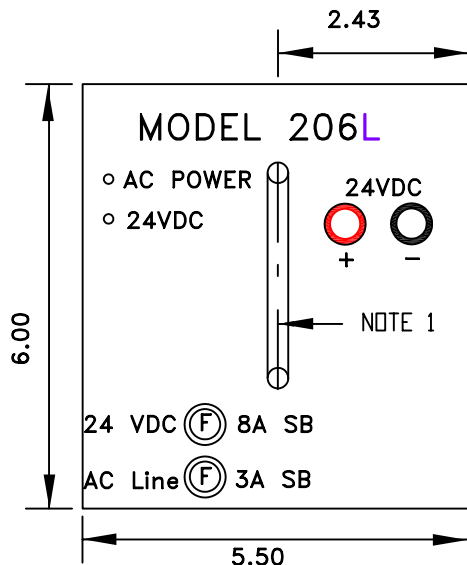
CONNECTOR C2S

NOTES:

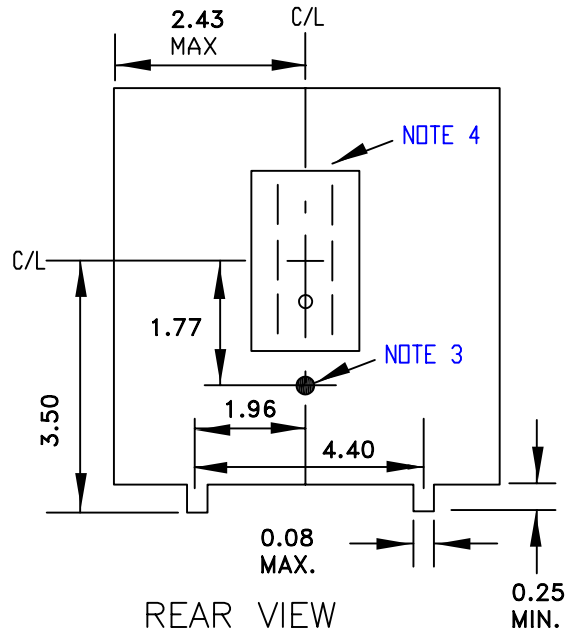
1. Cable length shall be 36.00in minimum. The cable shall be 2-pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.
2. Each conductor (AUDIO IN or AUDIO OUT) shall be labeled.
3. All dimensions shown are in inches.

TITLE: C2 MODEM HARNESS	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A3-5

MODEL 206L POWER SUPPLY MODULE

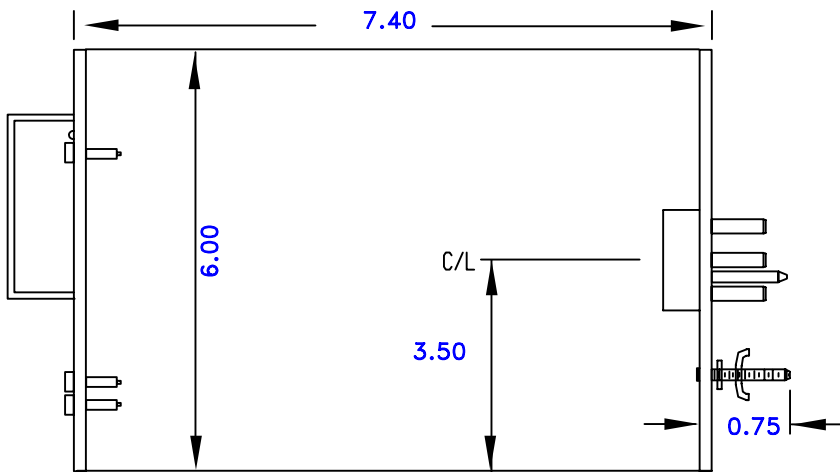


FRONT VIEW

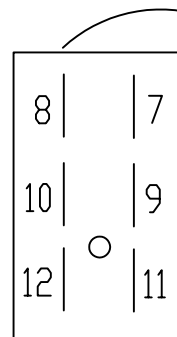


REAR VIEW

POWER SUPPLY MODULE WIRING DETAIL



SIDE VIEW



REAR VIEW

PIN NO.	CIRCUIT
7	+24 VDC
8	DC GND
9	EQUIPMENT GND
10	NA
11	AC- CLEAN
12	AC+ CLEAN

NOTE:

- "U" sharpened rod handle fabricated of 0.25 ± 0.05 diameter, aluminum stock, with 4.00 ± 0.125 length, & rod center to center, shall be provided. The handle shall be vertically centered. The depth from the vertical centerline of the handle rod to the module from panel shall be 1.25 ± 0.125 .
- The power supply module dimension, from panel to connector plug, shall be $7.375 + 0.000, -0.125$
- A standard 8-32 metal stud retaining screw shall provide proper securing of the power supply when installed in the PDA using washers and a wingnut.
- Connector BEAU P-5406 or equivalent.
- All dimensions shown are in inches.

TITLE:

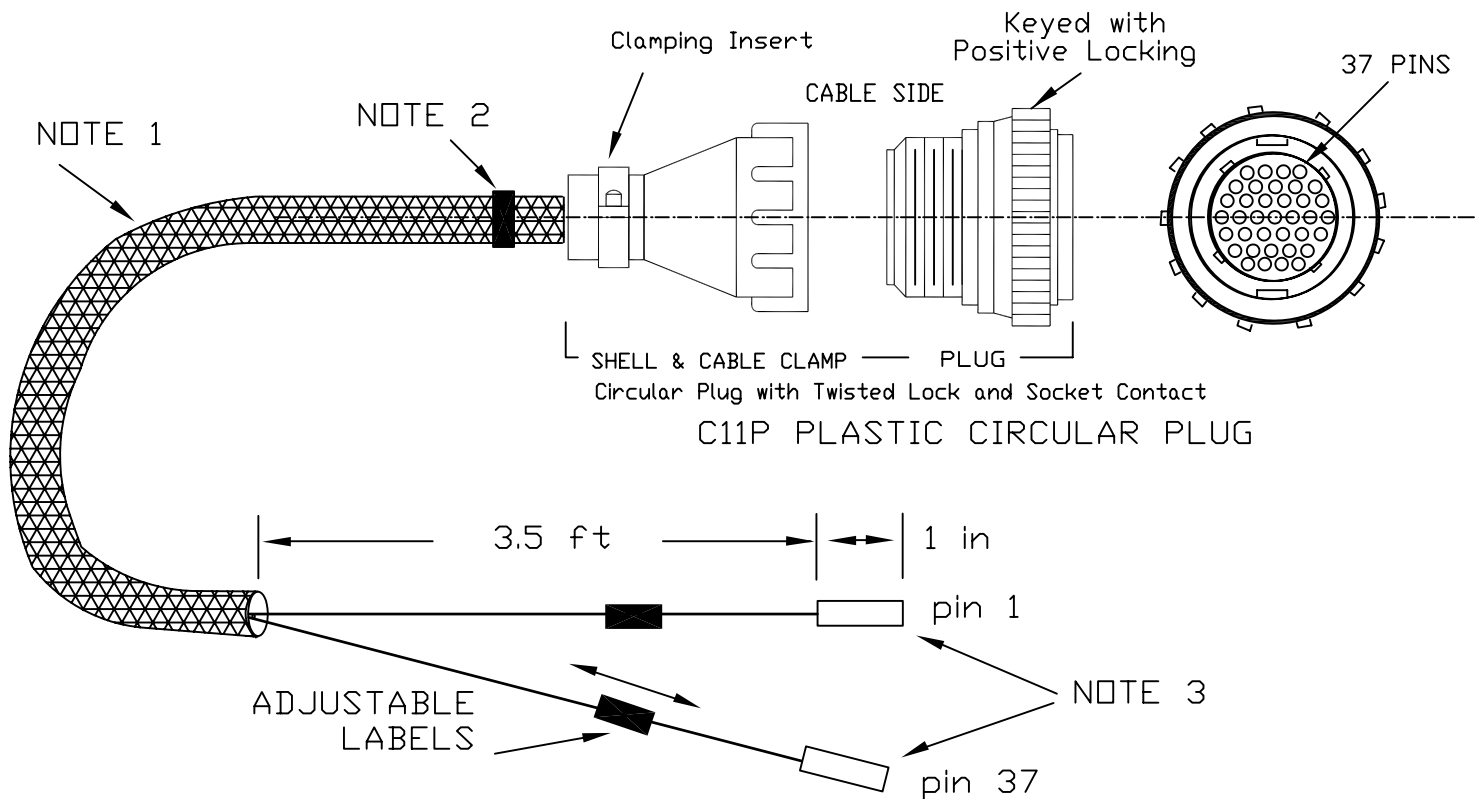
MODEL 206L POWER SUPPLY

1-21-2010, ERRATA 1

NO SCALE

TEES 2009

A3-6



C11P PIN ASSIGNMENT & LABELS

PIN 1	08-1	PIN 11	14-2	PIN 21	17-7	PIN 31	DCG #2
PIN 2	08-2	PIN 12	14-3	PIN 22	17-8	PIN 32	NC
PIN 3	08-3	PIN 13	14-4	PIN 23	18-1	PIN 33	NC
PIN 4	08-4	PIN 14	DCG #2	PIN 24	18-2	PIN 34	NC
PIN 5	08-5	PIN 15	17-1	PIN 25	18-3	PIN 35	NC
PIN 6	08-6	PIN 16	17-2	PIN 26	18-4	PIN 36	NC
PIN 7	08-7	PIN 17	17-3	PIN 27	18-5	PIN 37	NC
PIN 8	08-8	PIN 18	17-4	PIN 28	18-6		
PIN 9	DCG #2	PIN 19	17-5	PIN 29	18-7		
PIN 10	14-1	PIN 20	17-6	PIN 30	18-8		

TABLE 1

NOTES:

1. The C11 Harness shall be a minimum of 7.5ft in length. Four feet of the harness wire bundle shall be provided with external protection. The conductors shall be compliant to section 6.5.2
2. The connectorized end of the C11 harness shall be labeled as C11.
3. Each conductor of the loose end of the C11 Harness shall be labeled with the port assignment as indicated in Table 1. Each end of the conductors shall be cover with one inch of heat shrinkable tubing.
4. The C11P circular plastic connector shall have quick connect/disconnect capability with thread assist, positive detent coupling. The connector shall be UL Recognized, UL 94 V-1 rated and made of stabilized, heat resistant, self-extinguishing thermoplastic material.
5. The manufacturer shall be provide a bag with 45 #8 stud spring spades for each C11 harness.

TITLE:

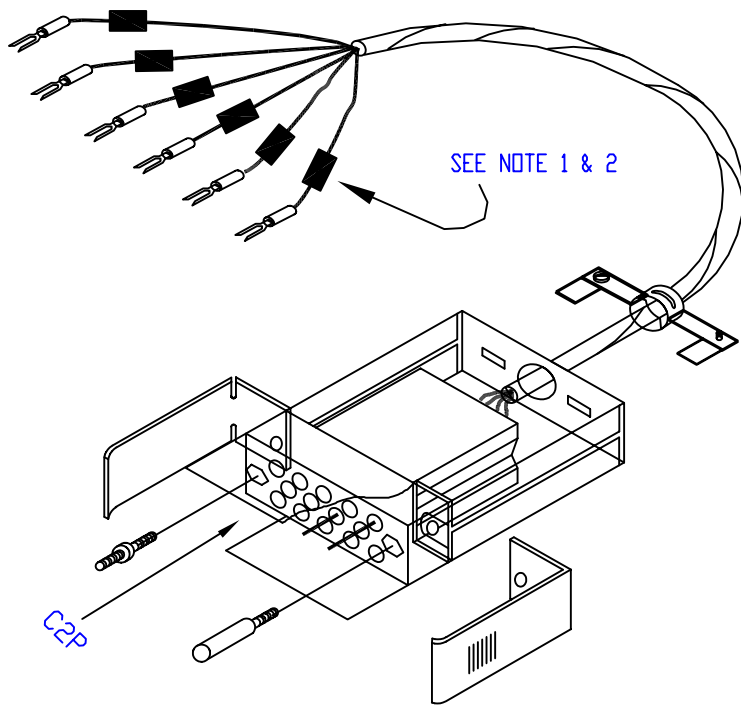
C11 HARNESS

1-21-2010, ERRATA 1

NO SCALE

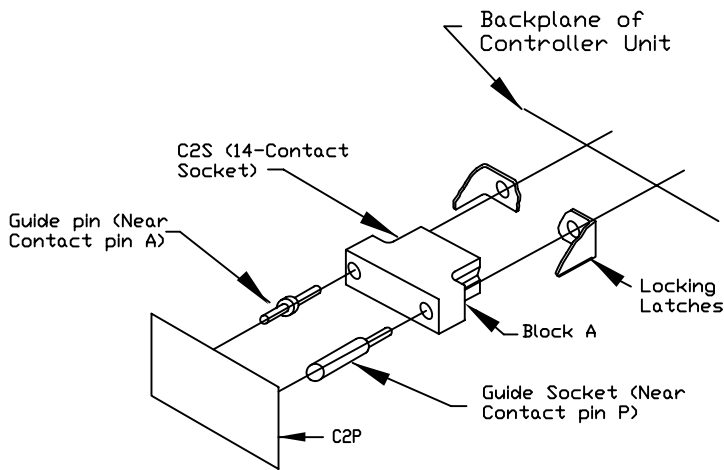
TEES 2009

A3-7

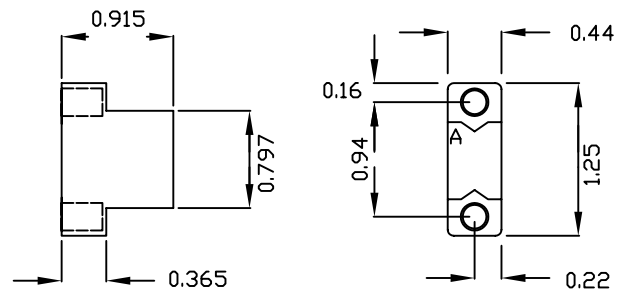


C2 SERIAL HARNESS

C2P CONNECTOR ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
A	NA	J	RTS
B	NA	K	RXD
C	NA	L	TXD
D	NA	M	CTS
E	NA	N	GND
F	NA	P	NA
H	DCD	R	NA



CONNECTOR C2 DETAIL



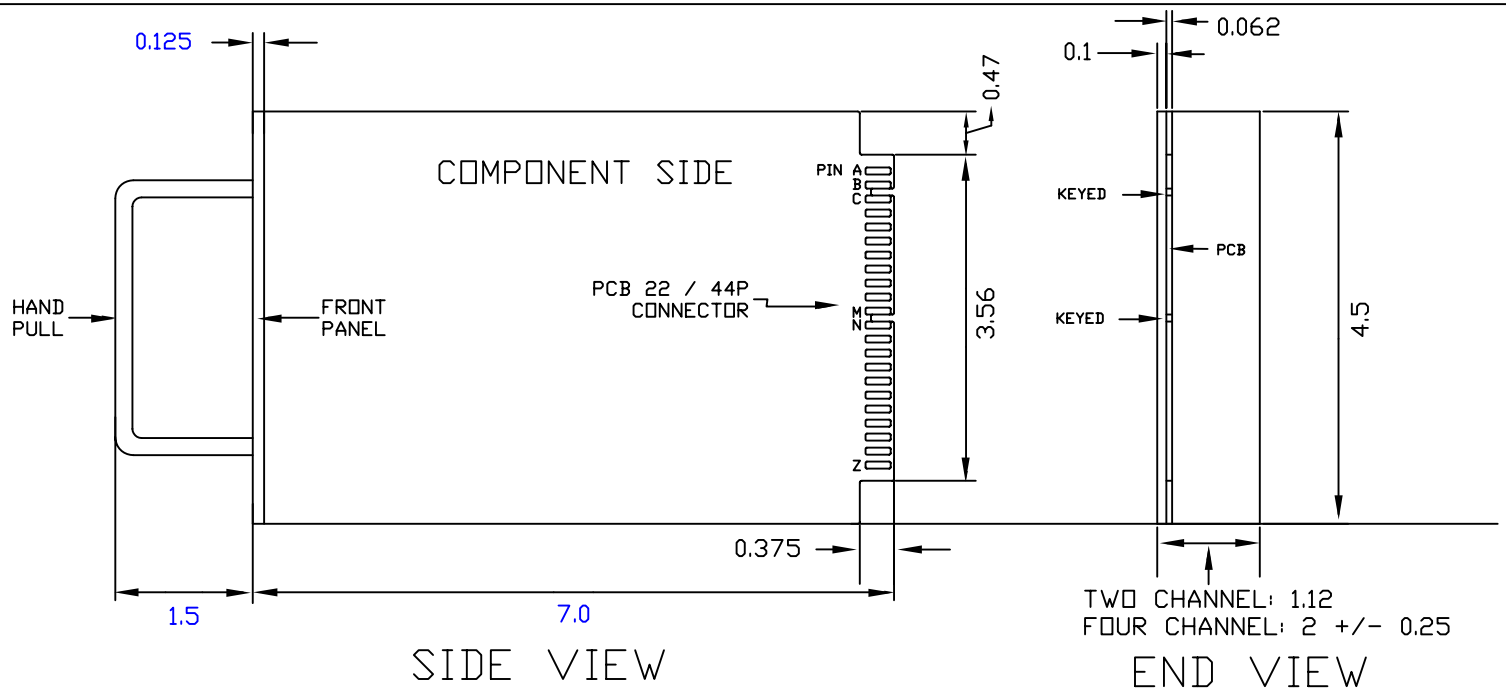
CONNECTOR C2S

NOTES:

1. Cable length shall be 36.00in minimum. The cable shall be 24AWG, 6 conductors, Belden 9536 or equal. The field end connections shall be #6 stud spring spade type.
2. Each conductor (DCD, RTS, RXD, TXD, CTS, GND) shall be labeled.
3. All dimensions shall be inches.

TITLE:		C2 SERIAL HARNESS	
1-21-2010, ERRATA 1		NO SCALE	
TEES 2009		A3-8	

**APPENDIX A5
CHAPTER 5 DETAILS**



MODEL 222, 224 & 232
CONNECTOR ASSIGNMENTS

PIN	FUNCTION (SENSORS)
A	DC GROUND
B	+24 VDC

*C	DETECTOR RESET
D	INPUT #1
E	INPUT #1
F	OUTPUT #1 (C)
H	OUTPUT #1 (E)
J	INPUT #2
K	INPUT #2
L	EQUIPMENT GROUND
M	AC-

N	AC+
P	INPUT #3
R	INPUT #3
S	OUTPUT #3 (C)
T	OUTPUT #3 (E)
U	INPUT #4
V	INPUT #4
W	OUTPUT #2 (C)
X	OUTPUT #2 (E)
Y	OUTPUT #4 (C)
Z	OUTPUT #4 (E)

MODEL 242 & 252
CONNECTOR ASSIGNMENTS

PIN	FUNCTION (ISOLATORS)
*A	DC GROUND
*B	+24 VDC

C	NA
D	INPUT #1
E	INPUT #1
F	OUTPUT #1 (C)
H	OUTPUT #1 (E)
J	INPUT #2
K	INPUT #2
L	EQUIPMENT GROUND
M	AC-

N	AC+
P	NA
R	NA
S	NA
T	NA
U	NA
V	NA
W	OUTPUT #2 (C)
X	OUTPUT #2 (E)
Y	NA
Z	NA

NOTES:

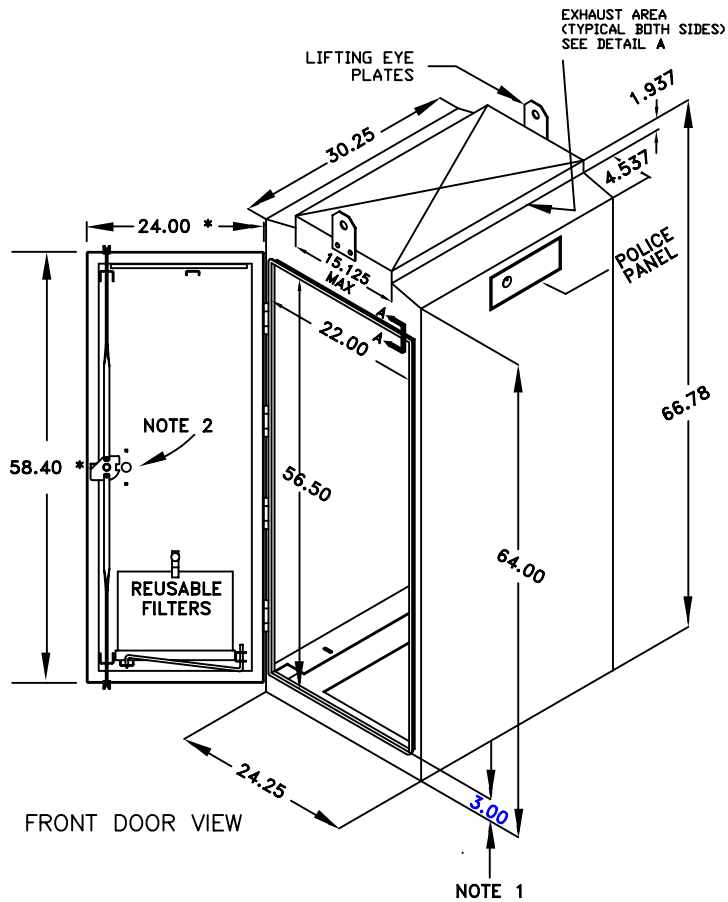
1. Tolerance dimensions are +/-0.02 in except as noted
2. Sheet definitions:
 ----= Slotted for keying
 (C) = Collector
 (E) = Emitter
 * = NA for these connections on Models 232 & 242
3. "U" shape rod handle shall be fabricate of 0.18 in to 0.26 in diameter stock.
4. All dimensions shall be in inches.

TITLE: SENSOR UNIT AND ISOLATOR DETAILS	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A5-1

APPENDIX A6
CHAPTER 6 DETAILS

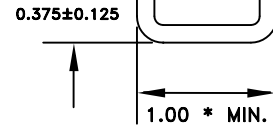
Cabinet Housing Details - sheet 1 of 4	A6-1
Cabinet Housing Details - sheet 2 of 4	A6-2
Cabinet Housing Details - sheet 3 of 4	A6-3
Cabinet Housing Details - sheet 4 of 4	A6-4
Cabinet Equipment Mounting Details	A6-5
Drawer Shelf Details	A6-6
Model 332L and 336L One Line Diagram	A6-7
SSR Installation Details	A6-8
Model 334L One Line Diagram	A6-9
Service Panel Assembly Details – sheet 1 of 3	A6-10
Service Panel Assembly Details – sheet 2 of 3	A6-11
Service Panel Assembly Details - sheet 3 of 3	A6-12
PDA #2L & #3L Details – sheet 1 of 3	A6-13
PDA #2L & #3L Details – sheet 2 of 3	A6-14
PDA #2L & #3L Details – sheet 3 of 3	A6-15
Input/Output Files Details - sheet 1 of 5	A6-16
Input/Output Files Details - sheet 2 of 5	A6-17
Input/Output Files Details - sheet 3 of 5	A6-18
Input/Output Files Details - sheet 4 of 5	A6-19
Input/Output Files Details - sheet 5 of 5	A6-20
Side Panel Details - sheet 1 of 4	A6-21
Side Panel Details - sheet 2 of 4	A6-22
Side Panel Details - sheet 3 of 4	A6-23
Side Panel Details - sheet 4 of 4	A6-24
Harness Wiring Details - sheet 1 of 5	A6-25
Harness Wiring Details - sheet 2 of 5	A6-26
Harness Wiring Details - sheet 3 of 5	A6-27
Harness Wiring Details - sheet 4 of 5	A6-28
Harness Wiring Details - sheet 5 of 5	A6-29
Fan and Thermostat Details	A6-30

CABINET HOUSING 1B



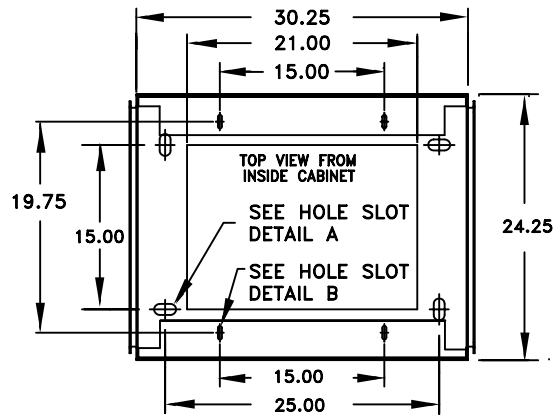
DETAIL A CABINET HOUSING 1B & 2 VENTILATION EXHAUST DETAIL

SECTION A-A CABINET HOUSING 1B & 2 FLANGE AROUND DOOR OPENING

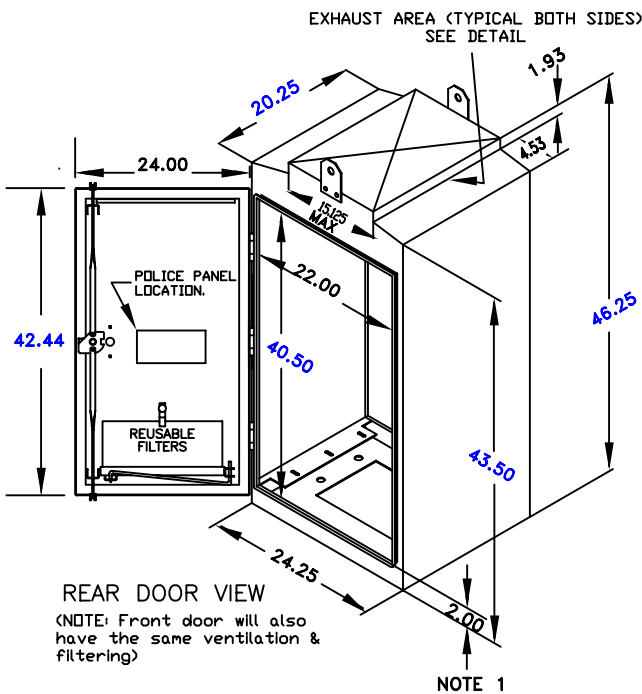


* TOLERANCE +0.0625, -0

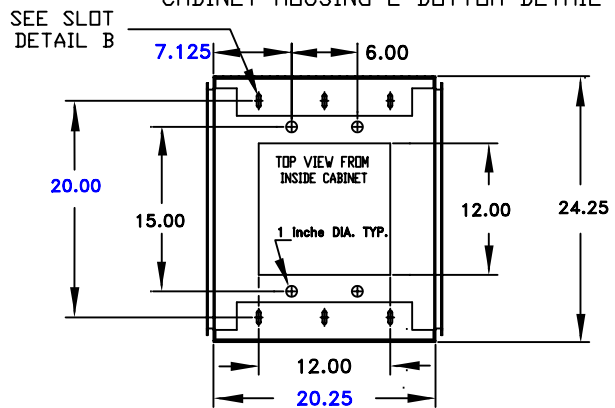
CABINET HOUSING 1B BOTTOM DETAIL



CABINET HOUSING 2

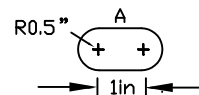


CABINET HOUSING 2 BOTTOM DETAIL



NOTE: ALL HOLE PATTERNS CENTERED ON CABINET BOTTOMS.

Hole slot detail



0.375"x1.25" □BROUND

NOTE:

1. Cabinet base to door opening.
2. The locks & handles shall be on left side of the front door & the right side of the rear door (viewed externally)
3. All dimensions shown are in inches.

TITLE:

CABINET HOUSING DETAILS SHEET 1 OF 4

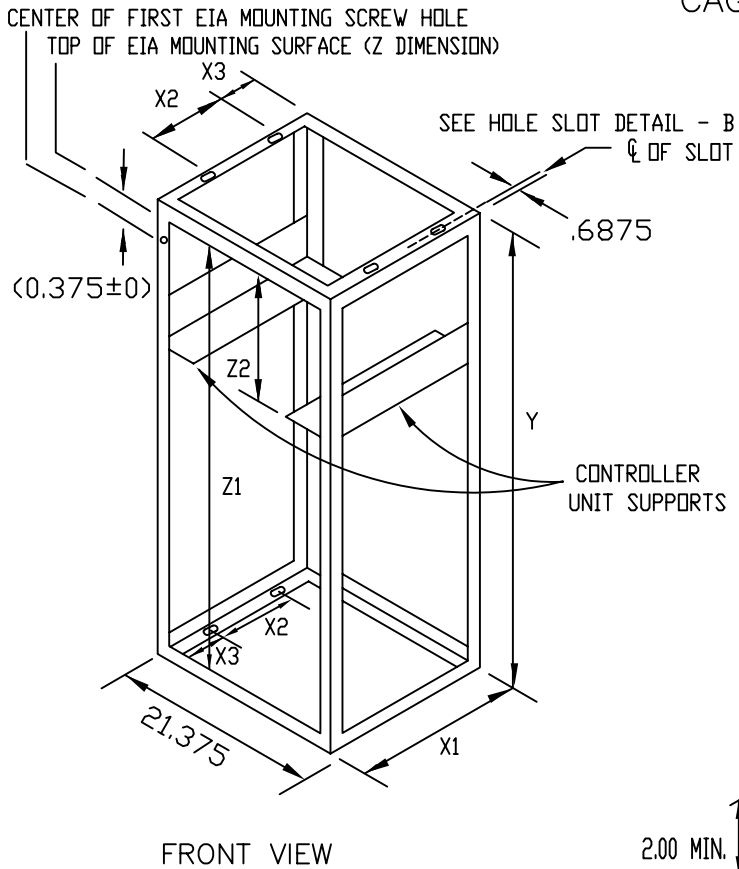
1-21-2010, ERRATA 1

NO SCALE

TEES 2009

A6-1

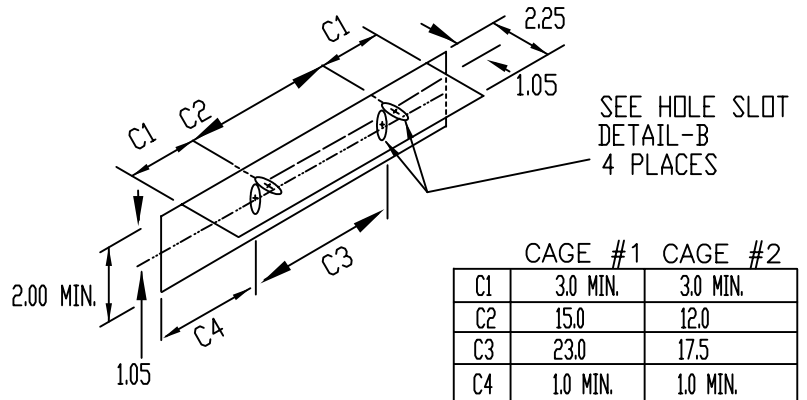
CAGE SUPPORT DETAIL



CABINET CAGE DIMENSIONS

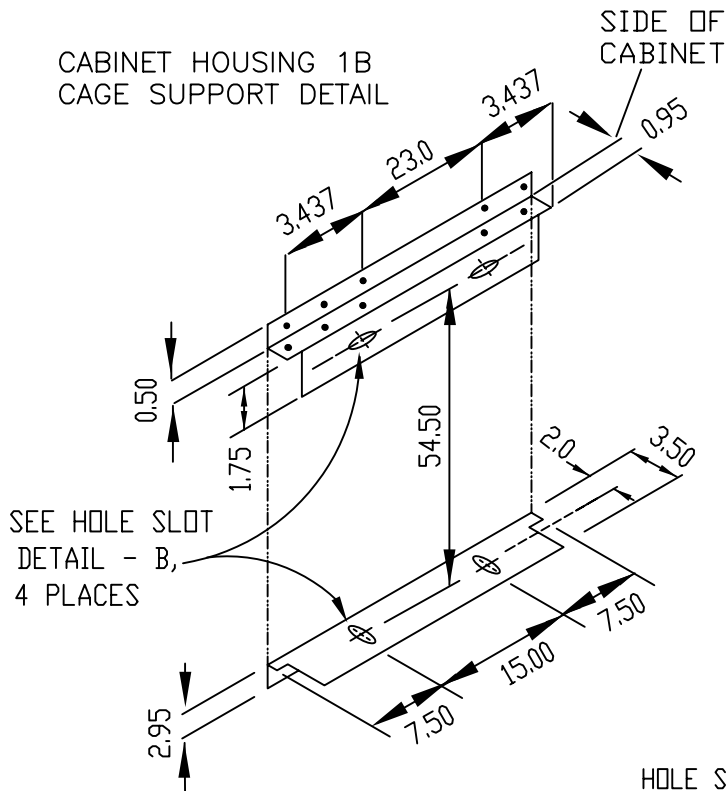
	CAGE #1	CAGE #2
X1	21.375	16.00
X2	15.00	12.00
X3	3.188	2.00
Y	55.50	40.00
Z1	53.00 MIN.	39.00 MIN.
Z2	15.75	7.25

SPACER BRACKET DETAIL

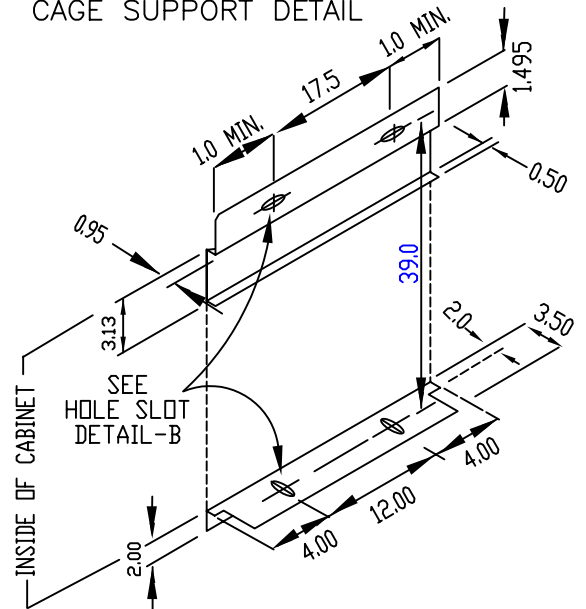


	CAGE #1	CAGE #2
C1	3.0 MIN.	3.0 MIN.
C2	15.0	12.0
C3	23.0	17.5
C4	1.0 MIN.	1.0 MIN.

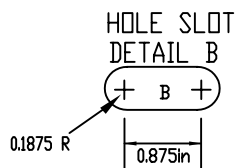
CABINET HOUSING 1B CAGE SUPPORT DETAIL



CABINET HOUSING 2 CAGE SUPPORT DETAIL



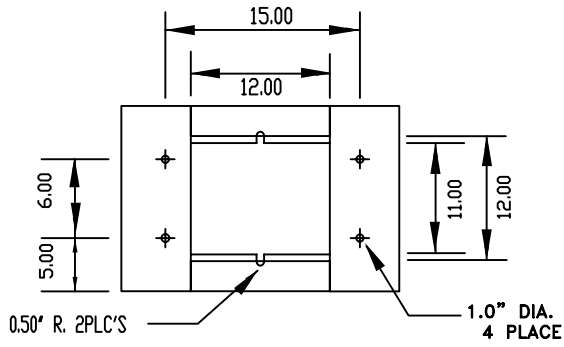
NOTE:
All dimensions shown are in inches



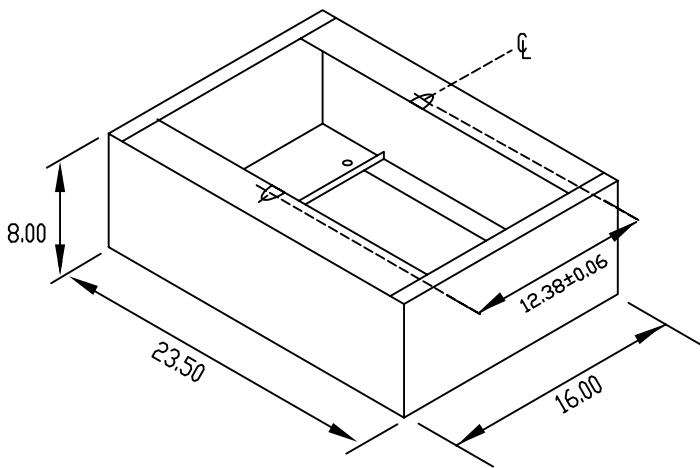
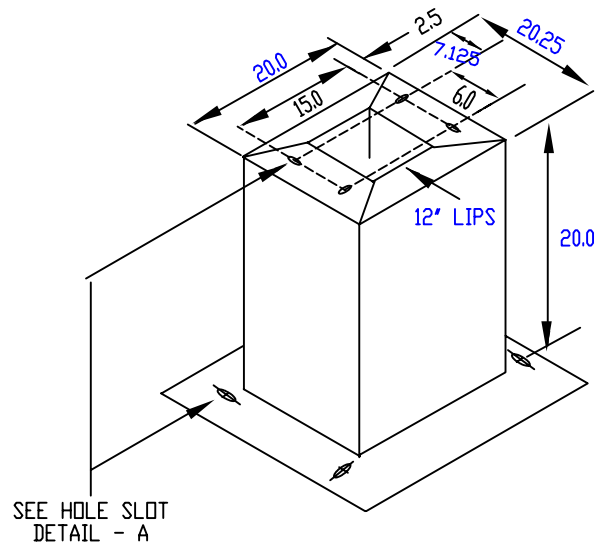
TITLE: CABINET HOUSING DETAILS SHEET 2 OF 4	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-2

TYPE 332/336 ADAPTOR

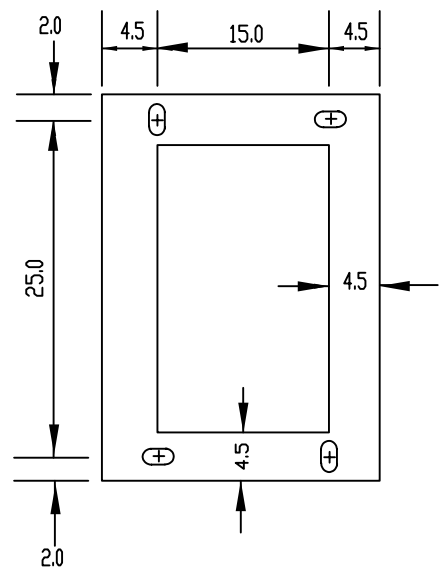
CABINET HOUSING 2
"M" BASE ADAPTOR DETAIL



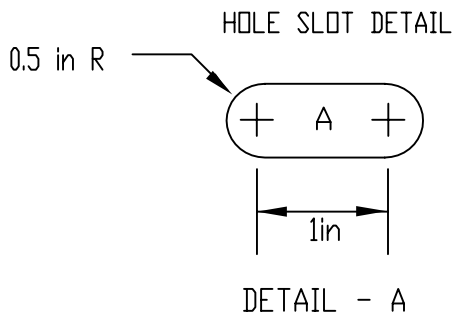
TOP VIEW



BOTTOM VIEW



332 BASE VIEW

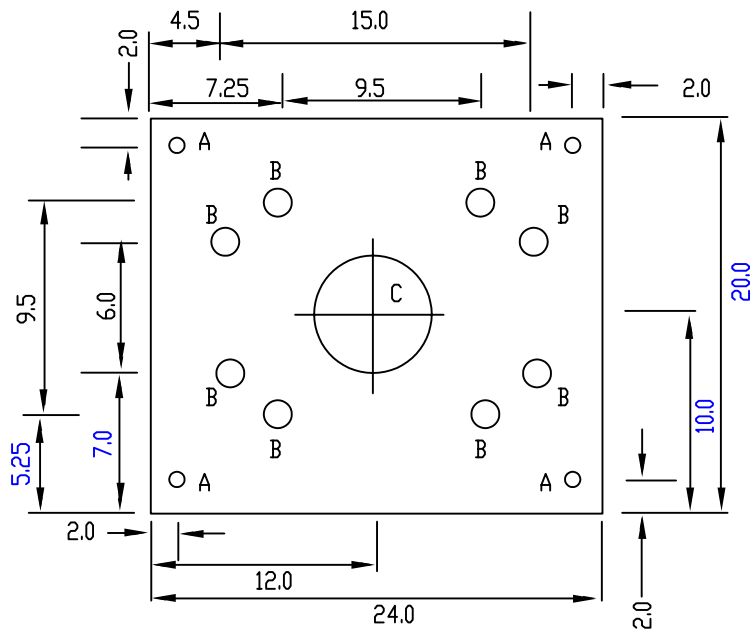


NOTE:

All dimensions shown are in inches.

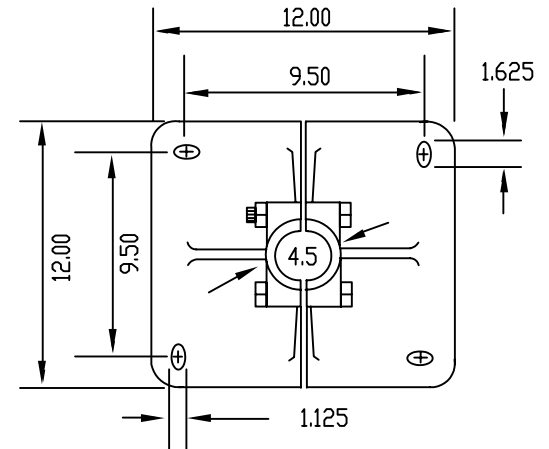
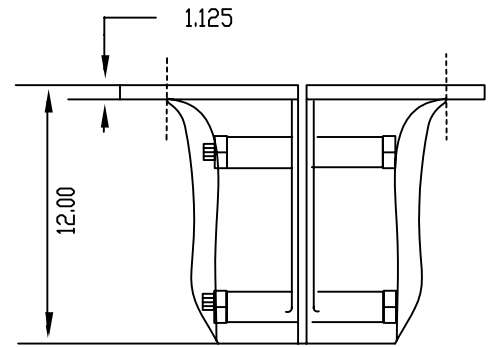
TITLE: CABINET HOUSING DETAILS SHEET 3 OF 4	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-3

CABINET HOUSING 2 PEDESTAL ADAPTOR

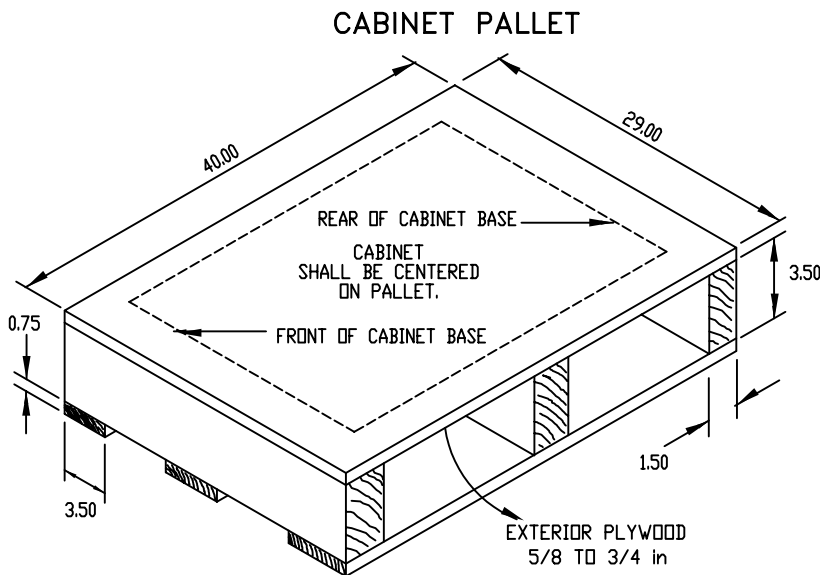


**SLIPFITTER BASE PLATE DETAIL
(0.375 inches ALUMINUM)**

- A = 0.50 in DIA.
- B = 1 in DIA.
- C = 5 in DIA.



**SLIPFITTER (CAST ALUMINUM)
DETAIL**



NOTE: (FOR DETAILS A6-1 to A6-4)

1. Housing 1B used in cabinets 332L & 334L and Housing 2 in cabinet 336L.
2. Adaptors delivered separately shall be delivered centered and bolted on a plywood shipping pallet.
3. Dashed lines on cabinet cage support detail delineates the cabinet side wall.
4. The bottom cabinet cage supports shall be continuously welded along the sides of the cabinet & extended to the inside corner of door openings.
The top cabinet cage supports shall be continuously welded along the sides of the cabinet.
5. Cage support hole slots dimension shall be common for top & bottom.
6. All dimensions shown are in inches.

TITLE:

**CABINET HOUSING DETAILS
SHEET 4 OF 4**

1-21-2010, ERRATA 1

NO SCALE

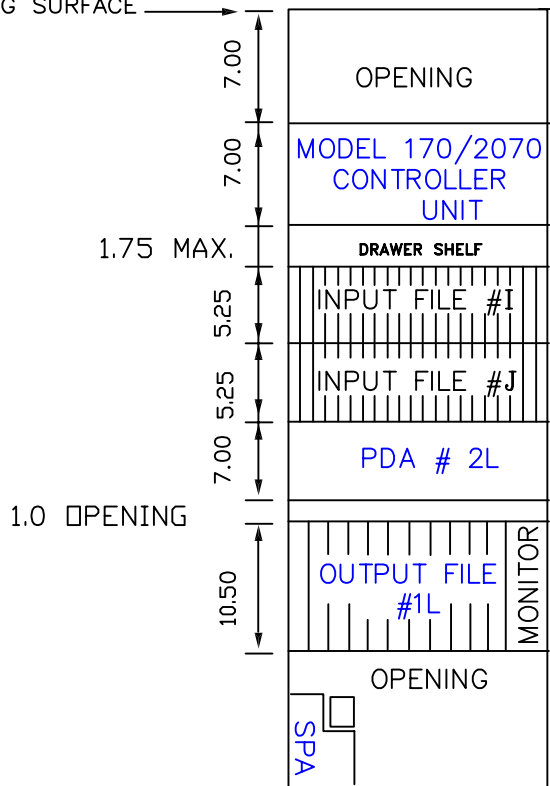
TEES 2009

A6-4

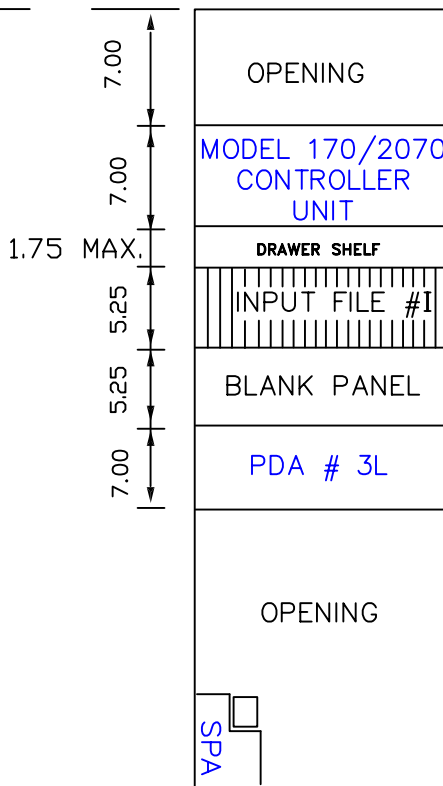
TOP OF EIA
MOUNTING SURFACE

332L CABINET

334L CABINET



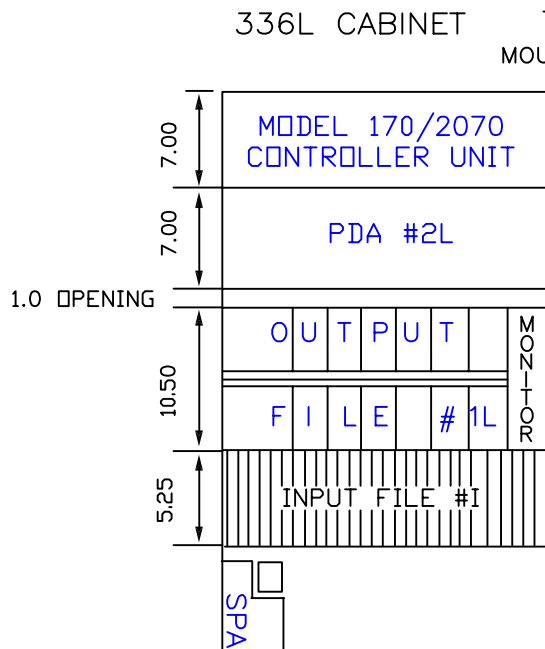
FRONT VIEW



FRONT VIEW

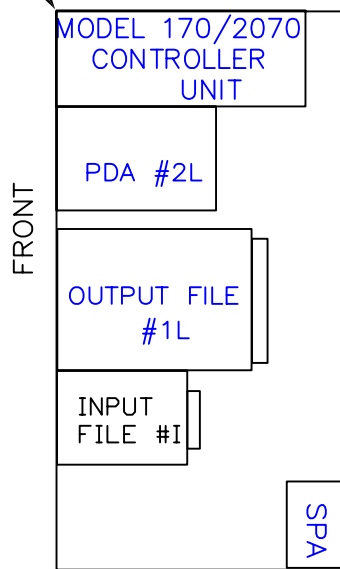
336L CABINET

336L CABINET



FRONT VIEW

TOP OF EIA
MOUNTING SURFACE



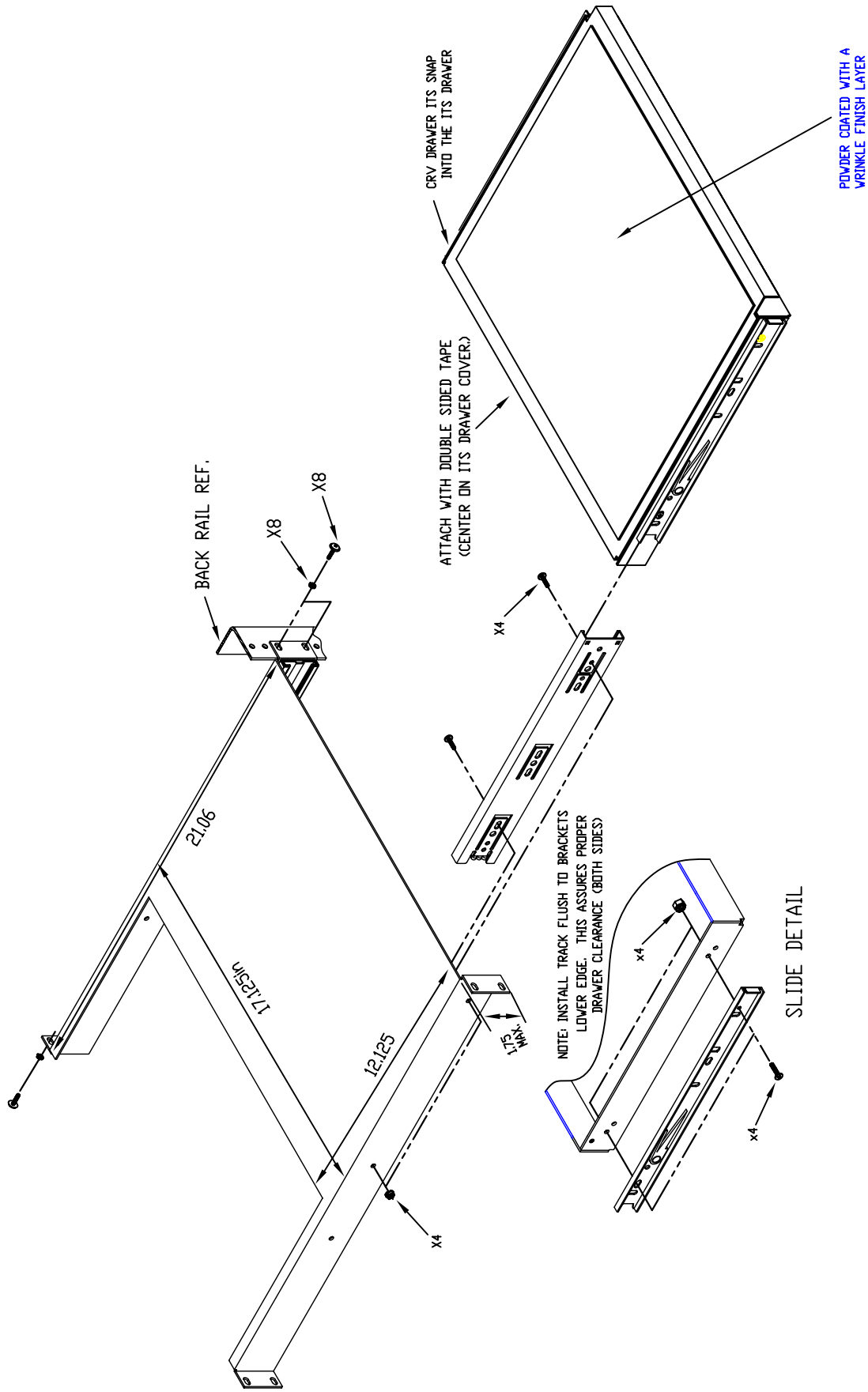
SIDE VIEW

NOTE:

All dimensions shown are in inches.

TITLE: CABINET EQUIPMENT MOUNTING DETAILS	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-5

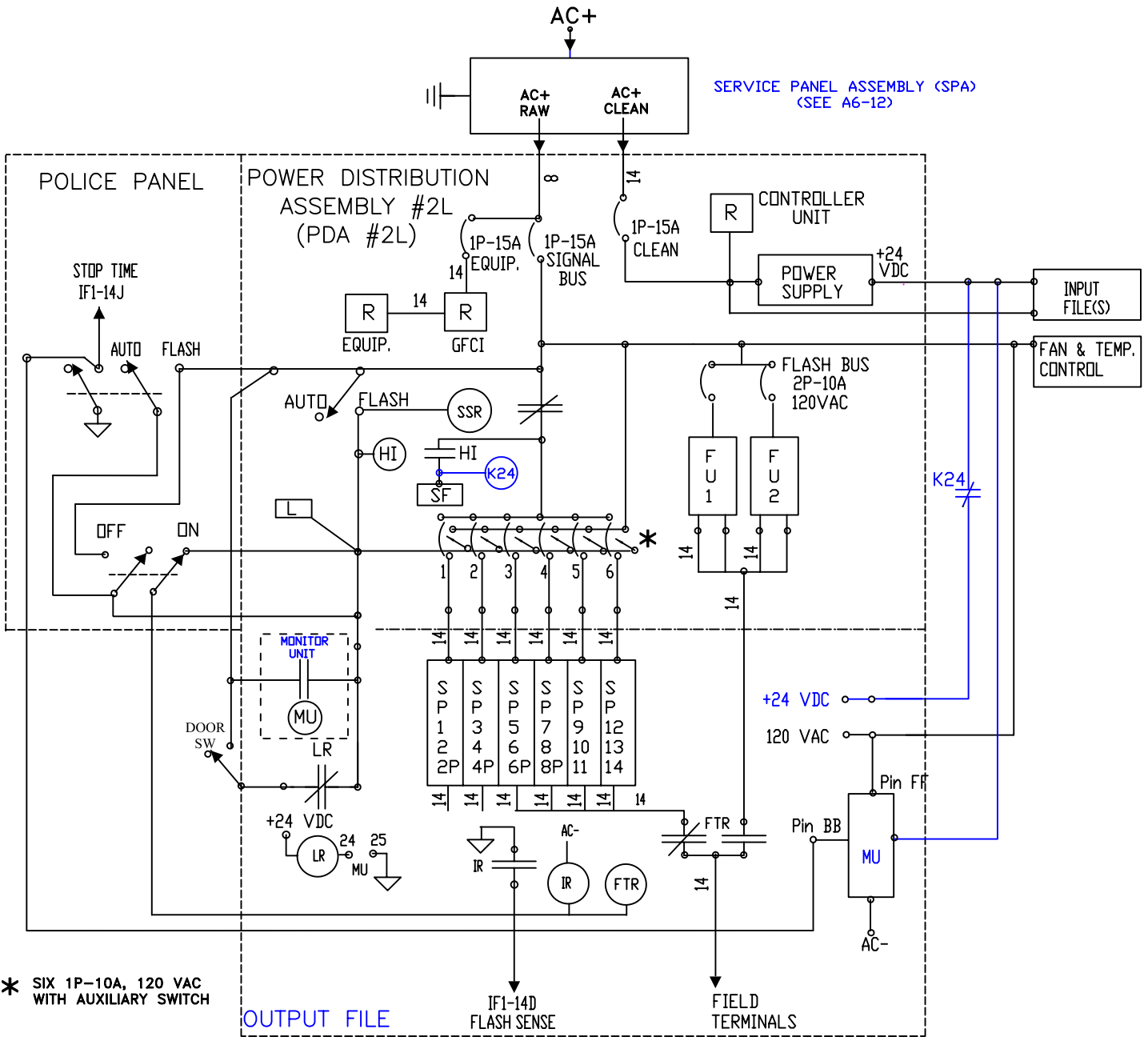
DRAWER SHELF UNIT



NOTE:
All dimensions shown are in inches

TITLE: DRAWER SHELF DETAILS	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-6

332L & 336L CABINET ONE LINE DIAGRAM



* SIX 1P-10A, 120 VAC WITH AUXILIARY SWITCH

SHEET DEFINITIONS

TBS	TERMINAL BLOCK - SERVICE	(*)	RELAY COIL - * RELAY NAME	TR	TRANSFER RELAY
	EQUIPMENT GROUND		FLASHER UNIT ONE	IR	ISOLATION RELAY
8	WIRE SIZE, IF NOT INDICATED SHALL BE #16 AWG OR LARGER		DC GROUND		SWITCH CONTACT
	CIRCUIT BREAKER	WDT	WATCHDOG TIMER	LR	LOGIC RELAY
	DUPLEX RECEPTACLE	FTR	FLASH TRANSFER RELAY	CB-1	SIGNAL CIRCUIT BREAKER 1 (SECONDARY)
WGFI	WITH GROUND FAULT INTERRUPTER		PDA FLASH ON DISPLAY LAMP	IF1-14J	INPUT FILE 1, TERM. BLOCK 14, TERM. DESIGNATION J (CHANNEL 2 INPUT)
	RELAY CONTACT, NORMALLY CLOSED	SPA	SERVICE PANEL ASSEMBLY	T2-6	TERMINAL BLOCK 2, POSITION 6
	RELAY CONTACT, NORMALLY OPEN	MU	MONITOR UNIT	C1-65	C1 CONNECTOR, PIN 65
SSR	SOLID STATE RELAY	SF	SSR Fault Indicator		Health Indicator Relay
					Disconnect 24VDC Relay

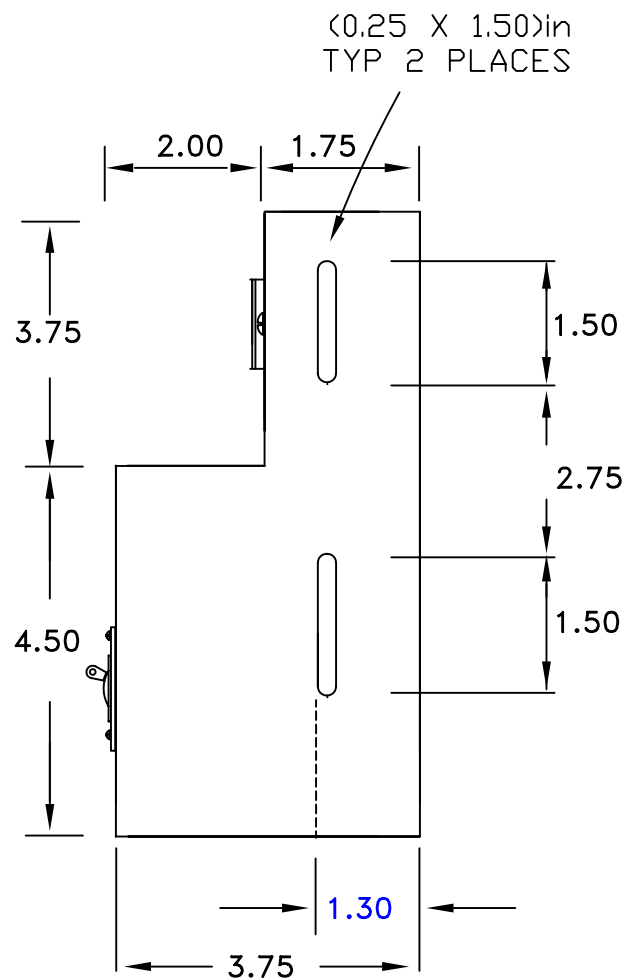
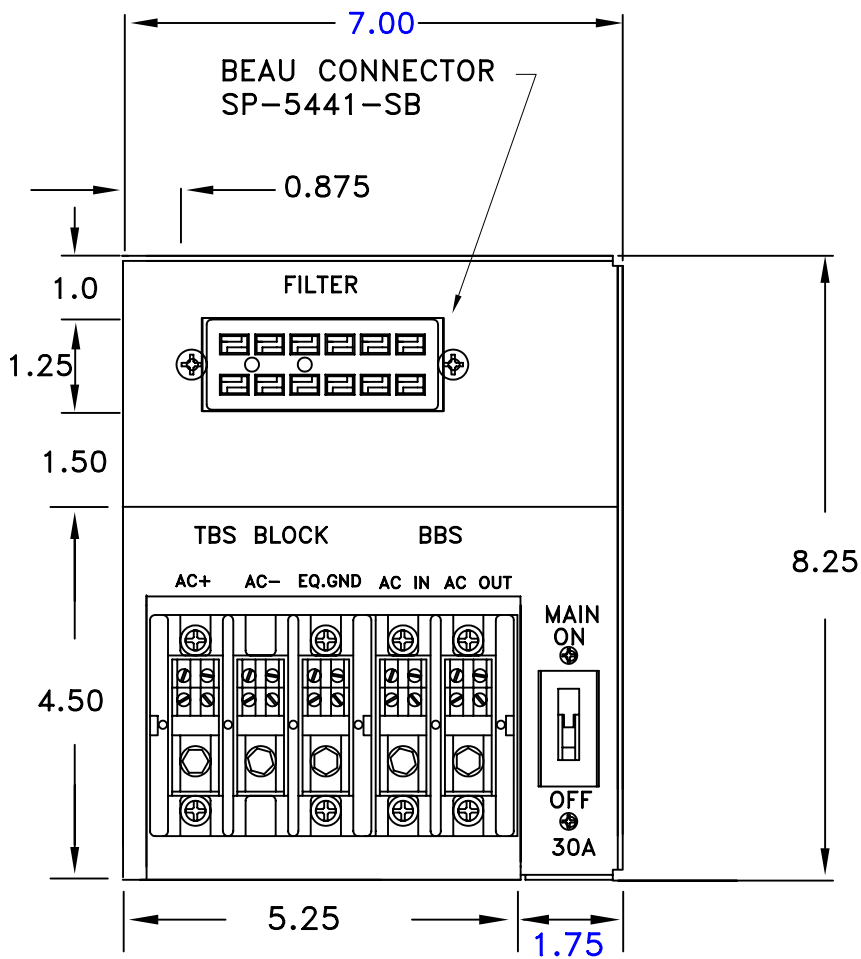
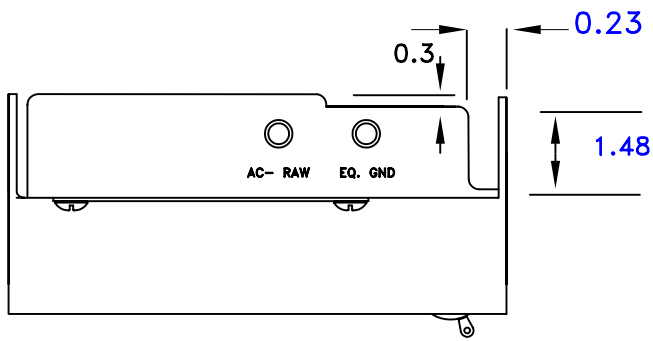
TITLE: **MODEL 332L AND 336L ONE LINE DIAGRAM**

1-21-2010, ERRATA 1

NO SCALE

TEES 2009

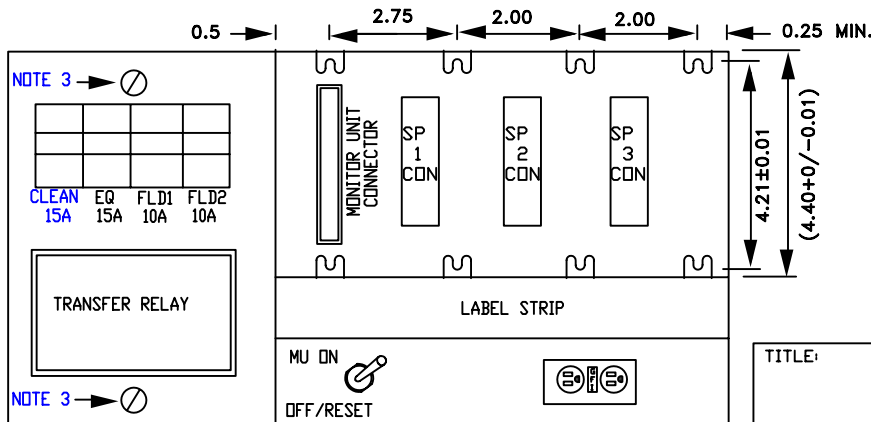
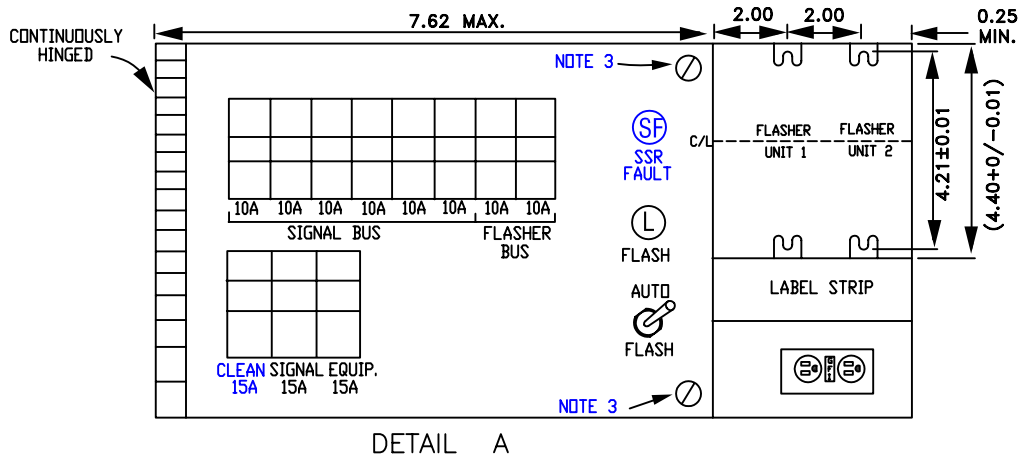
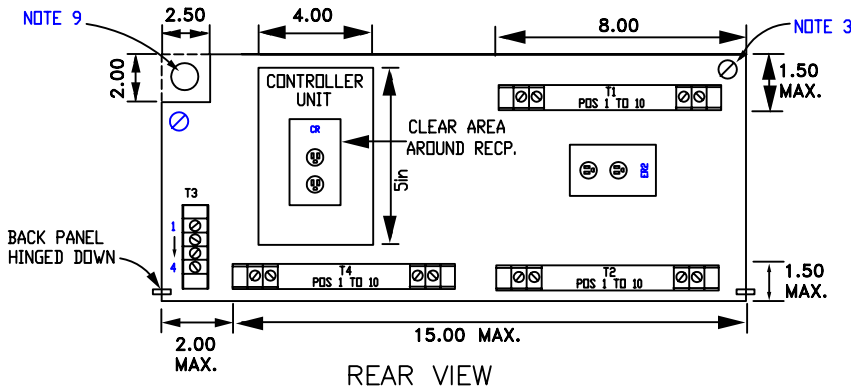
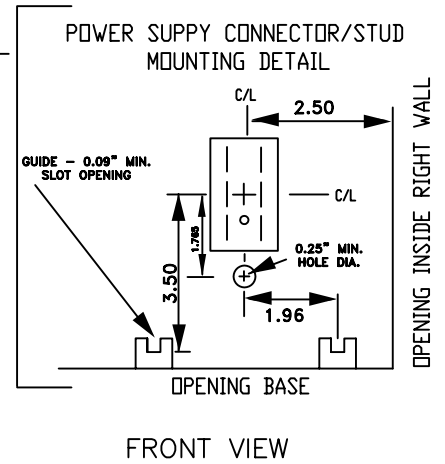
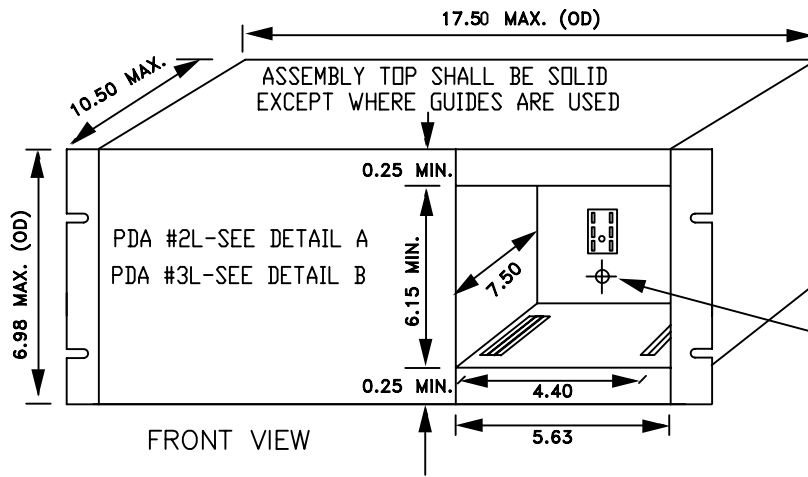
A6-7



NOTE:

All dimensions shown are in inches.

TITLE:	
SERVICE PANEL ASSEMBLY (SPA) DETAILS SHEET 1 OF 3	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-10



DETAIL B

TITLE:	
PDA #2L & #3L DETAILS SHEET 1 OF 3	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-13

NOTE:
All dimensions shown are in inches.

POWER DISTRIBUTION ASSEMBLY TERMINAL BLOCK ASSIGNMENT DETAIL

BLOCK	T1	T2		T3	T4	
PDA's POS	2L A B	2L A B	3L A B	2L & 3L A B	2L A B	3L A B
1.	EG BUS / EG	* / ER AC-	EG BUS / EQ GND	24VDC BUS / PS-7	NA / NA	FL1 / SP 3-3
2.	AC- BUS / AC-	01-5 / FU1-7	AC- BUS / AC-	24VDC (CONTROLLED) / PS-7	NA / NA	FL2 / SP 3-5
3.	CR AC- / AC-CLEAN	01-6 / FU1-8	* / AC+ CLEAN	DC GND BUS / PS 8	NA / NA	FL3 / SP 3-7
4.	* / SCB CKT 5	01-7 / FU2-7	* / AC+ RAW	DC GND BUS / PS-8	NA / NA	FL4 / SP 2-3
5.	* / AC+ RAW	01-8 / FU2-8	* / MU		NA / NA	FL5 / SP 2-5
6.	CR AC+ / AC+ CLEAN	* / FTR DRIVE	* / TR COIL		NA / NA	FL6 / SP 2-7
7.	* / SSR	01-1 / SCB CKT 1	NA / TRC2ND		NA / NA	FL7 / SP 1-3
8.	* / SCB CKT 6	01-2 / SCB CKT 2	NA / TRC2NC		NA / NA	FL8 / SP 1-5
9.	* / FCB1 (SEC)	01-3 / SCB CKT 3	03-5 / FLD2		NA / NA	FL9 / SP 1-7
10.	* / ER AC+	01-4 / SCB CKT 4	SPA AC- / AC-CLEAN		NA / NA	NA / NA

A = EXTERNAL SIDE B = INTERNAL SIDE * = WIRE PER ONE LINE DIAGRAM

NOTES: (FOR DETAILS A6-13 TO A6-15)

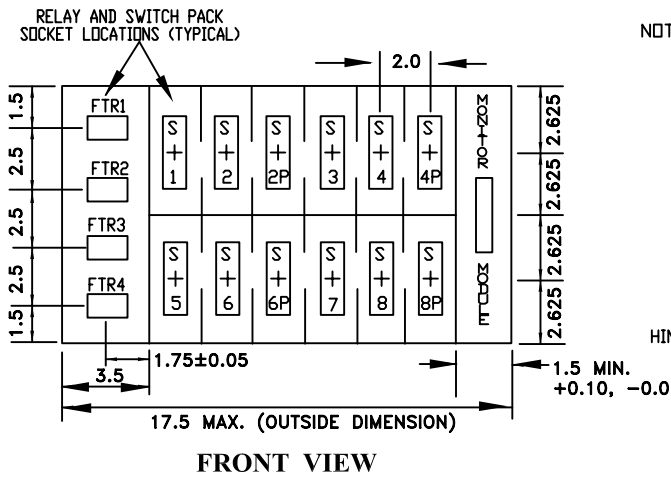
- All dimensions shown are in inches.
- SHEET DEFINITIONS:

CKT = CIRCUIT	EG = EQUIPMENT GROUND
FLD1 = FIELD 1 CIRCUIT BREAKER	FL1 = FIELD LOAD 1
FU1-7 = FLASHER UNIT #1, PIN 7	ER = EQUIPMENT RECEPTACLE
L = LAMP	LD CKT#1 = LOAD CIRCUIT 1
SSR = SOLID STATE RELAY	CR = CONTROL RECEPTACLE
MN = MAIN	MU-22 = MONITOR UNIT - PIN 22
OD = OUTSIDE DIMENSION	PDS = POSITION
PS-7 = POWER SUPPLY PIN 7	SCB = SIGNAL CIRCUIT BREAKER
SP 3-3 = SWITCH PACK 3, PIN 3	TR = TRANSFER RELAY
01-8 = OUTPUT FILE TB 01, POSITION 8	FCB1 = FIELD CIRCUIT BREAKER 1

- Thumb screw device.
- Transfer relay in PDA #2L & 3L shall extend no more than 1.0 inch out from the assembly front face.
- Slack shall be provided in the wiring for the circuit breakers and GFI receptacle to allow for the removal and repair. Excess bends and stress on the wiring shall be minimized.
- See Output File plan sheet for heavy duty relay and switch pack wiring assignments and connector mounting location.
- Wiring shall be routed (with extra length) to minimize movement when front panel door is opened. The wiring going to the front panel shall be routed such that it does not cause undue twisting or bending of the wires.
- No ventilation hole shall be large enough to place a 0.375 inch diameter object through.
- The C5P support connector and support bracket shall be installed (wiring NA) in the PDA #2L. If PDA #2L is used, the input panel C5P connector is not required and harness #2L - C5S connector shall be connected to PDA #2L C5P. If PDA #3L is used, harness #2 - C5S connector shall be connected to input panel C5P and C6P connector, support bracket and wiring shall be installed.

TITLE:	
PDA #2L & #3L DETAILS SHEET 3 OF 3	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-15

OUTPUT FILE #1L DETAIL



OUTPUT FILE #1L TERMINAL ASSIGNMENT DETAIL

01 TERM	FUNCTION
1	PDA CKT1/SWPKS 1,2,2P-1
2	PDA CKT2/SWPKS 3,4,4P-1
3	PDA CKT3/SWPKS 5,6,6P-1
4	PDA CKT4/SWPKS 7,8,8P-1
5	PDA FU1 CKT1/FTR1
6	PDA FU1 CKT2/FTR2
7	PDA FU2 CKT1/FTR3
8	PDA FU2 CKT2/FTR4
9	EQUIP. GROUND
10	AC-
11	AC+ (FROM PDA)
12	SSR (TO PDA)
13	DOOR SW. (FROM POL PAN)
14	FTR COILS (TO)

02 TERM	FUNCTION
1	+24VDC TO LOGIC RELAY COIL (LR)
2	DC GROUND
3	IFI-14J, STOP TIME (FROM M.U)
4	IFI-14D, FLASH SENSE (FROM I.R)
5	EXTERNAL (M.U) RESET
6	N/A
7	+24VDC (CONTROLLED) TO SWITCHPACKS (1-12) POSITION 9

FT1 TERM	FUNCTION	FT2 TERM	FUNCTION	FT3 TERM	FUNCTION
101	SWPK 4-RED	113	SWPK 2P-RED	125	SWPK 1-RED
102	SWPK 4-YEL	114	SWPK 2P-YEL	126	SWPK 1-YEL
103	SWPK 4-GRN	115	SWPK 2P-GRN	127	SWPK 1-GRN
104	SWPK 4P-RED	116	SWPK 3-RED	128	SWPK 2-RED
105	SWPK 4P-YEL	117	SWPK 3-YEL	129	SWPK 2-YEL
106	SWPK 4P-GRN	118	SWPK 3-GRN	130	SWPK 2-GRN
107	SWPK 8-RED	119	SWPK 6P-RED	131	SWPK 5-RED
108	SWPK 8-YEL	120	SWPK 6P-YEL	132	SWPK 5-YEL
109	SWPK 8-GRN	121	SWPK 6P-GRN	133	SWPK 5-GRN
110	SWPK 8P-RED	122	SWPK 7-RED	134	SWPK 6-RED
111	SWPK 8P-YEL	123	SWPK 7-YEL	135	SWPK 6-YEL
112	SWPK 8P-GRN	124	SWPK 7-GRN	136	SWPK 6-GRN

NOTE:

1. Thumb screws device
2. All dimensions shown are in inches

TITLE:

INPUT/OUTPUT FILE DETAILS
SHEET 2 OF 5

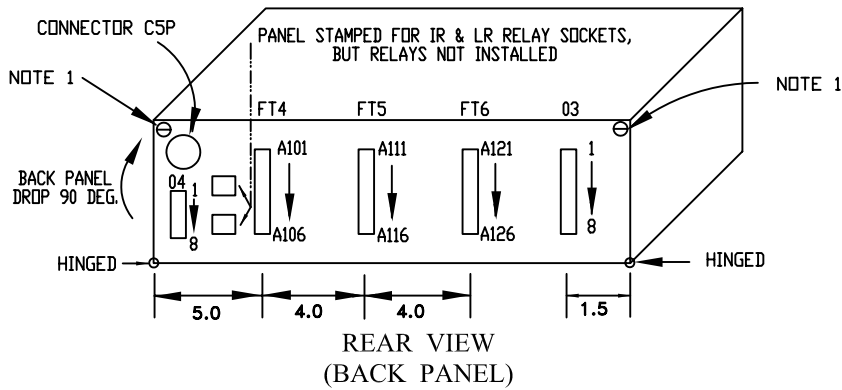
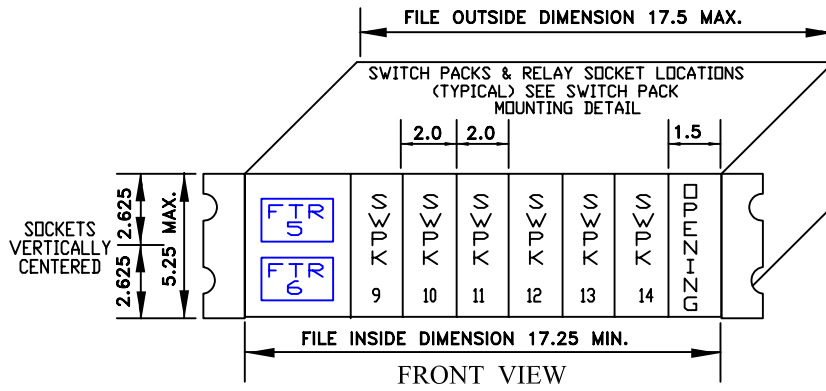
1-21-2010, ERRATA 1

NO SCALE

TEES 2009

A6-17

OUTPUT FILE #2L DETAIL



OUTPUT FILE #2L TERMINAL ASSIGNMENT DETAIL

03 TERM	FUNCTION
1	PDA FU1 CKT1/FTR5
2	PDA FU2 CKT2/FTR6
3	FTR COILS (TO)
4	AC-
5	PDA CKT5/SWPKS 9,10,11-1
6	PDA CKT6/SWPKS 12,13,14-1
7	EQUIP. GROUND
8	AC+ (FROM PDA)

04 TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	STOPTIME
4	FLASH SENSE
5	EXTERNAL RESET
6	WDT INPUT
7	LR COIL (UNIT IN)
8	SSR (PDA)

FT4 TERM	FUNCTION	FT5 TERM	FUNCTION	FT6 TERM	FUNCTION
A101	SWPK 13-RED	A111	SWPK 11-RED	A121	SWPK 9-RED
A102	SWPK 13-YEL	A112	SWPK 11-YEL	A122	SWPK 9-YEL
A103	SWPK 13-GRN	A113	SWPK 11-GRN	A123	SWPK 9-GRN
A104	SWPK 14-RED	A114	SWPK 12-RED	A124	SWPK 10-RED
A105	SWPK 14-YEL	A115	SWPK 12-YEL	A125	SWPK 10-YEL
A106	SWPK 14-GRN	A116	SWPK 12-GRN	A126	SWPK 10-GRN

NOTE:

1. Thumb screws device.
2. All dimensions shown are in inches.

TITLE:

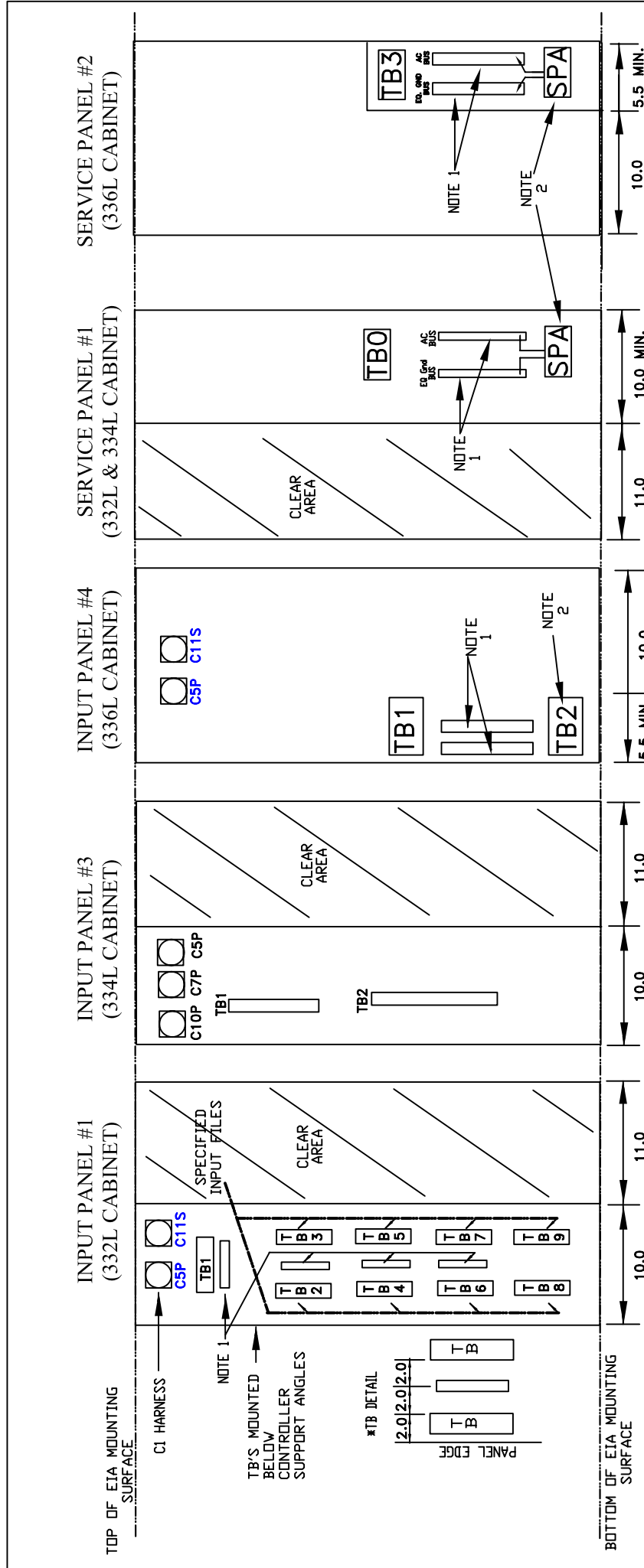
OUTPUT FILE #2L DETAILS

1-21-2010, ERRATA 1

NO SCALE

TEES

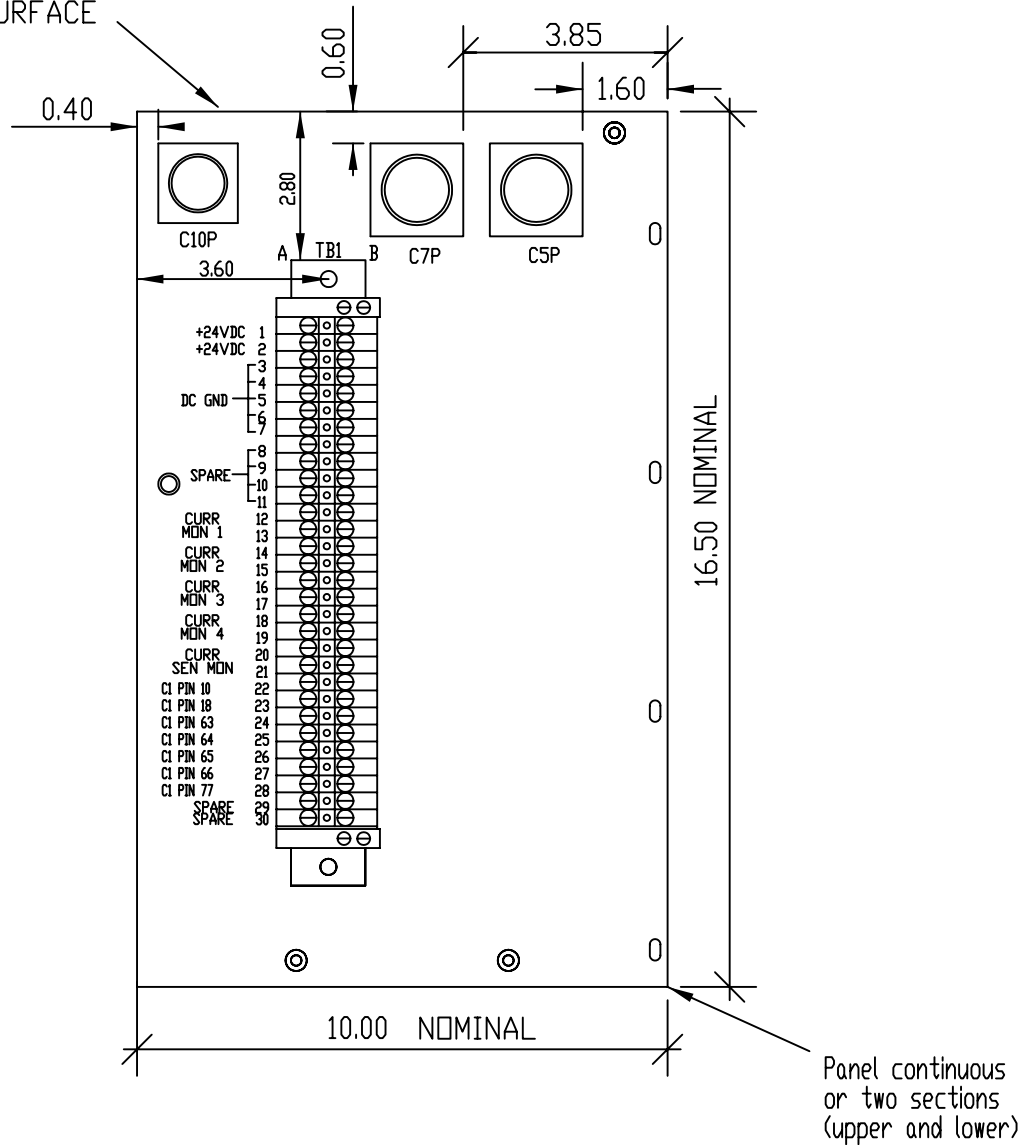
A6-18



NOTES:
 1. 10 terminal (#8 wire) minimum copper bus.
 2. See service panel assembly details A6-10, A6-11 & A6-12.
 3. The terminal block shall have terminal positions necessary to match position assignments. Terminal position screws shall be 8-32 except for TBS, TBO, TB3, which shall be 10-32
 4. All dimensions shown are in inches.

TITLE: SIDE PANEL DETAILS SHEET 1 OF 4	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A6-21

TOP OF EIA
MOUNTING SURFACE



NOTES:

1. Provide and install a 30 position TB1 Terminal Block & three circular connectors, C5P, C7P & C10P (no contacts), TB1 shall be a USK 10 Open Construct Phoenix Contact Terminal Block (or equal) mounted on DIN Railing (supported every 6 inches with position function label tabs and positions commoned and end locks).
2. A 4 foot length "CMS" Harness of 14 #20 (or larger) Conductors shall be furnished and installed in the cabinet. One end of the harness shall be the C10S Connector resting in C10P (mounted on the Input Panel #3) when not in used. The other end shall be stripped (according to manufacturers requirements) and connected to the "B Side" of TB1. The conductor bundle shall have external protection.
3. All dimensions shown are in inches.

TITLE:	
SIDE PANEL DETAILS SHEET 2 OF 4	
1-21-2010, ERRATA 1	No Scale
TEES 2009	A6-22

**INPUT PANEL #1
TERMINAL BLOCK ASSIGNMENT DETAIL**

POS	A	B	POS	A	B	POS	A	B
TB1 - * SEE INPUT PANEL #4 TB1 ASSIGNMENTS			TB4-1	I-4D	TB7-1	J-7D		
			TB4-2	DET 7 I-4E	TB7-2	DET 33 J-7E		
			TB4-3	DET 8 I-4J	TB7-3	DET 34 J-7J		
			TB4-4	I-4K	TB7-4	J-7K		
			TB4-5	DET 9 I-5D	TB7-5	DET 35 J-8D		
			TB4-6	I-5E	TB7-6	J-8E		
			TB4-7	DET 10 I-5J	TB7-7	DET 36 J-8J		
			TB4-8	I-5K	TB7-8	J-8K		
			TB4-9	DET 11 I-6D	TB7-9	DET 37 J-9D		
			TB4-10	I-6E	TB7-10	J-9E		
			TB4-11	I-6J	TB7-11	DET 38 J-9J		
			TB4-12	DET 12 I-6K	TB7-12	J-9K		
TB2-1	DET 1	I-1D	TB5-1	DET 25	J-4D	TB8-1	MANUAL	I-11D
TB2-2		I-1E	TB5-2		J-4E	TB8-2	SPARE	I-11J
TB2-3		I-1J	TB5-3		J-4J	TB8-3	11 COM	I-11K
TB2-4	DET 2	I-1K	TB5-4	DET 26	J-4K	TB8-4	PED Ø2	I-12D
TB2-5		I-2D	TB5-5		J-5D	TB8-5	PED Ø4	I-12J
TB2-6	DET 3	I-2E	TB5-6	DET 29	J-5E	TB8-6	12 COM	I-12K
TB2-7		I-2J	TB5-7		J-5J	TB8-7	PED Ø6	I-13D
TB2-8	DET 4	I-2K	TB5-8	DET 30	J-5K	TB8-8	PED Ø8	I-13J
TB2-9		I-3D	TB5-9		J-6D	TB8-9	13 COM	I-13K
TB2-10	DET 5	I-3E	TB5-10	DET 31	J-6E	TB8-10	FLH SENSE	I-14D
TB2-11		I-3J	TB5-11		J-6J	TB8-11	STOP TIME	I-14J
TB2-12	DET 6	I-3K	TB5-12	DET 32	J-6K	TB8-12	14 COM	I-14K
TB3-1		J-1D	TB6-1	DET 13	I-7D	TB9-1	SPARE 2	J-11D
TB3-2	DET 19	J-1E	TB6-2		I-7E	TB9-2	SPARE 3	J-11J
TB3-3		J-1J	TB6-3	DET 14	I-7J	TB9-3	11 COM	J-11K
TB3-4	DET 20	J-1K	TB6-4		I-7K	TB9-4	EVA	J-12D
TB3-5		J-2D	TB6-5	DET 15	I-8D	TB9-5	EVC	J-12J
TB3-6	DET 21	J-2E	TB6-6		I-8E	TB9-6	12 COM	J-12K
TB3-7		J-2J	TB6-7	DET 16	I-8J	TB9-7	EVB	J-13D
TB3-8	DET 22	J-2K	TB6-8		I-8K	TB9-8	EVD	J-13J
TB3-9		J-3D	TB6-9	DET 17	I-9D	TB9-9	13 COM	J-13K
TB3-10	DET 23	J-3E	TB6-10		I-9E	TB9-10	RR1	J-14D
TB3-11		J-3J	TB6-11	DET 18	I-9J	TB9-11	RR2	J-14J
TB3-12	DET 24	J-3K	TB6-12		I-9K	TB9-12	14 COM	J-14K

**INPUT PANEL #4
TERMINAL BLOCK ASSIGNMENT DETAIL**

TERM	A	B
TB1-1	(+24 VDC) 02-1/T3-1	I15-1, J15-1
TB1-2	M RESET	02-5
TB1-3	02-7/T3-2	C5-24
TB1-4	RESERVED	RESERVED (COMM IN)
TB1-5	RESERVED	RESERVED (COMM IN)
TB1-6	RESERVED	RESERVED (COMM OUT)
TB1-7	RESERVED	RESERVED (COMM OUT)
TB1-8	RESERVED	RESERVED
TB2-1 TO 6	NA	NA

**SERVICE PANELS 1 & 2
TERMINAL BLOCK ASSIGNMENT DETAIL**

TERM	A	B
TBS-1	AC+	TO PDA (without BBS) TO BBS-1 (with BBS)
TBS-2	AC-	AC- BUS
TBS-3	NA	TO EQ.GND BUS
BBS-1	AC+ IN	MBPS AC+ IN
BBS-2	MBPS AC+ OUT	TO PDA
TB0-1 TO 12	NA	NA
TB3-1 TO 6	NA	NA

(See Service Panel Assembly (SPA) details A6-10 & A6-11)

NOTES:

- Sheet definitions:
 11 COM = DC COMMON
 COMM = COMMUNICATION
 DET1 = DETECTOR #1
 EVA = EMERGENCY VEHICLE PREEMPTION A
 IFI-1D = INPUT FILE 1, SLOT 1, CONNECTOR PIN D
 OF = OUTPUT FILE
 M = MONITOR MODULE
 NA = NOT ASSIGNED
 RR1 = RAILROAD PREEMPTION 1
 MBPS = MANUAL BYPASS SWITCH
 BBS = BATTERY BACK-UP SYSTEM
 PDA = POWER DISTRIBUTION ASSEMBLY
- All dimensions shown are in inches.

**INPUT PANEL #3
TERMINAL BLOCK (TB #1) ASSIGNMENT DETAIL**

POS	A	B
TB1-1	+24 VDC	I/O FILES
TB1-2	+24 VDC	CAB. HARNESS #5
TB1-3	DC GND	C1 PINS 1 & 104
TB1-4	DC GND	I/O FILES & CAB. HARNESS #5
TB1-5	DC GND	
TB1-6	DC GND	
TB1-7	DC GND	
TB1-8	SPARE	NA
TB1-9	SPARE	NA
TB1-10	SPARE	NA
TB1-11	SPARE	NA
TB1-12	CURR. MONITOR 1	CAB. HARNESS #5
TB1-13	CURR. MONITOR 1	CAB. HARNESS #5
TB1-14	CURR. MONITOR 2	CAB. HARNESS #5
TB1-15	CURR. MONITOR 2	CAB. HARNESS #5
TB1-16	CURR. MONITOR 3	CAB. HARNESS #5
TB1-17	CURR. MONITOR 3	CAB. HARNESS #5
TB1-18	CURR. MONITOR 4	CAB. HARNESS #5
TB1-19	CURR. MONITOR 4	CAB. HARNESS #5
TB1-20	CURR. SEN. MON.	CAB. HARNESS #5
TB1-21	CURR. SEN. MON.	CAB. HARNESS #5
TB1-22	C1 PIN 10	CIA CONTROL 4
TB1-23	C1 PIN 18	NA
TB1-24	C1 PIN 63	NA
TB1-25	C1 PIN 64	NA
TB1-26	C1 PIN 65	POL. CONTROL SW.
TB1-27	C1 PIN 66	POL. LIGHTS SW.
TB1-28	C1 PIN 77	NA
TB1-29	SPARE	CAB. HARNESS #5
TB1-30	SPARE	CAB. HARNESS #5

**INPUT PANEL #3
TERMINAL BLOCK (TB #2) ASSIGNMENT DETAIL**

POS	A	B	POS	A	B
TB2-1	I-1D		TB2-38	EQ. GND	
TB2-2	I-1E		TB2-39	I-8J	
TB2-3	EQ. GND		TB2-40	I-8K	
TB2-4	I-1J		TB2-41	I-9D	
TB2-5	I-1K		TB2-42	I-9E	
TB2-6	I-2D		TB2-43	EQ. GND	
TB2-7	I-2E		TB2-44	I-9J	
TB2-8	EQ. GND		TB2-45	I-9K	
TB2-9	I-2J		TB2-46	I-10D	
TB2-10	I-2K		TB2-47	I-10E	
TB2-11	I-3D		TB2-48	EQ. GND	
TB2-12	I-3E		TB2-49	I-10J	
TB2-13	EQ. GND		TB2-50	I-10K	
TB2-14	I-3J		TB2-51	I-11D	
TB2-15	I-3K		TB2-52	I-11E	
TB2-16	I-4D		TB2-53	EQ. GND	
TB2-17	I-4E		TB2-54	I-11J	
TB2-18	EQ. GND		TB2-55	I-11K	
TB2-19	I-4J		TB2-56	I-12D	
TB2-20	I-4K		TB2-57	I-12E	
TB2-21	I-5D		TB2-58	EQ. GND	
TB2-22	I-5E		TB2-59	I-12J	
TB2-23	EQ. GND		TB2-60	I-12K	
TB2-24	I-5J		TB2-61	I-13D	
TB2-25	I-5K		TB2-62	I-13E	
TB2-26	I-6D		TB2-63	EQ. GND	
TB2-27	I-6E		TB2-64	I-13J	
TB2-28	EQ. GND		TB2-65	I-13K	
TB2-29	I-6J		TB2-66	I-14D	
TB2-30	I-6K		TB2-67	I-14E	
TB2-31	I-7D		TB2-68	EQ. GND	
TB2-32	I-7E		TB2-69	I-14J	
TB2-33	EQ. GND		TB2-70	I-14K	
TB2-34	I-7J		TB2-71	SPARE	
TB1-35	I-7K		TB1-72	SPARE	
TB1-36	I-8D		TB1-73	EQ. GND	
TB2-37	I-8E				

TITLE:

**SIDE PANEL DETAILS
SHEET 4 OF 4**

1-21-2010, ERRATA 1

NO SCALE

TEES 2009

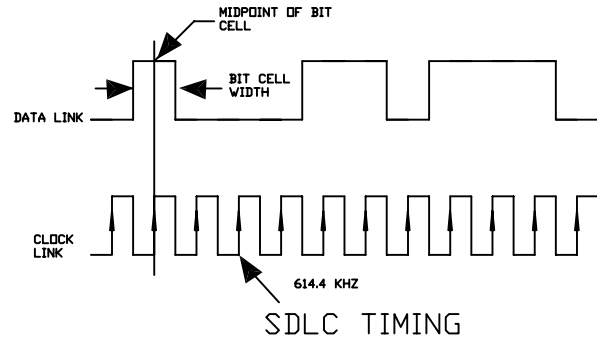
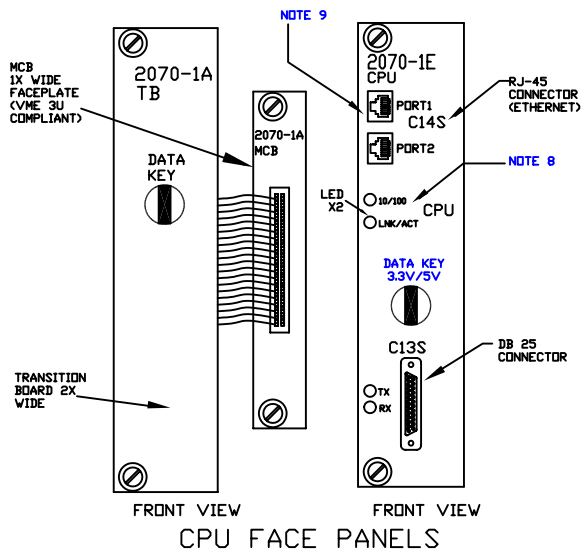
A6-24

APPENDIX A9
CHAPTER 9 DETAILS

Model 2070 - Chassis Front View	A9-1
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SERIAL PORT REQUIREMENTS			
LOGICAL PORT		RATE KBITS	PROTOCOL
SP1		1.2, NOTE 1	ASYNC
SP1S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP2		1.2, NOTE 1	ASYNC
SP2S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP3		1.2, NOTE 1	ASYNC
SP3S		614.4, NOTE 3	SYNC, HDLC, SDLC
SP4		9.6, NOTE 1	ASYNC
SP5		1.2, NOTE 1	ASYNC
SP5S		614.4	SYNC, HDLC, SDLC
SP6		38.4, NOTE 1	ASYNC
SP8**	NOTE 4	9.6, NOTE 1	ASYNC
SP8S**	NOTE 4	153.6	SYNC, HDLC, SDLC

SDLC FRAME LAYOUT					
OPENNING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8TXD+	14	SP8TXD-
2	SP8RXD+	15	SP8RXD-
3	SP8TXC+	16	SP8TXC-
4	SP8RXC+	17	SP8RXC-
5	SP8RTS+	18	SP8RTS-
6	SP8CTS+	19	SP8CTS-
7	SP8DCD+	20	SP8DCD-
8	NA	21	NA
9	LINESYNC+	22	LINESYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

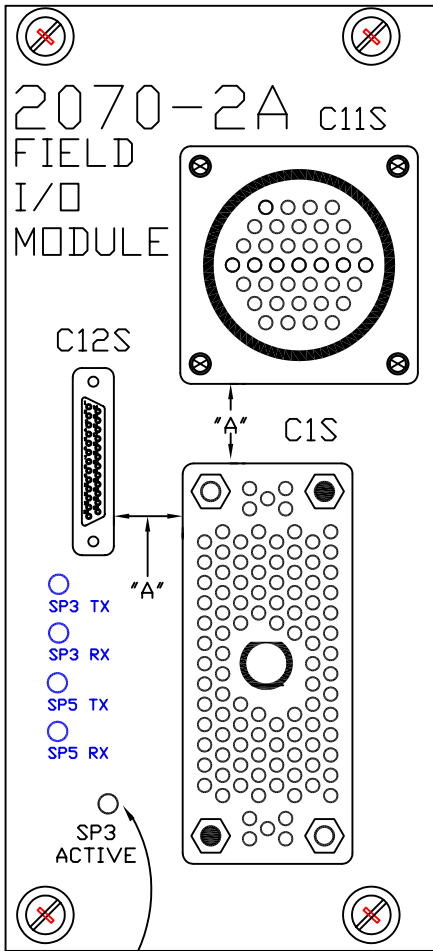
C14S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

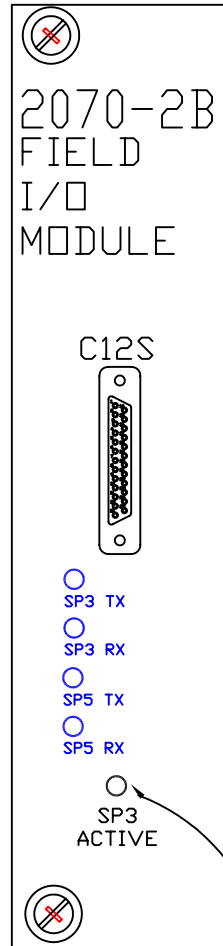
- Additional rates 1.2, 2.4, 4.8, 9.6, 19.2, 38.4.
- Additional descriptors for other rates:
SPxSa = 19.2, SPxSb = 38.4, SPxSc = 57.6
SPxSd = 76.8, SPxSg = 64.0, SPxSe = 153.6.
- Additional descriptors for other rates:
SPxSe = 153.6, SPxSf = 614.4.
- On 2070-1A, SP1 is assigned to 68360 SCC1. On 2070-1E, SP1 and SP8 are assigned to the dual SCC, and ETHERNET is assigned to 68EN360 SCC1.
- A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.
- BIAS +5VDC (50mA maximum) refers to voltage required for a Line Terminator device and is derived from the ISO +12VDC Power Supply.
- EG (Equipment Ground) pin is electrically connected to the faceplate.
- LED indicators between switch & CPU
- All RJ-45 connectors shall contain LED indicators 10/100 & LNK/ACT

** 2070-1E only.

TITLE:	MODEL 2070-1E CPU MODULES AND SERIAL PORT/SDLC PROTOCOL
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A9-7



FRONT VIEW



FRONT VIEW

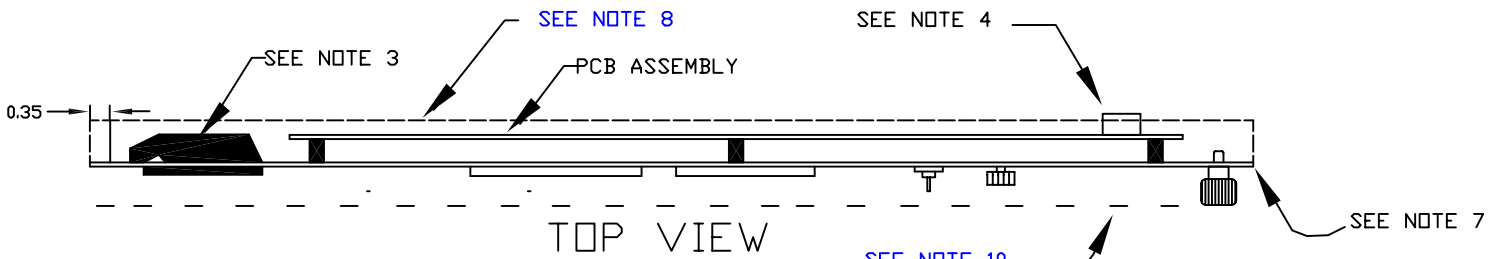
C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP5TXD+	14	SP5TXD-
2	SP5RXD+	15	SP5RXD-
3	SP5TXC+	16	SP5TXC-
4	SP5RXC+	17	SP5RXC-
5	SP3TXD+	18	SP3TXD-
6	SP3RXD+	19	SP3RXD-
7	SP3TXC+	20	SP3TXC-
8	SP3RXC+	21	SP3RXC-
9	LINE SYNC+	22	LINE SYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

FIELD I/O FACE PANELS

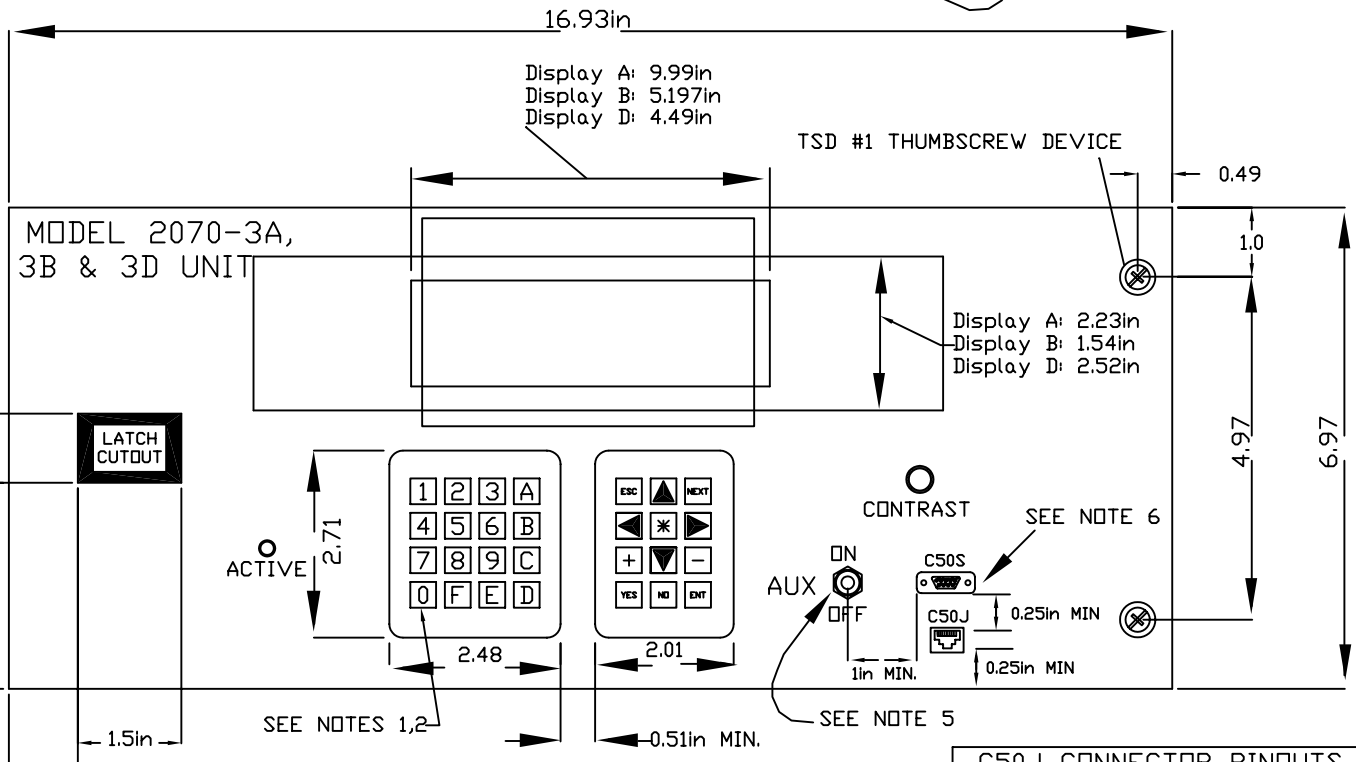
NOTES: (FOR THIS DETAIL)

- 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide. (SEE SYSTEM PCB MODULE, GENERAL DETAILS.)
- Dark Circles in the C1S Connector denote guide pin locations and opencircles denote guide socket locations.
- Dimension "A" shall be a minimum of 0.5in.
- C1S - M104 Type. C11S - 37-Pin Circular Plastic Type. C12S - 25-Pin DB Socket Type
- C12S pin 12 (BIAS +5VDC) at 50mA maximum is derived from the ISO +12 VDC Power Supply. BIAS +5VDC refers to voltage required for a Line Terminator device.
- EG (Equipment Ground) pin is electrically connected to the faceplate.
- LED indicators Tx & Rx for SP3 (field site) and SP5 shall be provided.
- C1 connector shall be bolted to the front plate.

TITLE:		MODEL 2070-2 FIELD I/O MODULES	
1-21-2010, ERRATA 1		NO SCALE	
TEES 2009		A9-8	



TOP VIEW



FRONT VIEW

NOTES: (FOR THIS DETAIL)

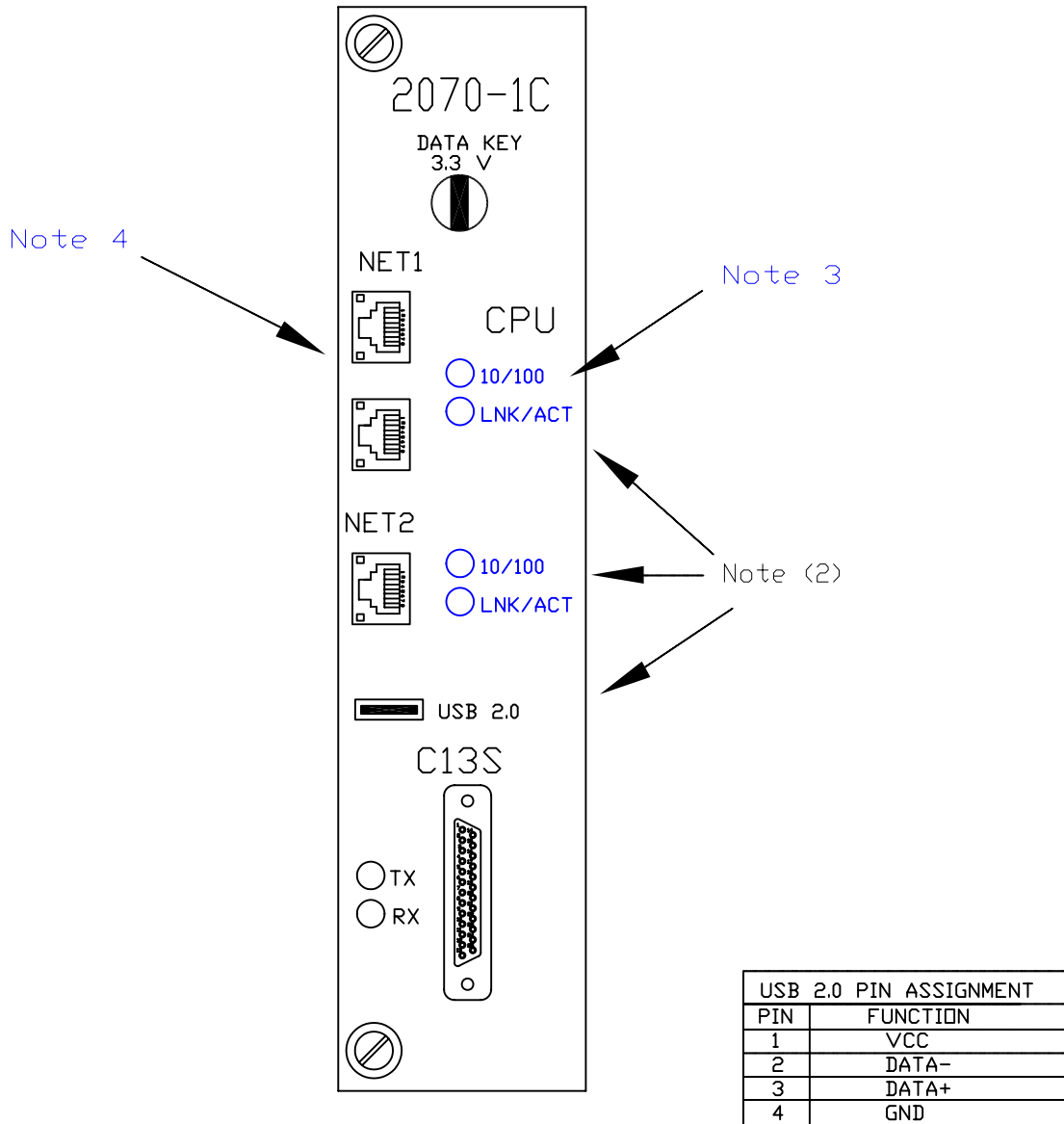
1. Key size shall be (0.3x0.3)in.
2. Key center to center spacing shall be 0.5in.
3. Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
4. The 40 contact connector shall be similar to AMP 102160-9 or equal & compatible to the FP harness in type and pin assignments. Center of the FP harness connector shall be vertically positioned (3.54+/-0.197)in as measured from the top of the FPA. The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
5. Two position LOGIC switch mounted vertically.
6. "C50S" connector shall be a DE-9 socket contact connector. "C50J" shall be a RJ-45 8-position jack. "C60P" connector shall be a DE-9 plug contact connector.
7. Front panel sheet metal thickness shall be (0.06±0.005) in.
8. The FPA shall be provided with a continuous top and bottom 0.63in (inside dimension) lip bent 90 degrees to the front plate and shall extend the full length of the FPA.
9. C60P B Box Power is +5VDC, 350mA max. All signals on C60 P are referenced to isolated interface ground DCG#3.
10. Components shall not protrude beyond the height of the thumbscrews when tightened.
11. See 9.4.1 for components required.
12. All dimensions shown are in inches.

C50S CONNECTOR PINOUTS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4RXD
3	SP4TXD
4	NA
5	DCG #1
6	NA
7	NA
8	NA
9	NA

C50J CONNECTOR PINOUTS	
PIN	FUNCTION
1	NA
2	SP4RXD
3	C50 ENABLE
4	NA
5	SP4TXD
6	DCG #1
7	NA
8	NA

C60P CONNECTOR PINOUTS	
PIN	FUNCTION
1	B Box Power, Note 9
2	SP6RXD
3	SP6TXD
4	NA
5	DCG #3
6	NA
7	CPURESET
8	NA
9	CPU LED

TITLE: MODEL 2070-3A, 3B & 3D FRONT PANEL ASSEMBLY	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A9-10



USB 2.0 PIN ASSIGNMENT	
PIN	FUNCTION
1	VCC
2	DATA-
3	DATA+
4	GND

NET1 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NET2 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

NOTES: (FOR THIS DETAIL)

- BIAS +5VDC refers to voltage required for a Line Terminator device.
- NET1, NET2, USB & C13S should be placed within the area as shown.
- LED indicators between switch & CPU.
- All RJ-45 connectors shall contain LED indicators 10/100 & LNK/ACT.

TITLE:	
MODEL 2070-1C CPU	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A9-15

SERIAL PORT DESCRIPTORS DEFAULTS			
SP1, SP2, SP3 and SP5	SP4	SP 6	SP 8
noupc	noupc	noupc	noupc
bsb	bsb	bsb	bsb
bsl	bsl	bsl	bsl
noecho	echo	echo	noecho
lf	lf	lf	lf
null=0	null=0	null=0	null=0
nopause	nopause	nopause	nopause
pag=24	pag=24	pag=24	pag=24
bsp=08	bsp=08	bsp=08	bsp=08
del=18	del=18	del=18	del=18
eor=0D	eor=0D	eor=0D	eor=0D
eof= 1B	eof= 1B	eof= 1B	eof= 1B
reprint=04	reprint=04	reprint=04	reprint=04
dup=01	dup=01	dup=01	dup=01
psc=17	psc=17	psc=17	psc=17
abort=03	abort=03	abort=03	abort=03
quit=05	quit=05	quit=05	quit=05
bse=08	bse=08	bse=08	bse=08
bell=07	bell=07	bell=07	bell=07
type=00	type=00	type=00	type=00
baud=1200	baud=9600	baud=38400	baud=9600
xon=11	xon=00	xon=11	xon=11
xoff=13	xoff=00	xoff=13	xoff=13
tabc=09	tabc=09	tabc=09	tabc=09
tabs=4	tabs=4	tabs=04	tabs=04

NOTES: (FOR THIS DETAIL)

1. All serial port descriptors shall be set with 8 Bit Word,
1 Stop & no Parity.
2. Model 2070-1C sp4 shall be set to 38.4 Kbps.
3. sp3s & sp5s shall be set to 614.4 Kbps.

TITLE: SERIAL PORT DESCRIPTORS DEFAULTS	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A9-16

**APPENDIX A10
CHAPTER DETAILS**

Model 2070-6 ASYNC / Modem Serial Communication Module	A10-1
Model 2070-7 ASYNC / SYNC Serial Communication Module	A10-2
Model 2070-6D Fiber Optics Communication Module	A10-3
Model 2070-Fx Fiber Optics Network Communication Module	A10-4
Model 2070-6W Wireless Modem Communication Module	A10-5
Model 2070-9 FSK / Dial Up Modem Communication Module	A10-6
Model 2070 - 6E Serial 2 Network Communication Module	A10-7
Model 2070 - 9D Dial-Up Modem Communication Module	A10-8
Model 2070 -7G Universal Time Base Module	A10-9

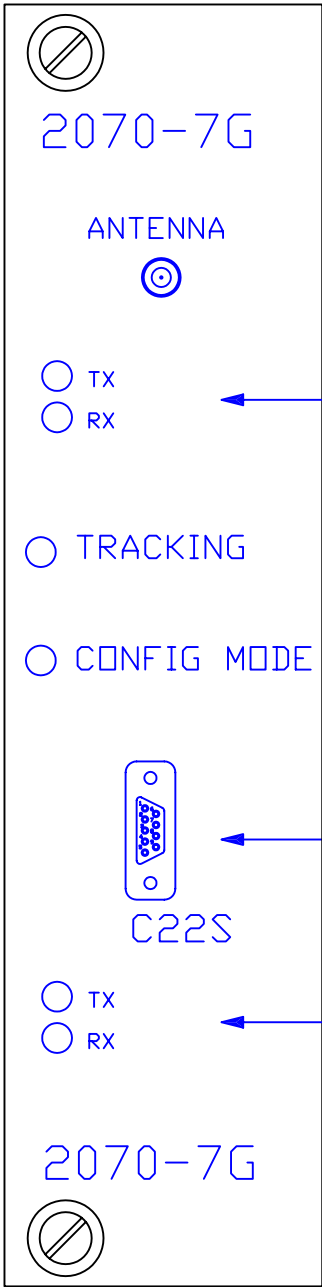
GENERAL NOTES

The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on the module.

Line drivers/receivers shall be socket or surface mounted.

Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.

The Comm modules shall be "Hot" swappable without damage to circuitry or operations.



DB9 - PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	GND
6	NA
7	RTS
8	CTS
9	NA

TITLE:	
MODEL 2070-7G UNIVERSAL TIME BASE MODULE	
1-21-2010, ERRATA 1	NO SCALE
TEES 2009	A10-9



TRANSPORTATION ELECTRICAL EQUIPMENT SPECIFICATIONS

TEES



March 12, 2009

**STATE OF CALIFORNIA
DEPARTMENT OF TRANSPORTATION**



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**CHAPTER 1
ELECTRICAL EQUIPMENT
GENERAL SPECIFICATIONS**

CHAPTER 1-SECTION 1

ELECTRICAL TERMONOLOGY

1.1.1 Glossary of Terms

A	Amperes
AASHTO	American Association of State Highway and Transportation Officials
AC	Alternating Current
AC+	120 Volts AC, 60 hertz ungrounded power source
AC-	120 Volts AC, 60 hertz grounded return to the power source
AGENCY	Purchasing Government Agency
ANSI	American National Standard Institute
API	Application Program Interface
ASCII	American Standard Code for Information Interchange
Assembly	A complete machine, structure or unit of a machine that was manufactured by fitting together parts and/or modules
ASTM	American Society for Testing and Materials
ATC	Advanced Transportation Controller
AWG	American Wire Gage
bps	bits per second
Big Endian	The sequencing of byte order in memory such that the most significant byte is stored at the lowest memory address, with the next byte in significance stored at the next memory location, and so on.
C	Celsius
C Language	The ANSI C Programming Language
Cabinet	An outdoor enclosure generally housing the controller unit and associated equipment
Certificate of Compliance	A certificate signed by the manufacturer of the material or the manufacturer of assembled materials stating that the materials involved comply in all respects with the requirements of the specifications
Channel	An information path from a discrete input to a discrete output
CIA	CMS Controller Isolation Assembly
CIP	CMS Interface Panel
CMOS	Complementary Metal Oxide Semiconductor
CMS	Changeable Message Sign
CMS SYSTEM	Includes Controller Unit, Model 334C Cabinet, Interconnect Harnesses, CMS and other associated equipment required to operate the system.
Component	Any electrical or electronic device

Contractor	The person or persons, manufacturer, firm, partnership, corporation, vendor or combination thereof, who have entered into a contract with the AGENCY, as party(s) of the second part or legal representative
Controller Unit	That portion of the controller assembly devoted to the operational control of the logic decisions programmed into the assembly
CPDA	CMS Pixel Driver Assembly
CPDM	CMS Pixel Driver Module
CPMM	CMS Pixel Matrix Module
CPU	Central Processing Unit
CR	ACIA Control Register
CRC	Cyclic Redundancy Check
CTS	Clear To Send
DAT Program	The AGENCYs Diagnostic and Acceptance Test Program
Daughter Board	(from TechEncyclopedia) A Printed Circuit Board that plugs into another Printed Circuit Board to augment its capabilities
DB	Decibel
DBa	Decibels above reference noise, adjusted
DC	Direct Current
DCE	Data Communications Equipment
DIN	Deutsche Industrie Norm
DMA	Direct Memory Access
DTA	Down Time Accumulator
DTE	Data Terminal Equipment
DPST	Double Pole Single Throw
EG	Equipment Ground
EIA	Electronic Industries Association
EMI	Electro Magnetic Interference
Engineer	The AGENCY director, acting either directly or through properly authorized agents, such agents acting within the scope of the particular duties delegated to them
EPROM	Ultraviolet Erasable, Programmable, Read Only Memory Device
EEPROM	Electrically Erasable, Programmable, Read Only Memory Device
Equal	Connectors: comply to physical dimensions, contact material, plating and method of connection. Devices: conforming to function, pin out, electrical and operating parameter requirements, access times and interface parameters of the specified device
ETL	Electrical Testing Laboratories, Inc.
FCU	Field I/O Controller Unit.
Firmware	A computer program or software stored permanently in PROM, EPROM, ROM or semi-permanently in EEPROM

FLASH	An IC Memory Device with nonvolatile, electrically erasable, programmable, 100K read/write minimum cycles and fast access time features
FPA	Front Panel Assembly
HDLC	High-Level Data Link Control
HEX	Hexadecimal
Hz	Hertz
IC	Integrated Circuit
I.D.	Identification
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
IPI	Initial Protocol Identifier
ISP	Internet Support Package
ISO	Short for “Isolated” and signifies that two or more power supplies each have different reference grounds.
ISO/IEC	International Standards Organization
ITE	Institute of Transportation Engineers
ITS	Intelligent Transportation Systems
Jumper	A means of connecting/disconnecting two or more conductive points by soldering/desoldering a conductive wire.
KB	Kilobytes
Laboratory	The established laboratory of the AGENCY or other laboratories authorized by the AGENCY to test materials involved in the contract
LED	Light Emitting Diode
LOGIC	Negative Logic Convention (Ground True) State
LSB	Least Significant Byte
Lsb	Least Significant Bit
MB	Megabyte
MSB	Most Significant Byte
Msb	Most Significant Bit
m	Milli
MPU	Microprocessor Unit
MIL	Military Specifications
MODEM	Modulation/Demodulation Unit
Module	A functional unit that plugs into an assembly
Motherboard	A printed circuit connector interface board with no active or passive components
MOS	Metal-Oxide Semiconductor
MOV	Metal-Oxide Varistor
MS	Military Standards
M/170	Program Module/Model 170 Controller Unit Connector

M/170E	Model 170E Auxiliary Board Connector
N.C.	Normally closed contact
N.O.	Normally open contact
NA	Presently Not Assigned. Cannot be used by the manufacturer for other purposes
NEMA	National Electrical Manufacturer's Association
NETA	National Electrical Testing Association, Inc.
n	nano
NLSB	Next Least Significant Byte
Nlsb	Next Least Significant Bit
NMSB	Next Most Significant Byte
Nmsb	Next Most Significant Bit
NTCIP	National Transportation Communication for ITS Protocol
PCB	Printed Circuit Board
PDA	Power Distribution Assembly
PLA/PAL	Programmable Array Logic Device

PMPP	Point-to-Multi-Point Protocol
ppm	Parts per million
PPP	Point-to-Point Protocol
PWM	Pulse Width Modulation
RAM	Random Access Memory
RDR	ACIA Receiver Data Register
RF	Radio Frequency
RMS	Root-Mean-Square
ROM	Read Only Memory Device
RTC	Model 170E Controller Unit Real Time Clock. This circuitry provides a 170E CPU IRQ Interrupt pulse clocked off of the local power company's line frequency every 16.67 ms.
RTCA	Real Time Clock Adjuster Circuitry
RTS	Request to Send
RXD	Receive Data
R/W	Model 170E Controller Unit Read/Write Control Line
SCI	Serial Communications Interface
SDLC	Synchronous Data Link Control
S	Logic State
TEES	

S	second
SS	Second Source. Produced by more than one manufacturer
Shunt	A means of connecting/disconnecting two conductive points on a solderless PCB post heater.
SR	ACIA Status Register
SRAM	Static Random Access Memory Device
SW	Switch
TB	Terminal Block
TDR	ACIA Transmit Data Register
TIA	Telecommunications Industry Association
TOD	Time Of Day Clock
Triac	Silicon-Controlled Rectifier which controls power bilaterally in an AC switching circuit
TTL	Transistor-Transistor Logic
TSD	Thumb Screw Device. A retractable screw fastener with projecting stainless steel screw, spring and natural aluminum knob finish. (TSD No. 2 shall be flat black.) TSD No.1 - 8-32 SOUTHCO #47-62-301-20 or equal. TSD No.2 - 8-32 SOUTHCO #47-62-301-60 or equal. TSD No.3 - M3 SOUTHCO #47-81-181-10 or equal.
TXC	Transmit Clock
TXCI	Transmit Clock Input
TXCO	Transmit Clock Output
TXD	Transmit Data
μ	Micro
UL	Underwriter's Laboratories, Inc.
VAC	Voltage Alternating Current
VDC	Voltage Direct Current
VMA	Valid Memory Address
VME	Versa Module Eurocard, VMEbus Standard IEEE P1014/D1.2
VMS	Variable Message Sign
X	Number Value
XX	Manufacturer's Option
WDT	Watchdog Timer: A monitoring circuit, external to the device watched, which senses an Output Line from the device and react

CHAPTER 1-SECTION 2 GENERAL

1.2.1 Chapter Conflict

In case of Chapter Conflict, the individual Chapter shall govern over Chapter 1.

1.2.2 Furnished Equipment

All furnished Equipment shall be new and unused. Vacuum or gaseous tubes and electro-mechanical devices (unless specifically called out) shall not be used.

1.2.3 Interchangeability

The following assemblies and their respective associated devices shall electrically and mechanically intermate and be compatible with each other:

<u>ASSEMBLIES</u>	<u>ASSOCIATED DEVICES</u>
Output File #1 & #2	Model 200 Switch Pack Model 210 Monitor Unit Model 430 Heavy Duty Relay
Input File	Models 222 & 224 Detectors Models 242 & 252 Isolators
PDA #2L	Model 204 Flasher Unit Model 206 Power Supply Module
PDA #3L	Model 200 Switch Pack Model 206 Power Supply Module Model 208 Monitor Unit Model 430 Heavy Duty Relay
PDA #4L	Model 206 Power Supply CMS Isolation Module
Model 170E Controller Unit	Cabinet Models 332, 334 & 336 Model 400 MODEM Model 412C Program Module
Model 2070 Controller Unit	Cabinet Models 332, 334, 336 & ITS Model 2070-1 CPU Module Model 2070-2 Field I/O Module Model 2070-3 Front Panel Assembly Model 2070-4 Power Supply Model 2070-5 VME Cage Assembly Model 2070-6 Serial Comm Module Model 2070-7 Serial Comm Module

Model 2070-N1 Controller Unit	Model 2070 Controller Unit Model 2070-8 NEMA Module Model 2070-2B Field I/O Module Model 2070-4N Field I/O Module
Model 2070-N2 Controller Unit	Model 2070 Controller Unit Model 2070-2N Field I/O Module Model 2070-4N Power Supply Module
Pixel Driver Assembly	Pixel Driver Module

1.2.4 Documentation

1.2.4.1 Manual

Two copies of Manual Documentation shall be supplied for each item purchased up to 200 manuals per order. The manual shall be bound in durable covers made of either 65-pound stock paper or clear plastic. The manual shall be printed on 8.5 in by 11 in paper, with the exception that schematics, layouts, parts lists and plan details may be on 11 in by 17 in sheets, with each sheet neatly folded to 8.5 in by 11 in size. Manual text font shall be ARIAL BOLD, size 12. Text characters shall be no more than 10 characters per 1 in and 7 lines per 1 in, with the exception of schematic text, which shall be no more than 18 characters per 1 in and 11 lines per 1 in.

1.2.4.2 Parts Listed

The State of California title, device name, date, serial numbers and revision numbers of equipment covered by the manuals shall be printed on the front cover of the manuals. The manual shall be separated into two volumes; volume one shall be labeled as Operating Manual and volume two shall be label as Electrical/Mechanical Drawings.

Volume one of the Manual shall include a table of contents and items 2 through 9 and Volume two shall include a table of contents and items 10 through 12 in order as listed:

Item #	Section #	Description
1	N/A	Table of Contents
2	1	Glossary
3	2	General Description
4	3	General Characteristics
5	4	Installation
6	5	Adjustments
7	6	Theory of Operation <ul style="list-style-type: none"> a. Systems Description (include block diagram). b. Detailed Description of Circuit Operation.

8	7	Maintenance <ul style="list-style-type: none"> a. Preventive Maintenance. b. Trouble Analysis. c. Trouble Shooting Sequence Chart. d. Wave Forms. e. Voltage Measurements. f. Alignment Procedures.
9	8	Parts List (include circuit and board designation, part type and class, power rating, component manufacturer, mechanical part manufacturer, data specification sheets for special design components and original manufacturer's part number).
10	9	Electrical Interconnection Details & Drawings.
11	10	Schematic and Logic Diagram.
12	11	Assembly Drawings and a pictorial diagram showing physical locations and identification of each component or part.

1.2.4.3 Cabinet Manuals

Manuals and Wiring Diagram Sheets for the Cabinet shall be furnished in a weatherproof plastic pouch placed in the cabinet. Cabinet Wiring Diagrams shall be on non-fading, minimum 22-inch x 34-inch sheets.

1.2.4.4 Draft

A preliminary Draft of the Manual shall be submitted to the Engineer for approval prior to final printing.

1.2.5 Packaging

Each item delivered shall be individually packed in its own shipping container. When loose styrofoam is used for packing the item, the item shall be sealed in a plastic bag to prevent direct contact with the styrofoam.

1.2.6 Delivery

Each item delivered for testing shall be complete, including manuals, and ready for testing.

1.2.7 Metal Edges

All sharp edges and corners shall be rounded and free of any burrs.

1.2.7.1 Aluminum

Aluminum sheets shall be Type 3003-H14 or Type 5052-H32 ASTM Designation B209 aluminum alloy. Rod, Bar and Extruded shall be Type 6061-T6, or equal.

1.2.7.2 Stainless Steel

Stainless Steel Sheets shall be annealed or one-quarter-hard complying with the ASTM Designation: A666 for Type 304, Grades A or B, stainless steel sheet.

1.2.7.3 Cold Rolled Steel

Cold Rolled Steel Sheets, Rods, Bars and Extruded shall be Type 1018/1020.

1.2.7.3.1 Plating

All cold roll steel shall be plated. All plating shall be either cadmium plating meeting the requirements of Federal Specification QQ-P-416C, Type 2 Class 1 or zinc plating meeting the requirements of ASTM B633-85 Type II SC4.

1.2.8 Mechanical Hardware

All Hardware bolts, nuts, washers, screws, hinges and hinge pins shall be stainless steel unless otherwise specified.

1.2.9 Electrical Isolation

Within the circuit of any device, module, or PCB, Electrical Isolation shall be provided between DC logic ground, equipment ground and the AC- (Neutral) conductor. They shall be electrically isolated from each other by 500 M Ω , minimum, when tested at the input terminals with 100 Volts DC.

1.2.10 Daughter Boards

Keyboards and LCD/LED Displays are considered daughter boards. Daughter boards shall be mechanically secured with four spacers / metal screws depending on the area supported. Connectors shall be either Flat Cable or PCB Headers. Components are allowed to be mounted under the daughter board.

CHAPTER 1-SECTION 3 COMPONENTS

1.3.1 General

All components shall be second sourced and shall be of such design, fabrication, nomenclature or other identification as to be purchased from a wholesale distributor or from the component manufacturer, except as follows:

1.3.1.1 Special Design

When a component is of such Special Design that it precludes the purchase of identical components from any wholesale distributor or component manufacturer, one spare duplicate component shall be furnished with each 20, or fraction thereof, components used.

1.3.1.2 Electronic Circuit

The Electronic Circuit design shall be such that all components of the same generic type, regardless of manufacturer, shall function equally in accordance with the specifications.

1.3.2 Electronic Components

1.3.2.1 Socket Mounted

NO device shall be Socket Mounted unless specifically called out or requested and approved at Qualified Product List Submittal.

1.3.2.2 Rated Power

NO component shall be operated above 80% of its maximum Rated Voltage, current or power ratings. Digital components shall not be operated above 3% over their nominal voltage, current or power ratings.

1.3.2.3 Manufactured Date

NO component shall be provided where the Manufactured Date is 3 years older than the contract award date. The design life of all components, operating continuously (24 hours a day, 365 days per year) in their circuit application, shall be 10 years or longer.

1.3.2.4 Encapsulation

Encapsulation of 2 or more discrete components into circuit modules is prohibited except for transient suppression circuits, resistor networks, diode arrays, solid-state switches, optical isolators, transistor arrays and termination networks. Components shall be arranged so they are easily accessible, replaceable and identifiable for testing and maintenance. Where damage by shock or vibration exists, the component shall be supported mechanically by a clamp, fastener, retainer, or hold-down bracket.

1.3.2.5 Contractor

The Contractor shall submit detailed engineering technical data on all components at the request of the Engineer. A letter from the component manufacturer shall be submitted with the detailed engineering data when the proposed application of the component alters the technical data. The letter shall certify that the component application meets specification requirements.

1.3.2.6 Temperature Rating

All components used shall be designed to operate within the full temperature range specified. The component data sheets shall be the only accepted form of validation of the temperature range. Testing and/or screening of commercial grade components is not permitted.

1.3.3 Capacitors

The DC and AC voltage ratings as well as the dissipation factor of a capacitor shall exceed the worst-case design parameters of the circuitry by 150% **except for Supercaps which shall be 110%. Supercaps are capacitors rated less than 10 working Volts DC with capacitance values greater than or equal to 1.0F.** Capacitor encasements shall be resistant to cracking, peeling and discoloration. **With the exemption of Surface Mount Capacitors,** all capacitors shall be insulated and shall be marked with their capacitance values and working voltages. Electrolytic capacitors shall not be used for capacitance values of less than 1.0 microfarad and shall be marked with polarity.

1.3.4 Potentiometers

Potentiometers with ratings from 1 to 2 watts shall meet Military Type RV4 requirements. Potentiometers with ratings less than 1 Watt shall be used only for trimmer type function. The potentiometer power rating shall be at least 100% greater than the maximum power requirements of the circuit.

1.3.5 Resistors

Fixed carbon film, deposited carbon, or composition-insulated resistors shall conform to the performance requirements of Military Specifications **MIL-PRF-22684F and Amendment 1.** All resistors shall be insulated and shall be marked, **except for surface mount,** with their resistance values. Resistance values shall be indicated by the EIA color codes, or stamped value. **The value of the resistors shall not vary by more than 5% between -34.6⁰F and 165.2⁰F.**

1.3.5.1 Thermal

Special Ventilation or Heat Sinking shall be provided for all 2-watt or greater resistors. They shall be insulated from the PCB.

1.3.6 Semiconductor-Devices

1.3.6.1 Solid State

All Solid State devices, except LED's, shall be of the silicon type.

1.3.6.2 Transistors / IC / Diodes

All Transistors, Integrated Circuits, and Diodes shall be a standard type listed by EIA. **With exemption of Surface Mount Components, Transistors, Integrated Circuits and Diodes shall be clearly identifiable.**

1.3.6.3 Metal Oxide Semi-Conductor

All Metal Oxide Semi-Conductor components shall contain circuitry to protect their inputs and outputs against damage due to high static voltages or electrical fields.

1.3.6.4 Device Pin 1

Device Pin "1" locations shall be properly marked on the PCB adjacent to the pin.

1.3.7 Transformers / Inductors

With the exemption of Surface Mount Components, all power transformers and inductors shall have the manufacturer's name or logo and part number clearly and legibly printed on the case or lamination. All transformers and inductors shall have their windings insulated, shall be protected to exclude moisture, and their leads color

coded with an approved EIA color code or identified in a manner to facilitate proper installation.

1.3.8 Triacs

Each triac with a designed circuit load of greater than 0.5 Amperes at 120 VAC shall be mounted to a heat sink with thermal conductive compound or material, in addition to being mechanically secured.

1.3.9 Circuit Breakers

Circuit Breaker shall be UL 489 approved. The trip and frame sizes shall be plainly marked (marked on the breaker by the manufacturer), and the Amperes rating shall be marked and visible from the front of the breaker. Contacts shall be silver alloy and enclosed in an arc-quenching chamber. Overload tripping shall not be influenced by an ambient air temperature range of from 0.4 °F to 122 °F. The minimum Interrupting Capacity shall be 5,000 Amperes, RMS when the breaker is secondary to a UL approved fuse or primary circuit breaker and both breakers in concert provide the rated capacity. For circuit breakers 80 Amperes and above, the minimum interrupting capacity shall be 10,000 Amperes, RMS. Circuit breakers shall be the trip-free type with medium trip delay characteristic (Carling switch Time Delay Curve #24 or equal).

1.3.10 Fuses

All Fuses shall be 3AG Slow Blow type and resident in a holder. Fuse size rating shall be labeled on the chassis, PCB or beside the holder. Fuses shall be easily accessible and removable without use of tools.

1.3.11 Switches

1.3.11.1 Dual-Inline-Package-(DIP)

Dual-inline-package, quick snap switches shall be rated for a minimum of 30,000 operations per position at 50 mA, 30 VDC. The switch contact resistance shall be 100 milliohms maximum at 2 mA, 30 VDC. The contacts shall be gold over brass (or silver). Contact for VAC or 28 VDC and shall be silver over brass (or equal). The DIP shall have recessed switches to prevent accidental switching.

1.3.11.2 5 VDC Logic Switch

5 VDC Logic rating shall be 0.4VA @ 20VAC or DC with contact material of gold over nickel plating or copper alloy. The switch shall be rated for a minimum of 40,000 operations.

1.3.11.3 12 -24 VDC Logic/Control Switches

12-24 VDC control switch contacts shall be rated for a minimum of five-Amperes resistive load at 120 VAC or 28 VDC and shall be gold over brass (or equal). The switch shall be rated for a minimum of 40,000 operations.

1.3.11.4 Power Rating

The switch contacts shall be rated for a minimum of 10 Amperes resistive load at 120 VAC or 28 VDC and shall be silver over brass or equal.

1.3.12 Terminal Blocks

The terminal blocks shall be barrier type, rated at 20 Amperes and 600 VAC RMS minimum. The terminal screws shall be 0.313 in minimum length nickel plated brass binder head type with screw inserts of the same material. Screw size is called out under the associated file, panel or assembly.

1.3.13 Wiring / Cabling / Harnesses

1.3.13.1 Harnesses

Harnesses shall be neat, firm and properly bundled with external protection. They shall be tie-wrapped and routed to minimize cross talk and electrical interference. Each harness shall be of adequate length to allow any conductor to be connected properly to its associated connector or termination point. Conductors within an encased harness have no color requirements. Printed circuit motherboards are to be used where possible to eliminate or reduce cabinet wiring.

1.3.13.2 AC Wiring

Wiring containing AC shall be bundled separately or shielded separately from all DC logic voltage control circuits.

1.3.13.3 Cabling

Cabling shall be routed to prevent conductors from being in contact with metal edges. Cabling shall be arranged so that any removable assembly may be removed without disturbing conductors not associated with that assembly.

1.3.13.4 Labeling

All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

1.3.13.5 Conforming

All conductors shall conform to MIL-W-16878G/1 or better and shall have a minimum of 19 strands of copper. The insulation shall be polyvinyl chloride with a minimum thickness of 10 mils or greater. Where insulation thickness is 15 mils or less, the conductor shall conform to MIL-W-16878/17.

1.3.13.6 Conductor Color

Conductor Color identification shall be as follows:

AC - (Neutral) circuits	White.
Equip. Ground	Solid green or continuous green color with 1 or more yellow stripes.
DC logic ground	Solid white or continuous white with a red stripe.
AC + (Line) circuits	Solid black or continuous black with colored stripe.
DC logic ungrounded or signal	Any color not specified.

1.3.14 Indicators / Displays

All indicators and character displays shall be readily visible at a radius of up to 4 ft within the cone of visibility when the indicator is subjected to 97,000 lux (9,000 foot-candles) of white light with the light source at 45 +/-2 degrees to the front panel.

1.3.14.1 Indicators

All indicators and character displays shall have a minimum 90 degrees cone of visibility with its axis perpendicular to the panel on which the indicator is mounted. All indicators shall be self-luminous. All indicators shall have a rated life of 100,000 hours minimum. Each LED indicator shall be white or clear when off and visibly illuminated when on. Indicators supplied on equipment requiring handles shall be mounted such that a horizontal clearance of 15 degrees minimum shall be provided for Models 208, 210, 212, 222, 232, 242 and 252, as well as a clearance of 30 degrees minimum for Models 200, 204 and 206.

1.3.14.2 Character Displays

Liquid Crystal Displays (LCD) shall operate at temperatures of -4 °F to 158 °F.

1.3.15 Connectors

1.3.15.1 Keyed

All connectors shall be keyed to prevent improper insertion of the wrong connector. The mating connectors shall be designated as the connector number and male/female relationship, such as C1P (plug or PCB edge connector) and C1S (socket).

1.3.15.2 Type T

The Type T connector shall be a single row, 10 position, feed through terminal block. The terminal block shall be a barrier type with 6-32, 0.25 in or longer, nickel plated brass binder head screws. Each terminal shall be permanently identified as to its function.

1.3.15.3 Plastic Circular / M Type

Plastic Circular and M Type connectors - Pin and socket contacts for connectors shall be beryllium copper construction sub-plated with 0.00005 in nickel and plated with 0.0000299 in gold. Pin diameter shall be 0.061811 in. All pin and socket connectors shall use the AMP #601105-1 or #91002-1 contact insertion tool and the AMP #305183 contact extraction tool.

1.3.15.4 Edge / PCB

Card Edge and Two-Piece PCB Connectors

1.3.15.4.1 PCB Edge

PCB Edge connectors shall have bifurcated gold-plated contacts. The PCB receptacle connector shall meet or exceed the following:

Operating Voltage:	600 VAC (RMS)
Current Rating:	5.0 Amperes
Insulation Material:	Diallyl Phthalate or Thermoplastic
Insulation Resistance:	5,000 MΩ
Contact Material:	Copper alloy plated with 0.00005 in of nickel and 0.000015 in of gold
Contact Resistance:	0.006 Ohm maximum

1.3.15.4.2 Two Piece PCB

The Two-Piece PCB connector shall meet or exceed the DIN 41612.

1.3.15.4.3 PCB 22/44

The PCB 22/44 Connector shall have 22 independent contacts per side; dual sided with 0.156 in contact centers.

1.3.15.4.4 PCB 28/56

The PCB 28/56 Connector shall have 28 independent contacts per side, dual sided with 0.156 in contact centers.

1.3.15.4.5 PCB 36/72

The PCB 36/72 Connector shall have 36 independent contacts per side, dual sided with 0.100 in contact centers.

1.3.15.4.6 PCB 43/86

The PCB 43/86 Connector shall have 43 independent contacts per side, dual sided with 0.100 in contact centers.

1.3.15.5 Wire Terminal Connectors

Each wire terminal shall be solderless with PVC insulation and a heavy-duty short - locking spade type connector. All terminal connectors shall be crimped using a Controlled-Cycle type crimping tool.

1.3.15.6 Flat Cable Connectors

Each flat cable connector shall be designed for use with 26 AWG cable; shall have dual cantilevered phosphor bronze contacts plated with 0.00015 of gold over 0.00005 inches of nickel; and shall have a current rating of 1 A minimum and an insulation resistance of 5 mega Ohms minimum.

1.3.15.7 PCB Header Post Connectors

Each PCB header post shall be 0.00155 in² by 0.343 in high; shall be mounted on 0.156 in centers; and shall be tempered hard brass plated with 0.000015 in of gold over 0.00005 in of nickel.

1.3.15.8 PCB Header Socket Connectors

Each PCB header socket block shall be nylon or diallyl phthalate. Each PCB header socket contact shall be removable, but crimp-connected to its conductor. The Contractor shall list the part number of the extraction tool recommended by its manufacturer. Each PCB header socket contact shall be brass or phosphor bronze plated with 0.00010 in of gold over 0.00005 in of nickel.

1.3.16 Surge Protection Device

A three-electrode gas tube type that is capable of withstanding 15 pulses of peak current each of which will rise in 8 μ s and fall in 20 μ s to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes. It shall have the following ratings:

Impulse Breakdown:	Less than 1,000 Volts in less than 0.1 us at 10 KV/us.
Standby Current:	Less than 1 mA.
Striking Voltage:	Greater than 212 Volts.

CHAPTER 1-SECTION 4 MECHANICAL

1.4.1 Assemblies

All assemblies shall be modular, easily replaceable and incorporate plug-in capability for their associated devices or PCBs. Assemblies shall be provided with 2 guides for each plug-in PCB or associated device (except relays). The guides shall extend to within 0.75 in from the face of either the socket or connector and front edge of the assembly. If Nylon guides are used, the guides shall be securely attached to the file or assembly chassis.

1.4.2 PCB Design

No components, traces, brackets or obstructions shall be within 0.125 in of the board edge (guide edges). The manufacturer's name or logo, model number, serial number, and circuit issue or revision number shall appear and be readily visible on all PCBs. Devices to prevent PC Board from backing out of their assembly connectors shall be provided.

1.4.3 Model Numbers

The manufacturer's model and serial number shall appear on the rear panel of all equipment supplied (where such panel exists). In addition to any assignment of model numbers by the manufacturer, the State model number shall be displayed on the front panel in bold type, at least 0.25 in high.

1.4.4 PCB Connectors

All PCB Connectors mounted on a motherboard shall be mechanically secured to the chassis or frame of the unit or assembly.

1.4.5 Fasteners

All screw type Fasteners shall utilize locking devices or locking compounds except for finger screws, which shall be captive.

1.4.6 Workmanship

Workmanship shall conform to the requirements of this specification and be in accordance with the highest industry standards.

1.4.7 Tolerances

The following tolerances shall apply, except as specifically shown on the plans or in these specifications:

Sheet Metal	+/- 0.0525 in
PCB	+/- 0.010 in
Edge Guides	+/- 0.015 in

CHAPTER 1-SECTION 5 ENGINEERING

1.5.1 Human Engineering

1.5.1.1 Equipment

The Equipment shall be engineered for simplicity, ease of operation and maintenance.

1.5.1.2 Knobs

Knobs shall be a minimum of 0.5 in diameter and a minimum separation of 0.5 in edge to edge.

1.5.1.3 PCB

PCBs shall slide smoothly in their guides while being inserted into or removed from the frame and shall fit snugly into the plug-in PCB connectors. PCBs shall require a force no less than 4.5 lbs or greater than 50 lbs for insertion or removal.

1.5.2 Design Engineering

The design shall be inherently temperature compensated to prevent abnormal operation. The circuit design shall include such compensation as is necessary to overcome adverse effects due to temperature in the specified environmental range. The design shall take into consideration the protection of personnel from all dangerous voltages.

1.5.3 Generated Noise

No item, component or subassembly shall emit a noise level exceeding the peak level of 55 dBa when measured at a distance of one meter away from its surface, except as otherwise noted. No item, component or subassembly shall emit a noise level sufficient to interfere with processing and communication functions of the controller circuits

CHAPTER 1-SECTION 6 PRINTED CIRCUIT BOARDS

1.6.1 Design, Fabrication and Mounting

The Design, Fabrication and Mounting of components and assemblies shall comply with the Association Connecting Electronics Industries Standards (IPC) as specifically listed in this specification. In the event of any conflict between the requirements of this specification and IPC standards, the IPC Standards shall govern.

1.6.1.1 Contacts on PCBs

All contacts on PCBs shall be plated with a minimum thickness of 0.00003 in gold over a minimum thickness of 0.000075 in nickel.

1.6.1.2 PCB Design

PCB design shall be such that when a component is removed and replaced, no damage is done to the board, other components, conductive traces or tracks.

1.6.1.3 Fabrication

Fabrication of PCBs shall be in compliance with **IPC-4101B and Amendment 2**, except as follows:

1.6.1.3.1 Copper Tracks

NEMA FR-4 glass cloth base epoxy resin copper clad laminates 0.0625 in minimum thickness shall be used. Inter-component wiring shall be by laminated copper clad track having a minimum weight of 1.0 ounces per square foot with adequate cross section for current to be carried. All copper tracks shall be plated or covered by solder mask to provide complete coverage of all exposed copper tracks. Jumper wires to external PCB components shall be from plated-through padded holes and as short as possible.

1.6.1.3.2 Pits, Dents, Bows and Twists

Grade of Pits and Dents shall be of Grade B or better. The permissible bow or twist shall be Class C or better.

1.6.1.4 Mounting

The mounting of parts and assemblies on the PCB shall conform to **IPC-2221A, Class 3**, except as follows:

1.6.1.4.1 Semiconductor Devices

Semiconductor devices that dissipate more than 250 mW or cause a temperature rise of 50 °F or more shall be mounted with spacers, transipads or heat sinks where applicable to prevent contact with the PCB.

1.6.1.4.2 Residual Flux

When completed, all residual flux shall be removed from the PCB.

1.6.1.4.3 Resistance

Except where Surface Mount Components are used, the resistance between any 2 isolated, independent conductor paths shall be at least 100 MΩ when a 500 VDC potential is applied.

1.6.1.4.4 Coated

All PCBs shall be conformal coated with a UV Tracer. This coating shall conform to the configuration of the object coated, applied on the completed board assembly. The coating shall be resistant to the affect of moisture and solvents.

1.6.1.4.5 Lateral Separation

Where less than 0.125 in lateral separation is provided between the PCB (or the components of a PCB) and any metal surface, a 0.03125 in \pm 0.0156 in thick Mylar (polyester) plastic cover shall be provided on the metal to protect the PCB.

1.6.1.5 Connector Edges

Each PCB connector edge shall be chamfered at 30 degrees from board side planes. The key slots shall also be chamfered so that the connector keys are not extracted upon removal of board or jammed upon insertion. The key slots shall be 0.045 in \pm 0.005 in for 0.1 in spacing and 0.055 in \pm 0.005 in for 0.156 in spacing.

1.6.2 Soldering

1.6.2.1 Hand Soldering

Hand soldering shall comply with [IPC-J-STD-00D and Amendments](#).

1.6.2.2 Automatic Flow Soldering

Automatic flow soldering shall be a constant speed, conveyor system with the conveyor speed set at optimum to minimize solder peaks or points. Temperature shall be controlled to within \pm 46.4 °F of the optimum temperature. The soldering process shall result in the complete coverage of all copper runs, joints and terminals with solder except that which is covered by an electroplating process. Wherever clinching is not used, a method of holding the components in the proper position for the flow process shall be provided.

1.6.2.3 Time-Temperature

If exposure to the temperature bath is of such time-temperature duration, as to come within 80% of any component's maximum specified time-temperature exposure, that component shall be hand soldered to the PCB after the flow process has been completed.

1.6.3 Definitions

Definitions for the purpose of this section on PCBs shall be taken from [IPC-613 and Amendment 1](#).

CHAPTER 1-SECTION 7 QUALITY CONTROL

1.7.1 Components

All components shall be lot sampled to assure a consistent high conformance standard to the design specification of the equipment.

1.7.2 Subassembly, Unit or Module

Complete electrical, environmental and timing compliance testing shall be performed on each module, unit, printed circuit or subassembly. Housing, chassis, and connection terminals shall be inspected for mechanical sturdiness, and harnessing to sockets shall be electrically tested for proper wiring sequence. The equipment shall be visually and physically inspected to assure proper placement, mounting, and compatibility of subassemblies.

1.7.3 Predelivery Repair

1.7.3.1 Defects / Deficiencies

Any defects or deficiencies found by the inspection system involving mechanical structure or wiring shall be returned through the manufacturing process or special repair process for correction.

1.7.3.2 PCB Flow Soldering

PCB flow soldering is allowed a second time if copper runs and joints are not satisfactorily coated on the first run. Under no circumstances shall a PCB be flow soldered more than twice.

1.7.3.3 Hand Soldering

Hand soldering is allowed for printed circuit repair.

CHAPTER 1-SECTION 8 ELECTRICAL, ENVIRONMENTAL AND TESTING REQUIREMENTS

1.8.1 General

The requirements called out in these specifications dealing with equipment evaluation are a minimum guide and shall not limit the testing and inspection to insure compliance.

1.8.2 Certification

These test procedures shall be followed by the Contractor who shall certify that they have conducted inspection and testing in accordance with these specifications.

1.8.3 Inspection

A visual and physical inspection shall include mechanical, dimensional and assembly conformance of all parts of these specifications.

1.8.4 Environmental and Electrical

All components shall properly operate within the following limits unless otherwise noted:

Applied Line Voltage: 90 to 135 VAC, note "Power Failure / Restoration" limits

Frequency: 60 (+/-3.0) Hertz

Humidity: 5% to 95%

Ambient Temperature: -34.6 °F to +165.2 °F

Shock - Test per Specification MIL-STD-810G Method 516.6.

Vibration - per Specification MIL-STD-810G Method 514.6.

1.8.4.1 Commencement Operation

All circuits, unless otherwise noted, shall commence operation at or below 90 VAC as the applied voltage is raised from 50 to 90 VAC at a rate of 2 (+/-0.5) volts / second.

1.8.4.2 Equipment Compliance

All equipment shall be unaffected by transient voltages normally experienced on commercial power lines. Where applicable, equipment purchased separately from the cabinet (which normally is resident) will be tested for compliance in a State accepted cabinet connected to the commercial power lines.

1.8.4.3 Power Line Surge Protection

The power line surge protection shall enable the equipment being tested to withstand (non-destructive) and operate normally following the discharge of a 25 μ F capacitor charged to $\pm 2,000$ volts, applied directly across the incoming AC line at a rate of once every 10 seconds for a maximum of 50 occurrences per test. The unit under test will be operated at 68 °F ± 41 °F and at 120 (± 12) VAC.

1.8.4.4 Operating

The equipment shall withstand (nondestructive) and operate normally when one discharge pulse of plus or minus 300 volts is synchronously added to its incoming AC power line and moved uniformly over the full wave across 360 degrees or stay at any point of Line Cycle once every second. Peak noise power shall be 5 kilowatts with a pulse rise time of 500 ns. The unit under test will be operated at 68 °F ± 41 °F and at 120 (+/-12) VAC.

1.8.4.5 Modules

The controller unit communications modules shall be tested resident in a State-accepted controller unit which in turn is housed in the cabinet.

1.8.4.6 CMS System Equipment

CMS system equipment will be tested for compliance as a complete system with power from commercial power lines applied at the CMS CIP Panel.

1.8.4.7 UL Requirements

Equipment shall comply only with the requirements of UL Bulletin of Research No. 23, "Rain Tests of Electrical Equipment."

1.8.4.8 Normal Operation

All equipment shall continue normal operation when subjected to the following:

1.8.4.8.1 Low Temperature Test

With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be lowered from 68 °F to 34.6 °F at a rate of not more than 64.4 °F per hour. The item shall be cycled at -34.6 °F for a minimum of 5 hours and then returned to 68 °F at the same rate.

1.8.4.8.2 High Temperature Test

With the item functioning at a line voltage over Electrical Range the Device in its intended operation, the ambient temperature shall be raised from 68 °F to 165.2 °F at a rate of not more than 64.4 °F per hour. The item shall be cycled at 165.2 °F for 5 hours and then returned to 68 °F at the same rate. The test shall be repeated with the line voltage at 135 VAC.

1.8.4.8.3 Normal Operation

All equipment shall resume normal operation following a period of at least 5 hours at -34.6 °F and less than 10 percent humidity and at least 5 hours at 165.2 °F and 22% humidity, when 90 VAC is applied to the incoming AC.

1.8.4.9 Humidity and Ambient Temperature

The relative humidity and ambient temperature values in the following table shall not be exceeded.

**AMBIENT TEMPERATURE VERSUS RELATIVE HUMIDITY
AT BAROMETRIC PRESSURES (29.92 In. Hg.)**

Ambient Temperature/ Dry Bulb (in °F)	Relative Humidity (in percent)	Ambient Temperature/ Wet Bulb (in °F)
-34.6 to 33.98	10	1.04 to 108.86
33.98 to 114.8	95	108.86
119.84	70	108.86
129.92	50	108.86
140.0	38	108.86
149.72	28	108.86
160.16	21	108.86
165.2	18	108.86

1.8.4.10 Opening and Closing of Contacts

All equipment shall be capable of normal operation following opening and closing of contacts in series with the applied voltage at a rate of 30 openings and closings per minute for a period of 2 minutes in duration.

1.8.5 Contractor's Testing Certification

1.8.5.1 QC / Final Test

A complete QC / final test report shall be supplied with each item. The test report shall indicate the name of the tester and shall be signed by a responsible manager.

1.8.5.2 Quality Control Procedure & Test Report

The quality control procedure and test report format shall be **supplied** to the Engineer for approval within 15 days following the award of the contract. The quality control procedure shall include the following:

Acceptance testing of all supplied components.

Physical and functional testing of all modules and items.

A minimum 100-hour burn-in of all equipment.

Physical and functional testing of all items.

CHAPTER 1-SECTION 9 CONNECTOR DETAILS

1.9.1	M104 – Connector	Appendix
1.9.2	M14 – Connector	A1-1
1.9.3	M50 & Circular Plastic Connectors	A1-2
1.9.4	M14S- Serial Connector	A1-3
		A1-4

Section Notes:

M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 Mega Ohms. The contacts shall be secured in the blocks with stainless steel springs.

M Type connector corner guides shall be stainless steel. The guide pins shall be 1.097 inches in length and the guide sockets shall be 0.625 inches in length.

Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated heat stabilized and fire resistant.

CHAPTER 2
MODEL 170E ENHANCED CONTROLLER &
ASSOCIATED MODULES SPECIFICATIONS

CHAPTER 2-SECTION 1 GENERAL

2.1.1 System READ Access Time

With Model 412C Module Resident in the Controller Unit, valid data shall be present at the MPU at least 100 ns prior to the end of the machine cycle.

2.1.2 Diagnostic and Acceptance Test (DAT) Program

The DAT-170E Program shall be provided resident on the Model 412C Program Module U1 memory device and on the CPU U6 memory device. A copy of the DAT Programs will be available to the contractor at no charge.

2.1.3 PAL, EPROM, or ROM Devices

If a PAL, EPROM, or ROM device is used in address decoding and timing algorithms, the device code listing together with data sheet(s) and any specific coding requirements shall be included in the unit or module documentation. The device coding shall be delivered in the same form that the Contractor uses to directly reproduce the device.

2.1.4 System Address Organization

The system address organization of the Model 170E shall consist of two addressing configurations. The Decoder Input shall be furnished jumpered in address configuration 1. The internal module address organization shall be as specified in the appropriate module section.

2.1.4.1 Configurations

The two addressing configurations shall be selectable by use of one post jumper. The jumper shall control the Logic State of one Decoder Circuit Input. The logic line shall be a three-post type with the two logic levels on the outer posts. The following input line state conditions shall cause the Decoder circuit to provide the associated address configurations:

<u>CONFIGURATION</u>	<u>LINE</u>	<u>FUNCTION</u>
1.	+5 VDC	170E / 412C
2.	DC GND	170E INTERNAL / 170

2.1.4.2 Configuration 1-Address Organization

FUNCTION	ADDRESS RANGE	COMMENTS
CPU SRAM	0000-0FFF	
U4 Memory	1000-3FFF	412C
Reserved	4000-4FFF	
DTA Minutes	5000	READ
DTA Reset	5000	WRITE
INPUT / OUTPUT	5001-5008	
	5009-500A	WRITE
RESTART State	5004	BIT 1 READ
DTA Seconds	500F	READ
Reserve	5009-500E	READ
	500B-500F	WRITE
	5010-5FFE	
CPU STATUS	5FFF	READ Bit 1 - ACIA #1 IRQ Bit 2 - ACIA #2 IRQ Bit 3 - ACIA #3 IRQ Bit 4 - ACIA #4 IRQ Bit 5 - Reserved Bit 6 - Address Configuration Bit 7 - DTA Timeout Bit 8 - RTC IRQ
RTC Reset	5FFF	WRITE
ACIA #1	6000	WRITE CR, READ SR
ACIA #1	6001	WRITE TDR, READ RDR
ACIA #2	6002	WRITE CR, READ SR
ACIA #2	6003	WRITE TDR, READ RDR
ACIA #3	6004	WRITE CR, READ SR
ACIA #3	6005	WRITE TDR, READ RDR
ACIA #4	6006	WRITE CR, READ SR
ACIA #4	6007	WRITE TDR, READ RDR
Reserve	6008-600F	
CPU SRAM	6010-6FFF	

Program Module

Memory Write Protect	7000	WRITE
I.D. Feature	7000	READ
I.D. Location	7001	READ
	7001	WRITE Reserve
Reserve	7002-7009	
	700B-700E	WRITE
	700F	READ
RTCA Valid/Reset	700A	
RTCA Counters 1 to 4	700B-700E	READ
U3 Memory	7010-7FFF	
U1 & U2 Memory	8000- FFFF	

Note -- Address locations noted as "Reserve" are assignable by the Agency only and shall not be used. CPU STATUS Bit 6: "0" equals Address Configuration 1 and "1" equals Address Configuration 2.

2.1.4.3 Configurations 2-Address Organization

Configuration 2 Address Organization - This configuration provides all Model 412C Program Module features internal to the controller unit. The address organization is the same as CONFIGURATION 1 with the following exceptions:

CPU SRAM	0000-3FFF	U3 & U4 Memory internal
	6010-6FFF	
	7010-7FFF	
U6 EPROM	8000-FFFF	U1 & U2 Memory internal

2.1.5 Memory Devices

Each memory device shall stabilize to normal operation within 10 ms following Power Restoration and shall be in Standby until addressed. Each device shall have the following maximum power drain at +5 VDC in its various states:

MEMORY	ACTIVE	STANDBY	POWERDOWN
EPROM	100 ma	40 ma	-
SRAM	85 ma	20 ma	100 µa (non-internal power)

2.1.6 Prom Memory Sockets

PROM Memory Sockets shall be a 28 Pin AMP Diplomate LF #641894-2, or equal. The MPU, ACIA and other memory sockets shall be an AUGAT #500/800 series AG10DPC or equal. Each socket number shall be permanently marked on the PCB adjacent to its Pin 1. Should the "... or equal MPU" Pin / Package be other than the 40 pin package, the MPU socket used shall match the above specified socket features.

CHAPTER 2-SECTION 2 MODEL 170E CONTROLLER UNIT

2.2.1 Unit Composition

2.2.1.1 170E Controller Consisting

The Model 170E Controller Unit shall consist of the following:

- Central Processing Unit (CPU)
- Input / Output Interface
- Unit Chassis
- M170E Auxiliary Board
- Model 412C Program Module
- Unit Power Supply with external power connection
- Unit Standby Power
- Front Panel Assembly
- Internal System Interface
- Connectors C1S, C2S, C20S, C30S, C40S, and T-1
- Communications System Interface

2.2.1.2 Configuration

The 170E shall be delivered pinned for Configuration 1 Addressing.

2.2.1.3 Composition Weight

The composition weight shall not exceed 25 lbs.

2.2.2 Central Processing Unit (CPU)

2.2.2.1 Micro Processing Unit (MPU)

The CPU shall be provided with an MPU and shall properly execute object programs developed to operate on the MPU. The MPU interrupt requirements shall be as follows:

2.2.2.1.1 Non-Maskable Interrupt (NMI)

The NMI is exclusively assigned to the Power Failure Function. A Power Failure shall cause the MPU NMI line to immediately go LOW. The line shall be held LOW until the RES goes LOW to prevent multiple NMI issuance.

2.2.2.1.2 Reset Interrupt (RES)

The RES is exclusively assigned to Power Restoration and MPU Startup. The RES line shall go LOW 3 (± 1) ms following the NMI going LOW. The line shall remain LOW until 150 (± 75) ms after Power Restoration.

2.2.2.1.3 Interrupt Request (IRQ)

The IRQ Line shall be jointly used by the RTC and Four ACIAs to initiate IRQ to the MPU.

2.2.2.1.3.1 Real Time Clock (RTC)

Real Time Clock circuitry shall be provided to trigger an interrupt to the MPU on the IRQ line once every 1/60 of a second during the 270 degree to 330 degree portion of the AC Sine Wave. The AC Sine Wave shall be derived from the local power company's 120 VAC 60 Hz frequency. The RTC shall be READ at Bit 8, Address 5FFF (STATUS) and reset by a WRITE to Address 5FFF.

2.2.2.1.3.2 ACIA

Four ACIAs shall be provided, each capable of receiving and transmitting up to eight-bits of parallel data from the MPU for serial data communications. The ACIA shall have 4 registers which are addressable by the MPU. The MPU shall be capable of reading the Status Register (SR) and the Receiver Data Register (RDR), and writing in the Transmit Data Register (TDR) and in the Control Register (CR).

2.2.2.1.3.3 Jumpers

Each ACIA shall be provided with a 2 post type jumper between its IRQ output and the MPU IRQ input. The 170E shall be delivered with these jumpers installed.

2.2.2.2 CPU Clock Timing

The CPU clock circuitry shall be provided to generate the MPU clock timing. The clock circuitry and the MPU shall provide two selectable MPU machine cycle times of 0.651 and 1.302 (± 0.0015) μ s. The machine cycle time selection shall be by Post Jumper (Three Post Type) with jumper in for 1.302 μ s. The CPU clock circuitry shall be located no further than 2 in from the MPU clock pin inputs.

2.2.2.3 SRAM Memory

SRAM Memory, DALLAS 1235Y or equal, shall be provided.

2.2.1.4 AN EPROM Memory

AN EPROM Memory, [ST Microelectronics M27C256B](#) or equal, shall be provided in socket U6.

2.2.2.4 Restart Timer

A Restart Timer Circuitry shall be provided to react to the duration of power outage. The Restart Timer output is normally HIGH. When the NMI line goes LOW, the Restart Timer shall begin timing. If the timer reaches 1.75 (± 0.25) seconds, its output state shall go to LOW and remain in that state for 50 (± 24) ms after the RES line goes HIGH. If power is restored prior to the timer timing out, the output shall remain HIGH and the timer shall be reset to "0".

2.2.3 DownTime Accumulator (DTA)

2.2.3.1 Power Failure and Restoration

A DTA shall be provided to accumulate time between Power Failure and Restoration. The DTA shall start counting immediately upon NMI line going LOW and continue counting until the RES line goes HIGH following Power Restoration.

2.2.3.2 Binary Registers

The DTA shall have 2 eight-bit binary registers counting the number of minutes and seconds. DTA accuracy shall be ± 1 second over the 255-minute range. The DTA shall stop counting when the Minutes register equals 255 decimal. Both DTA registers shall

reset to 0 by a WRITE to Address 5000. The DTA shall READ Minutes at Address 5000 and Seconds at Address 500F. The Seconds Register shall count 0 to 59 seconds decimal in 1-second increments. At 60 seconds, the Minutes Register shall be incremented and reset the other register to "0".

2.2.4 Current Drain

Total Current Drain for DTA AND Restart Timer Circuitry (powerdown mode) shall not exceed 400 μA at 5 VDC, 95⁰F while timing and 100 μA at 5 VDC when timeout is latched.

2.2.5 Input / Output Interface

2.2.5.1 Ground True Logic

Input / Output Interface shall utilize a ground true logic. The transfer of data between interface and working registers within the MPU shall be in eight-bit word increments, minimum. The steering of data from inputs or outputs for a given address shall be controlled by the state of the MPU read / write command at the time the given address is valid.

2.2.5.2 Output Interface

The output interface shall consist of a minimum of 80 bits of buffered storage. Output data shall be latched at the time of writing from the MPU. This interface shall provide an NPN open collector output capable of driving up to 40 VDC and sinking up to 100 mA. A "1" from the MPU shall be presented as a grounded collector, and a "0" presented as an open circuit. Once a port is written into, the data shall remain present and stable until either another word is written into it or until the power is turned off. The state of these output ports at the time of power up or below power failure threshold shall be an open circuit.

2.2.5.3 Input Interface

The input interface shall consist of a minimum of 64 bits of gated inputs from external devices. Each logic level input shall be turned ON (true) when the input voltage is less than 3.5 VDC, shall be turned OFF (false) when the input current is less than 100 μA or the input voltage exceeds 8.5 VDC, shall pull up to 12 VDC, and shall not deliver in excess of 20 mA to a short circuit to logic level common. When the appropriate input address is impressed upon the input interface, the interface shall place its data on the data bus, which will be read by the MPU. Ground on any input shall be interpreted by the MPU as a "1" and an open on any input or the presence of a voltage greater than 8.5 VDC shall be interpreted as a "0" by the MPU when that input is read.

2.2.6 Unit Chassis

The controller unit shall be housed in a compact, portable metal enclosure suitably protected against corrosion. The controller unit shall mount in a standard EIA 19-inch rack. The enclosure shall be designed for convenient removal of PCBs without the use of tools.

2.2.7 Unit Power Supply

2.2.7.1 Power Supply

A power supply shall be provided to produce all DC power necessary to operate the controller unit. In addition, the supply shall provide the following voltages and current:

1. 1000 mA at +12 VDC
2. 300 mA at -12 VDC
3. 500 mA at + 5 VDC
4. 400 mA at- 5 VDC

2.2.7.2 DC Ground

The DC ground shall not be connected to equipment ground.

2.2.7.3 Controller Unit power

Controller Unit power shall be held up (DC logic voltages at normal operating levels) for a minimum of 50 ±17 ms beyond the NMI line going LOW.

2.2.7.4 Maximum DC Voltage

The maximum DC voltage generated shall not exceed 45 volts.

2.2.7.5 Power Supply

The Power Supply shall be so designed that no further filtering regulation is needed for the required DC voltages.

2.2.7.6 Radio Frequency Suppressors

Radio frequency suppressors shall be provided on the AC+ and AC- power lines. The part shall be COR COM 3VS1 or equal.

2.2.8 Unit Standby Power

2.2.8.1 Standby Power Supply

A standby power supply shall be provided to retain power (minimum of 72 hrs) to the CPU Restart Timer, DTA and Internal RTCA during power failure in the controller unit. The supply shall consist of holdup Capacitors, capacitor charging circuitry and power sense / transfer circuitry.

2.2.8.2 Power Sense / Transfer Circuitry

The power sense / transfer circuitry shall sense power loss and transfer battery power immediately to the required circuits. The transfer circuitry shall isolate the capacitors by transistor or relay until power loss transfer. The circuitry shall sense power restoration and transfer back to the normal isolation mode.

2.2.8.3 Charging Circuit

A charging circuit which shall, under normal operating conditions, fully charge and float the standby capacitors consistent with manufacturer's recommendations.

2.2.9 Front Panel Assembly

2.2.9.1 Fastening / Removing

The front panel shall be securely fastened to the chassis and removable without the need for tools. A continuous hinge shall be provided on the left side of the unit to permit opening of the front panel and ready access to the interior of the controller unit.

2.2.9.2 Connection

The front panel shall be electrically connected by means of Connector C3. The front panel shall be connected to equipment ground through Connector C3.

2.2.9.3 Character Displays

The character displays shall be hexadecimal with circuits to accept, store, and display four-bit binary data. The characters shall be 0.4 in high, minimum. Each character shall have latch strobe and blanking inputs. The second character from the right (lower row) shall have a right decimal point. The face of the character display shall be scratch and solvent-resistant. The transfer of data from the MPU through the output interface to the display shall result in the display of each character in its non-inverted state.

2.2.9.4 Indicators

The front panel shall be provided with 10 LED CALL / ACTIVE indicators.

2.2.9.5 Keyboard

A keyboard shall be provided. The transfer of data from the keyboard by way of the input interface to the MPU shall result in each character being received in its non-inverted state. The character shall consist of 4 bits of binary data, while the character control shall consist of 1 bit. A low state on the character control to the interface shall indicate the presence of a valid character. Each key shall be engraved or embossed with its function character, shall have a minimum surface area of 0.075 in² and shall be mounted on a minimum of 0.5 in centers; shall have an actuation force between 0.0001102 lbs and 0.0002205 lbs and shall provide a positive tactile indication of contact. Key contacts shall have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact opening.

2.2.9.6 Toggle LOGIC Switch

The front panel shall be provided with a toggle LOGIC switch to enable the stop timing function and shall be labeled "STOP TIMING".

2.2.9.7 Toggle CONTROL Switch and Fuse

An ON-OFF toggle CONTROL switch and fuse shall be provided for AC power. The switch and fuse shall protrude through the front panel, but shall remain with the controller unit chassis when the front panel is removed. The fuse shall be a 3AG Slow Blow type, rated at either 1 or 2 Amperes, dependent upon the controller unit power requirements.

2.2.9.8 Framework

The front panel, under the legend "OPERATING INSTRUCTIONS", shall include a framework to retain a card, 4 in wide by 6 in high by 0.063 in thick.

2.2.10 Internal System Interface

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2.2.10.1 Connector Spacing

PCB to PCB Connector spacing shall be a minimum of 1 in. Continuous nylon card guides (permanent locking type) shall be provided for the modules and all internal PCBs.

2.2.10.2 22/44S & 36/72S PCB Connectors

Two PCB 22/44S Connectors shall be provided for the MODEM Modules MC1 and MC2, and two PCB 36/72S Connectors shall be provided for the M170 Connector / Program Module and the M170 Connector / M170E Auxiliary Board.

2.2.10.3 Depth Placement

The depth placement of the vertical M/170 Connector shall be such that the Program Module Front Panel shall be flush with the Model 170E Controller Unit Front Panel when the module is connected.

2.2.11 Data and Address Bus Requirements

2.2.11.1 Data Bus Buffers and Drivers

All Data Bus Buffers and Data Bus Drivers shall be tri-state buffered devices enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. The propagation delay time shall be less than 30 ns.

2.2.11.2 Address Bus Inputs

All Address Bus Inputs shall be buffered and shall load the bus by 1 TTL gate load and 100 picofarads.

2.2.12 Connector Requirements

2.2.12.1 Connector C1S

Connector C1S shall be mounted on the controller unit providing 44 inputs and 56 outputs of control interface to and from external devices or files.

2.2.12.2 400 MODEM and CPU ACIA Connections

The Model 400 MODEM and CPU ACIA connections into and out of the controller unit shall be made through Connector C2S, C20S, C30S, C40S, and Terminal Block T-1 (TYPE T Connector). The control and data transmission lines for ACIA 1 shall be paralleled through C2S and T-1 connectors. ACIA 2 lines shall be routed to C20S Connector, ACIA 3 to C30S, and ACIA 4 to C40S.

2.2.12.3 Signal Lines and Buffer

ACIA 4 RS 232 Signal Lines and Buffered mirrored signals NMI, RES and ROT Shall be internally route to M170 and M170E as noted in Pin Assignments under Section 5 Details.

2.2.13 Communication System Interface

2.2.13.1 Communication Consisting

The communication system shall consist of the CPU, ACIAs, motherboard connectors and lines, MODEM Module Connectors MC1 & MC2 and interfaces between ACIA & MODEM and both MODEM and ACIA to C2S, C20S, C30S, C40S and Connector / T-1 Terminal. The interface between the ACIA and MODEM shall comply with EIA RS-232-C Standards and all functions under T-1, C2, C20S, C30S, and C40S Connectors are referenced to the ACIA. AUDIO IN and AUDIO OUT are referenced to the MODEM. The RTS and TX Data lines to the MODEM shall have MARK and SPACE Voltages of -12 and +12 VDC respectively.

2.2.13.2 Connectors

C20S, C30S, and C40S Connectors shall meet the requirements for the C2S Connector.

2.2.13.3 Frequencies

A minimum of four baud rate generator frequencies, 19.2 kHz, 38.4 kHz, 76.8 kHz and 153.6 kHz shall be provided at the ACIA Rx / Tx Clock Inputs (pins 3 & 4). The frequency selection shall be by post type jumpers. Each ACIA shall have independent baud rate selection with jumpers delivered pinned for 19.2 kHz.

2.2.14 Electrical Requirements

2.2.14.1 Connection

The front panel and chassis shall be connected to equipment ground.

2.2.14.2 Surge Arrestor

A surge arrestor shall be provided between the AC+ and AC- for protection against powerline noise transients. The surge arrestor shall meet the following requirements:

1. Recurrent peak voltage: 212 Volts
2. Energy rating maximum: 20 Joules
3. Power dissipation, average: 0.85 Watt
4. Peak current for pulses less than 6 us: 2000 Amperes
5. Standby current: less than 1 mA

2.2.14.3 Power Resistors / Inductance

Two 0.5 Ohm, 10 watt wire-wound power resistors with a 0.2μH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three surge arrestors rated for 20 Joules shall be supplied between AC+ and ground, AC- and ground, and between AC+ and AC-. A 0.68μF capacitor shall be added between AC+ and AC- coming off the 0.5 Ohm resistor going to the surge arrestors.

2.2.14.4 AC Power

The AC power to the controller unit shall be supplied by a 3-conductor cable at least 3 feet in length. The cable shall terminate in a NEMA Type 5-15P grounding type plug.

2.2.14.5 Test Points

Test points shall be provided for monitoring all power supply voltages. All test points shall be readily accessible when the front panel is opened. Any provided test point shall be isolated such that attaching a test probe shall not impact the operation of the

controller unit. The test points shall be post type, 0.063 in diameter and 0.19 in high, minimum. The clearance between test points and other components shall be 0.25 in, minimum.

2.2.15 M170E Auxiliary Board

2.2.15.1 M170E Auxiliary Board

The M170E Auxiliary Board shall contain the RTCA Circuitry and the Identification Switches. (See Section 3 for the RTCA circuitry and the Identification Switch requirements.) The RTCA circuitry and the Identification Switches on the M170E Auxiliary Board shall be disabled when a Model 412C is installed. The M170 connector pins 71 and / or 72 shall provide a DC Ground path via the Model 412C Module (pins 69 & 70) to M170E connector (pins 71 & 72). A ground true present shall cause board feature disablement.

2.2.15.2 PCB Dimensions

The M170E Auxiliary Board's PCB dimensions shall meet the Model 400 Modem except for the PCB edge connector dimensions.

2.2.15.3 PCB Connector

The M170E Auxiliary Board's PCB connector shall be a PCB 36 / 72 and shall mate with the M170E connector.

CHAPTER 2-SECTION 3

MODEL 400, 400B AND 400BE MODEM MODULE

2.3.1 Modems

The Modems shall provide two-wire half-duplex and four-wire full-duplex communications. It shall be switch selectable between half duplex and full duplex. In half duplex, pins X and Y shall be used for Audio IN / OUT.

2.3.2 Compliance

The Modems shall be compatible with Bell Standard 202S and comply with the following requirements:

Model	Mark Hz	Space Hz	Soft Carrier Hz	Data Rate bps
400	1200	2200	900	300 - 1200
400B	11200	17600	7800	300 - 9600
400BE	19200	38400	13800	300 - 19200

2.3.2.1 Modulation

Modulation: Phase coherent frequency shift keying (FSK).

2.3.2.2 Data Format

Data Format: Asynchronous, serial by bit.

2.3.2.3 Line and Signal Requirements

Line and Signal Requirements: Type 3002 voice-grade, unconditioned.

2.3.2.4 Interface

ACIA and Modem Interface: EIA - 232 Standards.

2.3.2.5 Tone Carrier Frequencies

Tone Carrier Frequencies (Transmit & Receive): **MARK and SPACE with ±1% tolerance.** The operating band shall be (half power, -3dB) between 1000 and 2400 Hz.

2.3.2.6 Transmitting Output Signal Level

Transmitting Output Signal Level: 0, -2, -4, -6 and -8 dB (at 1700 Hz) continuous or switch selectable.

2.3.2.7 Receiver Input Sensitivity

Receiver Input Sensitivity: 0 to -40 dB.

2.3.2.8 Receiver Bandpass Filter

Receiver Bandpass Filter: Shall meet the error rate requirement and shall provide 20 dB/Octave, minimum active attenuation for all frequencies outside the operating band.

2.3.2.9 Clear-to-Send (CTS)

Clear-to-Send (CTS) Delay: 12 (±2) ms.

2.3.2.10 Receive Line Signal Detect Time

Receive Line Signal Detect Time: 8 (±2) ms mark frequency.

2.3.2.11 Receive Line Squelch

Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

2.3.2.12 Turn Off Time

Soft Carrier Turn Off Time: 10 (±2) ms.

2.3.2.13 Modem Recovery Timer

Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

2.3.2.14 Error Rate

Error Rate: Shall not exceed 1 bit in 100,000 bits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3000 Hz band.

2.3.2.15 Transmit Noise

Transmit Noise: Less than -50 dB across 600 Ohm resistive load within the frequency spectrum of 300 to 3000 Hz at maximum output.

2.3.3 Modem Power Requirements

The Modem power requirements are as follows:

Input Voltage	Maximum Current Consumption
+12 VDC	75 Milliamperes
-12 VDC	75 Milliamperes

2.3.4 Indicators

Indicators shall be provided on the front of the MODEM to indicate Carrier Detect, Transmit Data, and Receive Data.

CHAPTER 2-SECTION 4

MODEL 412C PROGRAM MODULE

2.4.1 General Requirements

2.4.1.1 Prevention

A device shall be provided to prevent the module, when inserted upside down, from making contact with the modules' mating connector within the controller unit.

2.4.1.2 Module PCB Connector

The module PCB Connector shall be provided with electrostatic discharge protection to prevent CMOS device damage.

2.4.1.3 VMA / Phase 2 (E) Clock Signal

The VMA / Phase 2 (E) Clock Signal (M/170 Pin 25) shall not be used in a memory device READ operation.

2.4.1.4 Current Requirements

The total module current requirements shall not exceed 450 mA at +12 VDC and 100 mA at +5 VDC.

2.4.1.5 Program Model 412 Identifier

Address 700E, Bit 8 shall permanently Read as "1". This bit state is used to differentiate between past delivered Model 412/64 modules (Bit 8 decoded "0") and the Model 412C module.

2.4.1.6 Module PCB Connector

The module PCB connector shall be a PCB 36/72P.

2.4.1.7 Module Front Panel

The module front panel shall be connected to Equipment Ground at M170 Pin 34.

2.4.1.8 Addressable Devices

All addressable devices shall be fully decoded.

2.4.1.9 Memory Sockets

All memory sockets shall be a 28 pin AUGAT #528/828 Series AG10DPC or equal.

2.4.2 Feature Requirements

2.4.2.1 Bus Inputs and Outputs

2.4.2.1.1 Data Lines

All data lines shall be tri-state buffered on the module enabling them to drive a load consisting of 10 TTL gates and 200 picofarads. When this module is not being addressed, the data output lines shall be disabled into a high impedance state and the data lines shall not source or sink more than 100 μ A.

2.4.2.1.2 Addressed Input Lines

All addressed input lines shall load the bus by 1 TTL gate load and 100 picofarads. The propagation delay time shall be less than 30 ns.

2.4.2.2 Memory

2.4.2.2.1 Memory Sockets

Four numbered memory sockets shall be provided and fully decoded using the following method. The module shall be delivered with MEMORY SELECT #3 Configuration designated memory devices (OR EQUAL), address decode and jumpers.

2.4.2.2.2 Device Manufacturer

Device manufacturer is designated as INT-Intel, D-Dallas and HD-Hitachi. The sockets shall be decoded by block jumper selection as follows:

	MEMORY	SOCKET ADDRESS RANGE AND			JUMPER		
	SELECT		DEVICE		PATTERN		
	<u>U1</u>	<u>U2</u>	<u>U3</u>	<u>U4</u>	<u>1</u>	<u>2</u>	<u>3</u>
1.	E000-FFFF INT2764A	C000-DFFF INT2764A	7010-7FFF DAL1225	1000-4FFF HD6264 OR HD62256	IN	IN	OUT
2.	C000-FFFF INT128A	8000-BFFF NT128A	SAME	SAME	OUT	IN	IN
3.	8000-FFFF	NOT ADRS	SAME	SAME	OUT	OUT	IN
4.	8000-FFFF INT27256A	3000-4FFF DAL1225	SAME	1000-2FFF SAME *	OUT	OUT	OUT

* The pin #26 jumper pattern shall provide either address line 13 for the HD62256 device or tied HIGH for CS2 function in HD6264. Pin 27 shall be assigned to WE function.

2.4.2.2.3 Jumper Positions

Jumper positions for Sockets U2 and U4 shall be provided to convert the sockets from an EPROM socket to a SRAM socket or vice versa. Jumper positions for Sockets U2, U3 and U4 shall be provided to convert the socket from a non-standby power socket to a standby power socket or vice versa. Sockets U2 and U3 shall be jumpered for non-standby power. Socket U4 shall be jumpered for standby power.

2.4.2.2.4 Write Protect Circuit (WPC)

A Write Protect Circuit (WPC) shall be provided to prevent writing to SRAM memory during the Controller Unit MPU RESET Interrupt Line in a LOW State. A WRITE to ADDRESS 7000 shall be decoded and shall activate the WPC to place the R/W in a READ ONLY State. A subsequent WRITE to ADDRESS 7000 shall be decoded and shall deactivate the WPC allowing R/W function. The WPC state shall be brought out to address 700E, Bit 7 ("1" State means "active"). The WPC power drain shall not exceed 40 μ A at +5 VDC.

2.4.2.3 Module Power Supply

2.4.2.3.1 Power Supply

A power supply shall be provided onboard the module consisting of a DC Regulation Circuit, Standby Power and all necessary support circuitry.

2.4.2.3.2 DC Regulator Device

A DC Regulator device with its circuitry shall be provided to reduce the +12 VDC to +5 VDC for module use. The Regulator shall have a minimum efficiency of 75% and provide +5 \pm 0.25 VDC from no load to full load with a maximum of 2% ripple.

2.4.2.3.3 Standby Power

Standby power shall be provided to holdup WPC, SRAM and RTCA circuits during a Model 170 Controller Unit Power Failure. A circuit shall be provided to sense the +12 VDC M/170 power line and switch to standby power when the line falls below +9

VDC. The standby power circuit shall switch off when the power line is greater than +11 VDC. The standby power shall be a standard "AA" cap terminal cell battery rated at a minimum of 1.6 Ampere-hours at 3.7 ±0.2 VDC. All module circuitry and devices shall not exceed a maximum power drain of 2 mA at 3.7 VDC on the Standby Battery.

2.4.2.3.4 Battery

The battery shall be delivered separate from the module. It shall not be used except for test loading check by the Contractor.

2.4.2.3.5 Battery Holder

A battery holder for a “AA” battery shall be provided securely mounted to the back of the front panel. The holder shall have a TAB header type connector attached to the battery's plus cathode mounting terminal.

2.4.2.4 Identification Switch Circuitry

2.4.2.4.1 Switch Packages and Associated Circuitry

Two identification packages 8-position SPST DIP switches and associated circuitry shall be provided. The switch packages shall be decoded at Address 7000 (features) and 7001 (locations). Each package shall have 8 SPST switch positions with each switch associated to a DATA Bit (Switch 1 to Bit 1 and so on). Switch ON shall denote a bit state and shall be read logic "1" by the 170 CPU MPU and Switch OFF shall denote bit state and shall be read logic "0" by the 170 CPU MPU.

2.4.2.4.2 Switch Package

The Switch Package shall be a DIP slide type.

2.4.2.5 Real Time Clock Adjuster (RTCA)

2.4.2.5.1 RTCA Adjusting

A RTCA shall be provided to adjust for missing RTC timing interrupts.

2.4.2.5.2 RTCA Accuracy

The RTCA shall be continuously powered and not affected by a controller unit power failure. RTCA accuracy shall be ±10 ppm at 77 °F. Integral devices incorporating RTCA features and functions may be used in lieu of individual components. The RTCA current drain shall not exceed 1.5 mA at +3.7 VDC.

2.4.2.5.3 Pulse Generator (PG)

The RTCA shall include a free running 60 Hz Pulse Generator (PG), a 24 bit binary counter counting 60 Hz pulses, 4 eight-bit buffer ports and port decode / PG interrupt logic. The PG shall trigger binary counter to increment on every input pulse, counting continuously until reset to 0 by its Reset Line. Bits 21, 22, 23 and 24 in an all "1"'s state shall cause that PG to be disabled (Binary Counter Bit 1 is the least significant bit).

2.4.2.5.4 Counter Bits

The counter bits shall be continuously read out to 4 eight-bit buffer ports. The ports shall be addressed and bits assigned as follows:

CPU ADDRESS	PORT BITS	COUNTER BITS	COMMENTS
-------------	-----------	--------------	----------

700A	This address shall normally READ (decode) "55 HEX". If the standby power supply fails or is removed, it shall decode "54 HEX". A WRITE to this address will RESET the RTCA Binary Counter.		
700B	1-6	1-6	READ Only
700C	1-6	7-12	READ Only
700D	1-6	13-18	READ Only
700E	1-6	19-24	READ Only

2.4.2.5.5 LOGIC Switch

A SPST finger throw LOGIC switch shall be provided on the board to activate/deactivate standby power to the RTCA Circuitry. With the switch in the deactivated state the RTCA Circuitry shall present NO power drain to the standby power supply.

CHAPTER 2-SECTION 5 MODEL 400N ETHERNET MODULE

2.5.1 Model 400N Ethernet Module

The Model 400N Ethernet Module shall provide an EIA-232 Asynchronous communications channel. The Model 400N Ethernet Module shall be a 170 plug-in module with EIA-232 activity LEDs on the front edge. The Network Model 400N Ethernet Module shall communicate over standard IEEE 802.3 networks using both TCP (point-to-point) and UDP (point-to-multipoint) protocols.

2.5.2 Mechanical/Electrical Requirements

The Model 400N Ethernet Module shall be dimensionally and electrically designed to fit in a single slot of a standard 170 controller. All components shall be protected from physical damage by a metal cover.

All EIA-232 LED Indicators shall be on the Front Panel.

The Model 400N Ethernet Module shall be provided with LED indicators for 10/100 and Half/Full Duplex Network Communications.

The Main Data Port shall be a 170 male 44 pin edge connector (PCB 22/44) located at the rear. The User Serial port shall be a DB9 Female connector accessible from the front. The Network port shall be a RJ45 modular jack connector accessible from the front. DIP switches shall be externally accessible. The Model 400N Ethernet Module shall be powered directly from the Model 170 Controller's Edge Connector (PCB 22/44).

2.5.3 Functional Requirements.

The Model 400N Ethernet Module shall interface to the 170 controller using controller's Main Port EIA-232.

The Main and User Serial Ports shall operate EIA-232 Asynchronous communications and shall support data rates of 1.2, 2.4, 9.6, 19.2, 38.4, 57.5 and 115.2Kbps.

The Model 400N Ethernet Module Network Interface shall meet IEEE 802.3 and ANSI 8802-3 Standards and support 10/100 Mbps.

The Auxiliary Port shall be configurable to operate as a DCE or DTE.

2.5.4 Network Configuration

The Model 400N Ethernet Module shall support the following features:

TCP and UDP over IP protocols.

Subnet masks for Class A, B, and C networks (see table below):

NETWORK CLASS	HOST BITS	Subnet Mask	Example IP Address
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100

C	8	255.255.255.0	192.168.0.100
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Manual or Automatic TCP/IP socket connections configuration.

Telnet access for both configuration and communications.

Dumb Terminal access using a User Serial port for configuring network parameters.

The Ability to adjust packet size and packing algorithm.

The Model 400N Ethernet Module shall be provided with a Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and Serial Settings using a Web Browser.

2.5.5 Data Interfaces

Main Data Port Model 170 male 44 pin Edge Connector

User Serial Port EIA-232 (DB9 Female)

Ethernet Data Port **RJ45 EIA 568B Pin Out**

2.5.6 Switch Selections for half duplex and full duplex

User Serial Port Directionality DTE/DCE

Main Port Operation Enabled / Disabled

DCD Constant / Switched

RXD Data Flow Control Constant / Switched

2.5.7 LED Indicators

RTS **Green or Red:** DTE Request to Send

CTS **Green or Red:** Network Clear to Send

TXD **Green or Red:** DTE Transmit EIA-232 Data

RXD **Green or Red:** DTE Receive EIA-232 Data

CD **Green or Red:** Network Data

2.5.8 Power Requirements

170 Module +12 VDC, 3 Watts

2.5.9 Environmental

The Model 400N shall operate within the specification listed in Chapter 1 Section 1.8.4.

CHAPTER 2-SECTION 6 MODEL 400F FIBER OPTICS MODULE

2.6.1 Model 400F Fiber Optics Module

The Model 400F Fiber Optics Module shall provide an RS232 Asynchronous communications channel. The Model 400F Fiber Optics Module (Model 400F) shall be a Plug-in Card style version for the 170 Controller. The Fiber Optic Model 400F shall operate over Single Mode Fiber.

2.6.2 Mechanical/Electrical Requirements

The Plug-in Card Model 400F shall have a protective cover or enclosure. The Model 400Fs card edge connector shall be fully compatible with the 170 Controller's Modem card slot. The Auxiliary Data port shall be a RJ45 connector. All DIP Switches shall be accessed externally without disassembly of the Model 400F. The Model 400F will be powered direct from the 170 Controller's edge connector.

2.6.3 Fiber Optics Module Requirements

The Model 400F shall meet the Fiber Optics Requirements of the Model 2070-6D Module as specified elsewhere in these specifications.

2.6.4 Electro Optical Requirements

The Model 400F shall meet the Electro Optical Requirements of the Model 2070-6D Module as specified elsewhere in these specifications.

2.6.5 Form Factor

See A2-8 for details

2.6.6 Power Requirements

The Model 400F shall draw less than 500mA on Model 170 \pm 12VDC Power Supply.

2.6.7 Environmental

The Model 400F shall operate within the specifications listed in Chapter 1 Section 1.8.4

CHAPTER 2-SECTION 7 MODEL 170E DETAILS

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2.7.1 Model 170E Controller Unit Diagram	A2-1
2.7.2 Model 170E Controller Unit Block Diagrams	A2-2
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2.7.8 Model 400F Fiber Module	A2-8

NOTES:

1. Program module' height and width dimensions are maximum.
2. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.
3. All function under connector C2 & the terminal block T-1 are in reference to the MODEM
4. Detail Definitions:
 - BL** = BLANKING
 - CC** = CHARACTER CONTROL OR STROBE
 - CD** = CARRIER DETECT
 - CH** = CHARACTER
 - CTS** = CLEAR TO SEND
 - DP** = DECIMAL POINT
 - LS** = LEAST SIGNIFICANT
 - MS** = MOST SIGNIFICANT
 - NA** = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
 - NLS** = NEXT LEAST SIGNIFICANT
 - NMS** = NEST MOST SIGNIFICANT
 - P&I** = PHASE AND INTERVAL
 - RTS** = REQUEST TO SEND

CHAPTER 3
AUXILIARY CABINET SPECIFICATIONS

CHAPTER 3-SECTION 1 GENERAL REQUIREMENTS

3.1.1 Models 200 and 204 General

3.1.1.1 Unit Chassis

The unit chassis shall be made of metal suitable to meet rigid support and environmental requirements. Where electrical isolation is the only requirement, plastic insulation material can be used in lieu of metal.

3.1.1.2 Unit Control Circuitry and Switches

The unit control circuitry and switches shall be readily accessible by the use of a screwdriver or wrench. Only one type of screw head end (Slotted or Phillips) shall be used.

3.1.1.3 Unit Handle

The unit shall be so constructed that no live voltage is exposed. A handle shall be attached to the front panel for insertion or removal from the unit mating connector.

3.1.1.4 Unit Lower Surface

The unit shall be so constructed that its lower surface shall be no more than 2.06 in below the centerline of the connector and no part shall extend more than 0.9 in to the left or 1.1 in to the right of the connector centerline.

3.1.1.5 Edge Guides

Continuous edge guides shall be provided on the unit.

3.1.1.6 Switching

Each switch shall be capable of switching any Current from 0.050 to 10.0 Amperes (AC) load with power factor of 0.85 or higher.

3.1.1.7 Operations

Each switch shall be designed for a minimum of 300 Million operations while switching a tungsten load of 1000 Watts at 158 °F. Switch isolation between DC input and AC output circuit shall be at least 10,000 Mega Ohms at 2000 VDC.

3.1.1.8 Positions

Each switch shall turn ON within ± 5 degrees of the zero voltage point of the AC sinusoidal line, and shall turn OFF within ± 5 degrees of the zero current point of the alternating current sinusoidal line. After power restoration, the zero voltage turn ON may be within ± 10 degrees of the zero voltage point only during the first half cycle of line voltage during which an input signal is applied. Turn ON and OFF shall be within 8.33 ms following application or removal of the logic signal, respectively.

CHAPTER 3-SECTION 2 MODEL 200 SWITCH PACK UNIT

3.2.1 Switches

The Model 200 Switch Pack Unit shall be a modular plug-in device containing three solid-state switches. Each switch shall open or close a connection between applied power and external load.

3.2.2 Grounds

A Ground True Controller Unit Input (0 to 6 VDC) shall cause the switch to energize and a Ground False (16 VDC or more) shall cause it to de-energize, State transition shall occur between 6 and 16 VDC. The input shall not sink more than 20 ma or be subjected to more than 30 VDC. The input shall have reverse polarity protection.

3.2.3 Maximum Currents

With all switches on, the unit shall not draw more than 60 mA at +16 VDC or more from the +24 VDC cabinet supply.

3.2.4 Rating

Each switch shall have an OFF state dv/dt rating of 100 V/ μ s or better. Each switch shall be isolated so that line transients or switch failure shall not alter the controller unit.

3.2.5 Unit Front Panel

The unit front panel shall have an indicator on the input to each switch. The indicator shall be labeled or color-coded “Red”-top switch, “Yellow”-middle switch, and “Green”-bottom switch. The middle switch indicator shall be vertically centered on the unit front panel with the other indicators positioned 1 inches above and below.

3.2.6 Resistance

The resistance between the AC+ input terminal and the AC+ output terminal of each switch shall be a minimum of 15K Ohms when the switch is in open state. When the switch is in off state the output current through the load shall not exceed 10 mA peak.

CHAPTER 3-SECTION 3
MODELS 204 - FLASHER UNIT AND
205 – TRANSFER RELAY UNIT

3.3.1 Model 204 Flasher Unit

3.3.1.1 Flasher Unit

The Flasher Unit shall be a modular plug-in device containing a flasher control circuit and two solid-state switches. The unit's function is to alternatively open and close connections between applied power and external load.

3.3.1.2 Internal DC Power

The unit shall generate its own internal DC power from the AC Line.

3.3.1.3 Flashing

The unit shall commence flashing operation when AC power is applied providing 50 to 60 flashes per minute per switch with a 50 % duty cycle.

3.3.1.4 Rating

Each switch shall have an OFF state dv /dt rating of 200 V/ μ s or better.

3.3.1.5 Indicator

An indicator showing the switch's output state shall be provided. The two indicators shall be centered with 1 in minimum spacing.

3.3.1.6 Operation

Each circuit shall be designed to operate in an open-circuit condition without load for 10 years minimum.

3.3.1.7 Arrestor

A surge arrestor shall be provided between AC (pin 11) and Flasher Output (pins 7 & 8). The arrestor shall meet the following requirements:

Recurrent Peak Voltage	212 Volts
Maximum Energy Rating	50 Joules
Average Power Dissipation	0.85 Watts
Peak I for pulses less than 6 μ s	2000 Amperes
Standby I	less than 1 mA

3.3.2 Model 205 Transfer Relay Unit

3.3.2.1 Type

The Transfer Relay Unit shall be of electromechanical type, designed for continuous duty:

3.3.2.2 Cover

Each unit shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating, and part number shall be placed on the cover. They shall be durable, permanent and readily visible.

3.3.2.3 Contacts

Each unit shall be provided with DPDT contacts. The contact points shall be of fine silver, silver alloy or a superior alternate material. Contact points and arms shall be capable of switching 20 Amperes or 1 Kilowatt Tungsten Load at 120 VAC per contact at least 100,000 operations without contact welding or excessive burning, pitting or cavitation. The points and arms shall be able to withstand 0.1 DA or 10 Gs, 10 –55 Hz without contact chatter.

3.3.2.4 Relay Coil

The relay coil shall have a power consumption of 2.0 Volt - Ampere maximum.

3.3.2.5 Relay Potential and Rating

Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a one cycle surge rating of 175 Amperes RMS and pickup and drop out within 20 ms.

CHAPTER 3-SECTION 4 MODEL 206L POWER SUPPLY UNIT

3.4.1 Unit Chassis

The unit chassis shall be vented. The power supply cage and transformers shall be securely braced to prevent damage in transit. When resident in the PDA, the units shall be held firmly in place by its stud screws and wing nut.

3.4.2 Unit Design

The unit shall provide +24 VDC to the cabinet files. The unit shall be a **Switch-Mode design**. It shall conform to the following requirements:

3.4.2.1 Input Protection

Two 0.5 Ohm, 10-watt wire-wound power resistors with a 0.2 μ h inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arrestors shall be provided between AC+ to AC, AC+ to EG, and AC- to EG. A 0.68 μ f. capacitor shall be placed between AC+ & AC- (between the resistors & arrestors).

3.4.2.2 Output Protection

The output shall be fused for over-current protection. The output shall also be protected against voltage transients by a suppressor with minimum rating of 1400 Watts.

3.4.2.3 Input and Output fuses

Input/Output fuse protection shall comply with IEC-60127.

3.4.2.4 Line and Load Regulation

Line and Load Regulation- shall not exceed +23 to + 25 VDC (4.2%) with a design voltage of +24 VDC at full load.

This includes ripple noise; from 90 to 135 VAC at 60 Hz, plus an additional 1.6% for each additional 1.0% frequency change; and current range from 1 to 5 Amperes with a maximum temperature rise of 86 $^{\circ}$ F above ambient.

3.4.2.5 Design Voltage

Design Voltage +24 \pm 0.5 VDC at full load, 86 $^{\circ}$ F, 115 VAC incoming voltage.

3.4.2.6 Full Load Current

Full Load Current 5 Amperes each for +24 VDC, minimum.

3.4.2.7 Ripple Noise

Ripple Noise - 2 volts peak-to-peak and 500 mV RMS at full load.

3.4.2.8 Efficiency

Efficiency (at full load) - 80% minimum.

3.4.2.9 Power Factor Correction

The Model 206L Power Supply shall include power factor correction circuitry resulting in a minimum full load power factor of 0.96.

3.4.2.10 Circuit Capacitors

Circuit capacitors shall be rated for 40 volts minimum.

3.4.3 Front Panel and Terminals

The front panel shall include AC and DC fuses, power ON light and test points for monitoring the output voltages. The unit including terminals shall be protected to prevent accidental contact with energized parts.

3.4.3.1 LED Indicators

LED indicators shall be provided on the Front Panel indicating AC Line input status and fuse integrity. The indicators shall also display output status and fuse integrity of the 24VDC output.

CHAPTER 3-SECTION 5 MODEL 208 MONITOR UNIT

3.5.1 **Monitoring**

The Model 208 Monitor Unit shall reliably sense and cause a relay output contact (Failed State) when monitoring the following:

1. A Watchdog Timer (WDT) Timeout Condition
2. Cabinet +24 VDC Power Supply below specified threshold

3.5.2 **WDT Monitor Requirements**

3.5.2.1 **WDT Circuitry**

WDT Circuitry shall be provided to monitor a controller unit output line state routed to the monitor unit at its assigned pin. The WDT Circuitry shall sense any line state change and the time between the last change. No state change for 1.56 ± 0.1 seconds shall cause a Failed State. The timer shall reset at each state change in a Non Failed state.

3.5.2.2 **Unit Reset / WDT**

Only the Unit Reset or a WDT inactive due to the voltage sense shall reset the WDT from a failed state.

3.5.2.3 **Failed State**

A Failed state caused by the WDT shall illuminate a front panel indicator light labeled "WDT ERROR". The indicator shall remain ON until Unit Reset Issuance.

3.5.2.4 **WDT Circuitry**

The WDT Circuitry shall sense the incoming VAC Line and when the voltage falls below 98 ± 2 VAC for 50 ± 17 ms shall inhibit the WDT Function. When the WDT Circuitry senses the incoming VAC Line rise above 103 ± 2 VAC for 50 ± 2 ms the WDT shall become active. A hysteresis between the Voltage Inhibit and the Voltage Active Settings shall be a minimum of 3 Volts.

3.5.3 **Power Supply Monitor Requirements**

3.5.3.1 **Monitor Unit**

The monitor unit shall sense the Cabinet +24 VDC Power Supply Output Voltage. Voltages sensed at +18 VDC or below for a duration of 500 ms or longer shall cause a Failed state. Voltages sensed at +22 VDC or above shall NOT cause a failed state. Voltages sensed below +22 VDC for a duration of 200 ms or less shall NOT cause a Failed state. All timing and voltages conditions other than those specified above may or may not cause a failed state.

3.5.3.2 **Indicator**

A Failed state caused by sensing the power supply shall illuminate a front panel indicator light labeled "VDC FAILED". The indicator shall remain ON until Unit Reset.

3.5.3.3 **Unit Reset**

Only Unit Reset shall reset the power supply sense circuitry from a **Failed State**.

3.5.4 **Failed State Output Circuits**

An electro-mechanical relay shall be provided to switch an output circuit during a **Failed State**. The relay coil shall be energized in a Non Failed State. The relay

contacts shall be rated for a minimum of 3 **Amperes** at 120 VAC and 100,000 operations. Contact opening/closing time shall be 30 ms or less.

3.5.5 Monitor Unit Reset

A momentary SPST Control switch labeled “RESET” shall be provided on the unit front panel to reset the monitor unit circuitry to a Non Failed state. The switch shall be so positioned on the front panel that the switch can be operated while gripping the front panel handle.

3.5.6 Provision

The unit shall be provided with provision to drive an external NE2H light through a 56 K Ohm, 1/2 Watt series resistor (resident on unit).

3.5.7 PDA #3 WDT Reset Input

The PDA #3 WDT Reset Input shall not be sensed by the unit.

3.5.8 Output Relay

The output relay Contact for Failed State shall be Open.

CHAPTER 3-SECTION 6 MODEL 210 MONITOR UNIT

3.6.1 Monitor Unit Conditions

The Monitor Unit shall sense the following conditions and cause a FAILED STATE should any of the conditions exist:

1. The cabinet +24 VDC power supply below the voltage threshold.
2. The WDT Timeout Condition.
3. Conflicting field Output Circuit ON Condition.

3.6.2 Requirements

See Chapter 3, Section 5 Model 208 Monitor Unit for requirements on Power Supply Monitoring, Watchdog Timer, Failed State Output Circuits and Monitor Unit Reset.

3.6.3 Conflict Monitoring

The monitor shall sense up to 16 Channels for conflict (32 field outputs of Green and Yellow). The Green and Yellow are Logically OR'd together. The associated cabinet output file assignment or operator selected output switches shall determine channel assignment.

3.6.3.1 Monitored Field Output Voltages

All monitored field output voltages shall be measured as true RMS responsive (up to 3 KHz) to both positive and negative alternations of the sine wave and the full cycle. The calculated value shall be averaged over a minimum of 2 cycles. If digital means are used in calculating RMS, a minimum of 2 samples shall be taken per alternation.

3.6.3.2 Sensed Conflicting Field Output Voltages

Sensed conflicting field output voltages 25 VAC or greater for a duration of 500 ms or longer shall cause a Failed state. Sensed conflicting field output voltages between 15 VAC or less OR any voltage having a duration of 200 ms or less shall NOT cause a Failed state(s).

3.6.3.3 Conflict Monitoring Circuitry

The Conflict Monitoring Circuitry shall be capable of detecting both a positive and negative half-wave failure under the foregoing conditions.

3.6.3.4 Failed State

A Failed state caused by sensing voltage conflicts shall be reset only by the Unit Reset.

3.6.3.5 Indicators

Sixteen indicators shall be provided on the unit front panel to indicate if the channel output is sensed ON. The indicators shall remain ON in a latched state during a Failed state unless unlatched by Unit Reset or a unit loss of power during said Failed state.

3.6.4 Conflict Programming Card

3.6.4.1 PCB Programming Card

A plug-in PCB Programming Card shall be provided in the monitor unit. The card shall plug into the unit through a slot in the unit front panel. The card shall contain 120 diodes (#1N4148 or equal). Each diode shall match 1 through 16 channels of possible conflict. The programming card shall be logically labeled and laid out for easy identification of the diodes by channel. With diodes in place all output channels being

monitored shall be in conflict. When the diode (anode to numerical pins and cathode to alphabetical pins) has been removed the channels shall be defined as non-conflict.

3.6.4.2 Pad / Placement

A pad for 16 yellow inhibit jumpers shall be provided. Placement of the associated channel jumpers shall be provided. Placement of the associated channel jumper between the channel yellow pin the yellow inhibit common shall disable sensing the said channel yellow.

3.6.4.3 Connection

The programming card shall intermate with a PCB 28/56S Connector. The card shall be provided with card ejectors. The monitor unit shall provide a mechanically sound card and connector support including continuous card guides. When the programming card is resident in the unit, the card's front end shall be flushed with the unit's front panel.

3.6.4.4 Pins 16 and T

Pins 16 and T shall be connected together on the programming card. Removal of the card shall be sensed as a conflicting FAILED state.

3.6.5 Conflicting

A front panel indicator labeled "CONFLICT" shall be provided. The indicator shall illuminate when there is a FAILED state caused by conflicting channels and go off only by Unit Reset Issuance.

3.6.6 Output Relay Contact

The output relay contact for FAILED State shall be "CLOSED".

3.6.7 Second Output Circuit

A second output circuit (STOPTIME controller input) shall be provided to sink a NPN Open Collector Transistor upon FAILED state. The transistor shall be rated to sink a minimum of 50 ma at up to 30 VDC. A blocking diode shall be provided on the transistor output to prevent it from sourcing power into the controller unit.

3.6.8 LOGIC Toggle Switch

An internal SPST LOGIC toggle switch shall be provided on the Model 210 Monitor Unit to activate the WDT function. When the switch is ON the WDT Circuitry shall be active. The switch shall be mounted on the module PCB in a readily accessible location.

3.6.9 RESET Switch

The Front Panel RESET Switch shall be tied to the External Test Reset Input Line (Pin Z). The External Line shall be optically isolated from internal circuitry

**CHAPTER 3-SECTION 7
MONITOR UNITS & POWER SUPPLY DETAILS**

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3.7.1 Model 200 Switch Pack & Model 204 & 205 Connector Details	A3-1
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CHAPTER 4
REFER TO BATTERY BACKUP SYSTEM
SPECIFICATIONS

CHAPTER 5
SPECIFICATIONS DETECTOR SENSOR UNITS,
ELEMENTS AND ISOLATORS

CHAPTER 5-SECTION 1 GENERAL REQUIREMENTS

5.1.1 Sensor and Isolator Channels

The sensor and isolator channels shall be operationally independent from each other. Each sensor or isolator channel shall draw no more than 50 mA from the +24 VDC cabinet power supply and shall be **insensitive to 700 mVolts** RMS ripple on the incoming +24 VDC line.

5.1.2 Front Panel

The sensor unit or isolator front panel shall be provided with the following:

Hand pull to facilitate insertion and removal from the input **file**.

Control switches **and Channel Indicators**.

Channel visual indication of detection or incoming signal.

5.1.3 Output

Each sensor or isolator channel output shall be an opto-isolated NPN Open Collector capable of sinking 50 mA at 30 VDC. The output shall be compatible with the controller unit inputs. **The output shall have a minimum impedance of 2 Mega Ohms when no vehicle is detected.**

5.1.4 Valid Channel Input

A valid channel input shall cause a channel Ground True Output to the controller unit of a minimum 100 ms in duration. An onboard two-post shunt jumper shall be provided to disallow this requirement when the jumper is in a OPEN position.

5.1.5 Sensor Unit

The sensor unit or sensing element shall operate and interface successfully with an associate CALTRANS Standard Sensing Unit or Element.

5.1.6 Output Transistor

The output transistor shall switch from OFF to ON state or ON to OFF state in 20 μ s or less.

5.1.7 Onboard Protection

Onboard protection shall be provided to enable the sensor unit or isolator to withstand the discharge of a 10 μ F capacitor charged to +/- 1000 Volts directly across the input pins with no load present. With a dummy load of 5 Ohms, protection shall enable the sensor unit or isolator to withstand the discharge of a 10 μ F capacitor charged to +/- 2000 Volts directly across either the input pins or from either side to equipment ground.

CHAPTER 5-SECTION 2 MODEL 222 & 224 LOOP DETECTOR SENSOR UNIT REQUIREMENTS

5.2.1 Sensor Unit Channel

The sensor unit channel shall produce an output signal when a vehicle passes over or remains over wire loops embedded in the roadway. The method of detection shall be based upon a design that renders the output signal when a metallic mass (vehicle) enters the detection zone causing a change of 0.02% minimum decrease in inductance of the circuit measured at the input terminals of the sensor unit. The detector zone shall include all configurations listed in paragraph 5.2.9.1.

5.2.2 Open Loop

An open loop shall cause the sensor unit channel to output a signal.

5.2.3 Detection

Each sensor unit channel shall be capable of detecting all types of California licensed motor vehicles when connected to the loop configuration/lead-in requirements of 5.2.9.1

5.2.4 Sensor Unit Compliance

The sensor unit shall comply with all performance requirements when connected to an inductance (loop plus lead-in) from 50 to 700 μ H with a Q-parameter as low as 5 at the sensor unit operating frequency.

5.2.5 Loop Inputs

Loop inputs to each channel shall be transformer isolated.

5.2.6 Switches

Each individual channel shall have a minimum of 4 switch selectable operating frequencies.

5.2.7 Tuning Circuits

The sensor unit channel tuning circuits shall be automatic and shall be so designed that drift caused by environmental changes, or changes in applied power shall not cause an actuation.

5.2.8 Modes Selection Requirements

Each sensor unit channel shall have Pulse and Presence selectable modes.

5.2.8.1 Pulse Mode

5.2.8.1.1 Vehicle Presence

In the Pulse Mode, each new vehicle presence within the detection zone shall initiate a sensor unit channel output pulse of 125 (\pm 25) ms in duration.

5.2.8.1.2 Detection Zone

Should a vehicle remain in a portion of the detection zone for a period in excess of 2 seconds, the sensor unit channel shall automatically “tune out” the presence of said vehicle. The sensor unit channel shall then be capable of detecting another vehicle entering the same detection zone. The recovery time to full sensitivity between the first vehicle pulse and channel capability to detect another vehicle shall be 3 seconds maximum.

5.2.8.2 Presence Mode

5.2.8.2.1 Duration

In the Presence Mode, the sensor unit channel shall recover to normal sensitivity within 1 second after termination of vehicle presence in the detection zone regardless of the duration of the presence.

5.2.8.2.2 Presence Sensitivity Settings

The channel sensitivity settings shall be provided that detect the presence of a vehicle in the detection zone for a specified time period and inductance change(s). The conditions are as follows:

	Minimum Time Duration	Detector Input Inductance Change
Setting 6	3 Minutes	0.02% or more
	10 Minutes	0.06% or more
Setting 2	4 Minutes	1.00% or more

5.2.9 Sensitivity

5.2.9.1 Standard Plans Loop Configurations

California Standard Plan ES-5A & B Loop Configurations. (California Department of Transportation Standard Plans.)

5.2.9.1.1 Single Type-250

Single Type A, B, Q or Round Loop with a 250 ft lead-in cable.

5.2.9.1.2 Single Type-1000

Single Type A, B, Q or Round Loop with a 1000 ft lead-in cable.

5.2.9.1.3 4 Type-Series/Parallel-250

4 Type A, B, or Q Loops connected in series/parallel with a 250 ft lead-in cable.

5.2.9.1.4 4 Type-Series-1000

4 Type A, B, Q or Round Loops connected in series with a 1000 ft lead-in cable.

5.2.9.1.5 Type C-250

One 50 foot Type C Loop with a 250 ft lead-in cable.

5.2.9.2 Sensitivity Settings

Each sensor unit channel shall be equipped with a front panel selectable sensitivity setting(s) in presence and pulse modes to accomplish the following under operational and environmental requirements of this specification.

5.2.9.2.1 Setting 2

Each sensor unit channel shall respond while in setting 2 to a nominal change in inductance between 0.15% to 0.4% (median sensitivity of 0.32%) while connected to the above 5.2.9.1 loop configuration. This setting shall not respond to an inductance change of less than 0.1%

5.2.9.2.2 Setting 6

Each sensor unit channel shall respond while in the setting 6 to an induction of 0.02% while connected to the above 5.2.9.1 loop configuration.

5.2.9.3 Vehicle Detection

The sensor unit channel shall not detect vehicles, moving or stopped, at distances of 3 ft or more from any loop perimeter, in all configurations listed in paragraph 5.2.9.1

5.2.9.4 Differ

All sensitivity settings shall not differ +/- 40% from the nominal value chosen.

5.2.9.5 Selectable Sensitivity Setting(s)

There shall be a minimum of 7 selectable sensitivity settings including specified sensitivity settings.

SETTING	SENSITIVITY	SETTING	SENSITIVITY
1	0.64%	5	0.04%
2	0.32%	6	0.02%
3	0.16%	7	0.01%
4	0.08%	8	Channel OFF

5.2.10 Response Time

Response time of the sensor unit channel for Sensitivity Setting, 2 shall be less than 5 ± 1 ms. That is, for any decreased inductive change which exceeds its sensitivity threshold, the channel shall output a ground true logic level within 5 ± 1ms. When such change is removed, the output shall become an open circuit within 5 ± 1ms.

5.2.11 Normal Operation

The sensor unit channels shall begin normal operation within 2 seconds after the application of power or after a reset signal of 30 μs.

5.2.12 Lightning Protection

Lightning Protection shall be installed within the sensor unit as defined in the Section 5.1.7 of these specifications.

5.2.13 Tracking Rate

The sensor unit shall be capable of compensating or tracking for an environmental change up to 0.001% change in inductance per second.

5.2.14 Tracking Range

5.2.14.1 Inductance

The sensor unit shall be capable of normal operation as the input inductance is changed $\pm 5.0\%$ from the quiescent tuning point regardless of internal circuit drift.

5.2.14.2 Resistance

The sensor unit shall be capable of normal operation as the input resistance is changed $\pm 0.5\%$ from the quiescent tuning point regardless of internal circuit drift.

5.2.15 Temperature Change

The operation of the sensor unit shall not be affected by changes in the inductance and/or capacitance of the loop caused by environmental changes with the rate of temperature change not exceeding 1°C per 3 minutes. The opening or closing of the controller cabinet door with a temperature differential of up to 18°C between the inside and outside air shall not affect the proper operation of the sensor unit.

5.2.16 Switch

A switch or switch position shall be provided on the front panel to disable each channel output.

CHAPTER 5-SECTION 3 MAGNETIC DETECTOR REQUIREMENTS

5.3.1 Model 231 Magnetic Detector Sensing Element

5.3.1.1 Sensing Element

Each sensing element shall be designed for ease of installation, repositioning, and removal. The sensing element shall be 2.24 in maximum in diameter, have no sharp edges, and its length not to exceed 18 in. The sensing element shall be constructed of nonferrous material and shall be moisture proof. The element shall contain no moving parts or active components. The element shall have a 100 ft lead-in cable. Leakage resistance shall be a minimum of 10 MegaOhms when tested with 400 VDC between lead wire, including lead wire entrance, and the fluid of a salt water bath after the device has been entirely immersed in the bath for a period of 24 hours at 68 °F +/- 37.4 °F. The salt water bath concentrate shall be one fourth ounce of salt per gallon of water.

5.3.1.2 Lead-In

Each sensing element including lead-in shall have a DC resistance of less than 3500 Ohms and an inductance of 20 Henrys +/- 15 %.

5.3.2 Model 232 Two Channel Magnetic Detector Sensing Unit

5.3.2.1 Sensing Channel

When resident in an active cabinet input assembly and attached to one or more Model 231 Sensing Elements resident in conduit [under the travel way](#), the sensing channel shall output a Ground True Output to the Controller Unit when sensing an induced voltage caused by a California Licensed Vehicle passing within 6 ft from an element with a 1000 ft of lead-in cable at all speeds between 3.11 and 80.78 mile per hour. The sensing channel output shall be continuous as long as the vehicle is detected. [A rotary sensitivity adjusting knob for Gain \(0 to Full\)](#) and a momentary test switch providing a voltage test input shall be furnished for each channel on the front panel.

CHAPTER 5-SECTION 4

MODEL 242 TWO-CHANNEL DC ISOLATOR REQUIREMENTS

5.4.1 Model 242 DC Isolator Channel

The Model 242 DC Isolator Channel shall provide isolation between a VDC input circuit (external electrical switch closure) and the controller unit input. The minimum isolation shall be 1000 MegaOhms and 2,500 VDC measured between the input and the output of the same channel.

5.4.2 Test Switch

Each isolation channel shall have a front panel mounted test switch to simulate valid input. The test switch shall be a single-pole double-throw, three position CONTROL test switch: The position assignment shall be UP – constant ON; MIDDLE – OFF; and DOWN – momentary ON.

5.4.3 Internal Power Supply

The isolator shall have an internal power supply supplying 20 +/- 4 VDC to the field input side of the isolation channels. The isolator shall not draw more than 2.5 watts of AC power. No current shall be drawn from the cabinet power supply. **PCB should be two layer design minimum, using plated-thru vias, and Gold Plated Fingers on Both Sides of PCB.**

5.4.4 Channel Contact Closure Input

A channel contact closure input of 2 ms or less shall not cause an output (ground true) to the controller. An input of 7 ms or greater shall cause an output to the controller. An input of duration between 2 and 7 ms may or may not cause an output to the controller.

5.4.5 Field Input

Each isolation channel field input shall be turned on (true) when a contact closure causes an input voltage of less than 8 VDC, and shall be turned off (false) when the contact opening causes the input voltage to exceed 12 VDC. Each input shall deliver no less than 15 mA nor more than 40 mA to an electrical contact closure or short from the power supply.

CHAPTER 5-SECTION 5

MODEL 252 TWO-CHANNEL AC ISOLATOR

5.5.1 Model 252 Two-Channel AC Isolator

The Model 252 Two-Channel AC Isolator shall contain 2 isolation channels which provide isolation between external 120 VAC input circuits and the controller unit input circuits. The method of isolation shall be based upon a design which provides reliable operation.

5.5.2 Channel Input Voltage “Von”

A channel input voltage “Von” of 80 +/- 5 VAC applied for a minimum duration of 110 ms ± 10 ms shall cause an output (Ground True) to the controller unit.

5.5.3 Channel Input Voltage “Voff”

A channel input voltage “Voff” (Von minus 10 VAC) applied for a minimum duration of 110 ms ± 10ms shall cause an output (Ground False) to the controller unit.

5.5.4 Post Jumper

A two post jumper shall be provided to select inverted output states for Von and Voff. When in CLOSED position (Grounded) Von shall cause a Ground False output. An indicator shall be provided on the front panel labeled ‘RR’ which shall indicate a Voff input, Ground True output.

5.5.5 Input Impedance

The input impedance of each channel shall be between 6,000 - 15,000 Ohms at 60 Hz.

5.5.6 Minimum Isolation

The minimum isolation shall be 1000 MegaOhms between the input and output terminals at 500 AC applied voltage.

**CHAPTER 5 SECTION 6
SENSOR & ISOLATOR DETAILS**

5.6.1 Sensor Unit and Isolator

**Appendix
A5-1**

CHAPTER 6
CABINET SPECIFICATIONS
MODELS 332L, 334L & 336L

CHAPTER 6-SECTION 1 GENERAL REQUIREMENTS AND CABINET MODEL COMPOSITION

6.1.1 Composition

Unless otherwise specified the model shall be furnished, ready for operation with the following composition.

6.1.1.1 Model 332L Cabinet

Model 332L Cabinet shall consist of:

Housing 1 B	Output File #1
Mounting Cage 1	C1 Harness #1
Power Distribution Assembly #2	Service Panel #1
Input Files I & J	Input Panel #1

6.1.1.2 Model 334L Cabinet

Model 334L Cabinet shall consist of:

Housing 1 B	PDA Assembly #3
Mounting Cage 1	C1 Harness #2
Input File I	Service Panel #1
Input Panel #3	

6.1.1.3 Model 336L Cabinet

MODEL 336L CABINET shall consist of:

Housing 2	Output File #1
Mounting Cage 2	C1 Harness #3
Power distribution Assembly #2	Service Panel #2
Input File I	Input Panel #4

6.1.1.4 Assemblies and Files

All assemblies and files shall be mounted on the cage mounting rails per cabinet model detail. Cabinet model interface wiring shall be per specified C1 Harness, detailed wiring lists and required One Line Wiring.

6.1.2 Cabinet Shipping Requirements

The cabinet shall be delivered mounted on a plyboard shipping pallet. The pallet shall be bolted to the cabinet base. The cabinet shall be enclosed in a slipcover cardboard packing shell. The housing doors shall be blocked to prevent movement during transportation.

6.1.3 Cabinet Adaptors

When specified, adaptors shall be provided. The adaptor shall be fabricated of the same material and finish as the cabinet housing.

6.1.4 Stainless Steel

All bolts, nuts, washers, screws (size 8 or larger), hinges and hinge pins shall be stainless steel unless otherwise specified.

6.1.5 Cage Mounting

A cage mounting clear area for the controller unit shall be provided. The area shall

extend 1.5 inches in front of and 16 inches behind the front EIA mounting angles.

6.1.6 Protection

All conductors, terminals and parts which could be hazardous to maintenance personnel shall be protected with suitable insulating material.

CHAPTER 6-SECTION 2 HOUSING REQUIREMENTS

6.2.1 Housing

The housing shall include, but not be limited to, the following:

Enclosure	Police Panel
Doors	Ventilization
Latches/Locks	Gasketing
Hinges and Door Catches	Cage Supports and Mounting

6.2.2 Housing Construction

6.2.2.1 Waterproof

The housing shall be rainproof with the top of the enclosure crowned to prevent standing water. It shall have single front and rear doors, each equipped with a lock.

6.2.2.2 Fabricating

The enclosure, doors, lifting eyes, gasket channels, police panel, and all supports welded to the enclosure and doors shall be fabricated of 0.125 in minimum thickness aluminum sheet. Bolted on supports shall be either the same material and thickness as the enclosure or 0.105 in minimum steel. The side panels and filter shell shall be fabricated of 0.080 in minimum thickness aluminum sheet.

6.2.2.3 Exterior

All exterior seams for enclosure and doors shall be continuously welded and shall be smooth. All edges shall be filed to a radius of 0.03125 in minimum. Exterior cabinet welds shall be done by gas Tungston arc TIG process only. ER5356 aluminum alloy bare welding electrodes conforming to AWS A5.10 requirements shall be used for welding on aluminum. Procedures, welders and welding operators shall conform to the requirements and practices in AWS B3.0 and C5.6 for aluminum. Internal cabinet welds shall be done by either gas metal arc MIG or gas Tungston arc TIG Process.

6.2.2.4 Aluminum surfaces

Aluminum surfaces shall conform to the following:

6.2.2.4.1 Anodic Coating

An anodic coating shall be applied to the aluminum surface after the surface has been cleaned and etched. The cleaning and etching procedure shall be to immerse in inhibited alkaline cleaner at 159.8 °F for 5 minutes (Oakite 61A, Diversey 909 or equivalent in mix of 6 ounces to 8 ounces per gallon to distilled water). Rinse in cold water. Etch in a sodium solution at 150.8 °F for 5 minutes 0.5 ounce sodium fluoride plus 5 ounces of sodium hydroxide mix per gallon to distilled water. Rinse in cold water. Desmut in a 50% by volume nitric acid solution at 68 °F for 2 minutes. Rinse in cold water.

6.2.2.4.2 Conforming

The anodic coating shall conform to MIL-A-8625F (Anodic Coatings for Aluminum and Aluminum Alloys) for Type II, Class I Coating except the outer housing surface coating shall have a 0.0007 inch minimum thickness and a 0.952 ounces per square inch minimum coating weight. The anodic coating shall be sealed in a 5% aqueous solution of nickel acetate (PH 5.0 to 6.5) for 15 minutes at 210.2 °F.

6.2.2.5 Enclosure Doorframes

The enclosure doorframes shall be double flanged out on all 4 sides and shall have strikers to hold tension on and form a firm seal between the door gasketing and the frame. The dimension between the door edge and the enclosure external surface when the door is closed and locked shall be 0.156 (+/- 0.08) in.

6.2.2.6 Gasketing

Gasketing shall be provided on all door openings and shall be dust-tight. Gaskets shall be 0.25 inch minimum thickness closed cell neoprene or silicone (BOYD R-10480 or equal) and shall be permanently bonded to the metal. If neoprene is used the mating surface of the gasketing shall be covered with a silicone lubricant to prevent sticking to the mating metal surface. A Gasket Top Channel shall be provided to support the top gasket on the door (prevent gasket gravitational fatigue).

6.2.2.7 Cage Bottom Support Mounting Angles

Cage bottom support mounting angles shall be provided on either side, level with the bottom edge of the door opening, for horizontal support and bolt attachment. In addition, side cage supports shall be provided for the upper cage bolt attachments. Spacer brackets between the side cage supports and the cage shall be a minimum thickness of either 0.188 in aluminum or 0.105 in steel.

6.2.2.8 Lifting Eyes

The housing shall be provided with 2 lifting eyes for placing the cabinet on its foundation. Each eye opening shall have a minimum diameter of 0.75 in. Each eye shall be able to support a weight load of 1000 pounds.

6.2.2.9 Exterior Bolt Heads

All exterior bolt heads shall be tamperproof type.

6.2.3 Door Latches & Locks

6.2.3.1 Latching Handles

The latching handles shall have provision for padlocking in the closed position. Each handle shall be 0.75 in minimum diameter stainless steel with a minimum 0.5 in shank. The padlocking attachment shall be placed at 4.0 in from the handle shank center to clear the lock and key. An additional 4.0 in minimum gripping length shall be provided.

6.2.3.2 Latching Mechanism

The latching mechanism shall be a three-point draw roller type. The pushrods shall be turned edgewise at the outward supports and have a cross section of 0.25 in thick by 0.75 in wide, minimum.

6.2.3.3 Locks and Handles

When the door is closed and latched, the door shall be locked. The locks and handles shall be on the right side of the front door and left side of the rear door. The lock and lock support shall be rigidly mounted on the door. In the locked position, the bolt throw shall extend a minimum of 0.25 ± 0.03125 in into the latch Cam area. A seal shall be provided to prevent dust or water entry through the lock opening.

6.2.3.4 Locks

The locks shall be Corbin 2 type, or equal. One key shall be supplied with each lock. The keys shall be removable in the locked position only.

6.2.3.5 Bolts

The locks shall have rectangular, spring-loaded bolts. The bolts shall have a 0.281 in throw and shall be 0.75 in wide by 0.75 in thick (tolerance is ± 0.035 in).

6.2.3.6 Center Latch Cam

The center latch cam shall be fabricated of a minimum thickness 0.1875 in steel or

aluminum. The bolt surface shall horizontally cover the cam thickness. The cam shall be structured to only allow the door to open when the handle is moved toward the center of the door.

6.2.3.7 Rollers

Rollers shall have a minimum diameter of 0.875 in with nylon wheels and steel ball bearings.

6.2.4 Ventilation

The housing ventilation including intake, exhaust, filtration, fan assembly and environmental control are as follows:

6.2.4.1 Front Door

The front door shall be provided with louvered vents. The louvered vent depth shall be a maximum of 0.25 in. A removable and reusable air filter shall be housed behind the door vents. The filter filtration area shall cover the vent opening area. A filter shell shall be provided that fits over the filter providing mechanical support for the filter. The shell shall be louvered to direct the incoming air downward. The shell sides and top shall be bent over a minimum of 0.25 in to house the filter. The filter resident in its shell shall be held firmly in place with a bottom bracket and a spring loaded upper clamp. No incoming air shall bypass the filter. The bottom filter bracket shall be formed into a waterproof sump with drain holes to the outside housing.

6.2.4.2 Intake and Exhaust Areas

The intake (including filter with shell) and exhaust areas shall pass a minimum of 60 cubic feet of air per minute for housing #1 and 26 cubic feet of air per minute for housing #2.

6.2.4.3 Electric Fan

The housing shall be equipped with an electric fan with ball or roller bearings and a capacity of at least 100 cubic feet of free air delivery per minute. The fan shall be mounted within the housing and vented.

6.2.4.4 Temperature Controlling

The fan shall be thermostatically controlled and shall be manually adjustable to turn on between 32 °F and 140 °F with a differential of not more than 20 °F between automatic turn on and off. The fan circuit shall be protected at 125% of the fan motor ampacity. The manual adjustment shall be graded in 20 °F increment scale. **The Thermostat shall be an Omega KT01101141900 or equal.**

6.2.4.5 Filter

The filter shall be 16 in wide by 12 in high by 0.875 in thick. The filter shall be an ECO-AIR Products E35S or equal.

6.2.5 Hinges & Door Catches

6.2.5.1 Leave Hinges

Two-bolt per leave hinges shall be provided to bolt the enclosure to the door. Housing 1 shall have 4 hinges and Housing 2 three hinges. Each hinge shall be 3.5 in minimum length and have a fixed pin. The pin ends shall be welded to the hinge and ground smooth. The pins and bolts shall be covered by the door edge and not accessible when the door is closed.

6.2.5.2 Front and Rear Doors

Front and rear doors shall be provided with catches to hold the door open at both 90 and 180 ±10 degrees. The catch minimum diameter shall be either 0.375 in for plated steel or aluminum rods or 0.25 in for Stainless steel. The catches shall be capable of

holding the door open at 90 degrees in a 60 mph wind acting at an angle perpendicular to the plane of the door.

6.2.6 Police Panel

6.2.6.1 Police Panel Assembly

A police panel assembly shall be provided to allow the police officers limited access to intersection control. The police panel assembly including switches shall not extend into the cabinet more than 1.5 in.

6.2.6.2 Police Panel Door

The police panel door shall be equipped with a lock. The lock shall be keyed for a master police key. One key shall be furnished with each police lock. Each police key shall have a shaft at least 1.75 inches in length.

6.2.6.3 Toggle Power Switches

The police panel shall contain 2 DPST Toggle Power Switches.

6.2.6.3.1 Model 334

One switch shall be labeled "ON-OFF LIGHTS" and the other "POLICE CONTROL ON-OFF".

6.2.6.3.2 Models 332 and 336

One switch shall be labeled "ON-OFF" and the other "FLASH/AUTOMATIC".

6.2.6.3.3 Front and Back of the Panel

The front and back of the panel shall be enclosed with a rigid metal covering so that no parts having line voltage are exposed.

6.2.6.3.4 Panel Assembly

The panel assembly shall have a drain to prevent water collecting within the assembly. The drain shall be channeled to the outside.

CHAPTER 6-SECTION 3 CABINET CAGE REQUIREMENTS

6.3.1 EIA 19-inch Rack Cage

A standard EIA 19-in rack cage shall be installed inside the housing for mounting of the controller unit and cabinet assemblies.

6.3.2 EIA Rack Portion

The EIA rack portion of the cage shall consist of 2 pairs of continuous, adjustable equipment mounting angles. The angle nominal thickness shall be either 0.1345 in plated steel or 0.105 Stainless Steel. The angles shall be tapped with 10-32 threads with EIA universal spacing. The [angle shall comply with Standard EIA RS-310-D and shall be supported at the top and bottom by either welded or bolted support angles](#) to form a cage.

6.3.3 Clearance

Clearance between rails for mounting assemblies shall be 17.75 in.

6.3.4 Angles

Two steel supporting angles extending from the front to the back rails shall be supplied to support the controller unit. The angles shall be designed to support a minimum of 50 pounds each. The horizontal side of each angle shall be a minimum of 3 in. The angles shall be vertically adjustable.

6.3.5 Cage

The cage shall be bolted to the cabinet at 4 points, via the housing cage supports and associated spacer brackets, 2 at the top and 2 at the bottom of the rails.

6.3.6 Cage Position

The cage shall be centered within the cabinet.

CHAPTER 6-SECTION 4 CABINET ASSEMBLIES

6.4.1 General

6.4.1.1 Equipment

The following equipment shall be completely removable from the cabinet without removing any other equipment and using only a slotted or Phillips screwdriver:

- Power Supply Assembly
- Power Distribution Assembly
- Input File
- Output File
- Monitor Unit Assembly

6.4.1.2 Fuses, Circuit Breakers, Switches and Indicators

All fuses, circuit breakers, switches (except Police Panel Switches and Fan Fuse) and indicators shall be readily visible and accessible when the cabinet front door is open.

6.4.1.3 Equipment in the Cabinet

All equipment in the cabinet, when required shall be clearly and permanently labeled. The marker strips shall be made of material that can be easily and legibly written on using a pencil or ballpoint pen. Marker strips shall be located immediately below the item they are to identify and must be clearly visible with the items installed.

6.4.1.4 Resistor-Capacitor Transient Suppression

Resistor-capacitor transient suppression shall be provided at all AC relay sockets (across relay coil) except for the Flash Transfer Relays (FTR) in the output files where one suppression device may be common for all.

6.4.1.5 Leakage Resistor

A leakage resistor, which permits a small amount of current to pass through the heavy duty relay coil, shall be installed across the terminals of a relay socket to overcome the residual magnetism.

6.4.1.6 Assembly

Assembly or file depth dimension shall include terminal blocks.

6.4.1.7 Air Circulation

All assemblies and files shall allow air circulation through its top and bottom unless specifically called out otherwise.

6.4.1.8 Socket Types

Socket types for the following equipment shall be

Switch Pack	BEAU S-5412-XX (or equal)
Heavy Duty Relay	BEAU S-5408-XX (or equal)
Flasher Unit & Power Sup Mod	BEAU S-5406-XX (or equal)
208 Monitor Unit	PCB 22/44S
210 Monitor Unit	PCB 28/56S

6.4.1.9 Mounting

Connector sockets for Flasher Unit, Power Supply, and Switch Pack modules shall be mounted with their front face 7.5 in deep from assembly or file front panel (Note: Output File Exception).

6.4.1.10 Guides

Guides (Top and Bottom) shall be provided for Switch Pack Modules, Flasher Units, Monitor Unit, Watchdog Timer Module, Detector & Isolator Modules, and Power Supply Module (Bottom only). **The guides shall begin 1.0±0.5 inches in from the front panel surface and extend to within 0.5 inches from the connector socket face.**

6.4.1.11 Fabricating

Assemblies and Files shall be fabricated of 0.060 in minimum thickness aluminum or stainless steel sheet. The metal surface shall be treated with clear chromate.

6.4.2 Power Supply Assembly

6.4.2.1 Power Supply

A power supply shall be provided to supply +24 VDC to the Input and Output Files for use by their associated devices. **The power supply shall be compliant with Chapter 3, Section 4 under Model 206L Power Supply Unit of these specifications.**

6.4.3 Power Distribution Assembly (PDA)

6.4.3.1 Equipment

The following equipment shall be provided with the power distribution assemblies:

6.4.3.1.1 PDA #1L

- 1 -- Duplex NEMA 5-15R Controller Receptacle
- 2 -- Duplex NEMA 5-15R Equipment Receptacle (one with GFCI)
- 1 -- 1 Pole 15 Amperes minimum, 120 VAC Clean Power Circuit Breaker
- 1 -- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
- 1 -- 6 Pole Ganged, 10 Amperes, 120 VAC Signal Bus Circuit Breaker
- 1 -- 2 Pole Ganged, 10 Amperes, 120 VAC Flash Bus Circuit Breaker
- 1 -- Solid State Relay (Normally Closed) - rated minimum 50 Amperes, 120 VAC, Crydom A2450-B or equal.
- 2 -- Model 204 Flasher Unit and Socket
- 1 -- AUTO/FLASH Control Switch
- 1 -- FLASH Indicator Light
- 1 -- Model 430 Heavy Duty Relay (Transfer Relay) & Socket
- 2 -- 10 Position Terminal Blocks (TBK) T1 & T2

6.4.3.1.2 PDA #2L

- 1 -- Duplex NEMA 5-15R Controller Receptacle
- 2 -- Duplex NEMA 5-15R Equipment Receptacle (one with GFCI)
- 1 -- 1 Pole 15 Amperes minimum, 120 VAC Signal Bus Circuit Breaker
- 1 -- 1 Pole 15 Amperes minimum, 120 VAC Clean Power Circuit Breaker
- 6 -- 1 Pole Ganged, 10 Amperes, 120 VAC Signal Bus Circuit Breaker with Auxiliary Switch
- 1 -- 1 Pole 15 Amperes, 120 VAC Equipment Circuit Breaker
- 1 -- 2 Pole Ganged, 10 Amperes, 120 VAC Flash Bus Circuit Breaker
- 1 -- Solid State Relay (Normally Closed) - rated minimum 50 Amperes, 120 VAC, A2450-B or equal.
- 2 -- Model 204 Flasher Unit and Socket
- 1 -- Model 206L Power Supply Module and Socket
- 1 -- Model 430 Heavy Duty Relay & Socket (Transfer Relay)
- 1 -- AUTO/FLASH Control Switch
- 1 -- Flash On Indicator Light
- 3 -- 10 Position TBK T1, T2 & T4
- 1 -- 4 Position TBK T3
- 1 -- SSR Fault Indicator Light

6.4.3.1.3 PDA #3L

- 1 -- Duplex NEMA 5-15R Controller Receptacle
- 2 -- Duplex NEMA 5-15R Equipment Receptacle
- 1 -- 1 Pole 15 Amperes, 120 VAC Equip. Circuit Breaker
- 2 -- 1 Pole 10 Amperes, 120 VAC Field Circuit Breakers
- 1 -- 1 Pole 15 Amperes, 120 VAC Clean Power CB
- 1 -- Model 206L Power Supply Module and Socket
- 1 -- Model 208 Monitor Unit and Socket
- 1 -- Model 430 Heavy Duty Relay and Socket
(Transfer Relay)
- 1 -- Watchdog Timer ON/OFF-RESET Control Switch
- 3 -- Model 200 Switch Pack Sockets
- 3 -- 10 Position TBK T1, T2 & T4
- 1 -- 4 Position TBK T3

6.4.3.2 Rating of Breakers

Rating of breakers shall be shown on face of breaker or handle. Breaker function shall be labeled below breakers on front panel.

6.4.3.3 Equipment Receptacle

The first equipment receptacle in the circuit shall have ground-fault circuit interruption as defined in the National Electrical Code. Circuit interruption shall occur on 6 ma of ground-fault current and shall not occur on less than 4 ma of ground-fault current.

6.4.3.4 AUTO/FLASH Switch

The AUTO/FLASH Switch when placed in FLASH position (down) shall energize the Solid State Relay (SSR). When the switch is placed in the AUTO Position (up) the switch packs shall control the signal indications. The switch shall be a SPST Toggle Control Switch.

6.4.3.5 FLASH Indicator Light

The FLASH Indicator Light labeled "Flash On" shall be mounted on the PDA Front Panel. The lamp shall be driven by Flasher Unit/Output through Flash Relay Circuit No. 1 or per Circuit Breaker.

6.4.3.6 SSR Fault Indicator Light

The SSR Fault Indicator Light labeled "SSR Fault" shall be mounted on the PDA Front Panel. The lamp shall be driven by the SSR output when the Health Indicator Relay is energized.

6.4.3.7 Conductors

All conductors from the power distribution assembly routed to the cabinet wiring shall be connected to the terminal block on the common side, except for the AC power conductor between the service terminal block and main circuit breaker. All internal conductors terminating at the blocks shall be connected to the other side of the blocks.

6.4.3.8 Ganged Circuit Breakers

Ganged Circuit Breakers shall be certified by the circuit breaker manufacturer that their circuit breakers shall gang trip.

6.4.3.9 Monitor Unit

The Monitor Unit ON/OFF-RESET Switch shall be a DPST Toggle Control mounted on the PDA #3L's front panel. When placed in DOWN Position (OFF-RESET) a grounded input shall be presented at the Monitor Unit Pin 22 (resetting the WDT Circuitry) and the other side switch circuit closes by passing the Monitor Unit.

6.4.3.10 Circuit Breaker with Auxiliary Switch

6.4.3.9.1 Single Pole

Six Single Pole 10 Ampere Circuit Breakers with Auxiliary Switch Feature and Medium Trip Delay Characteristic shall be provided.

6.4.3.9.2 Breakers

The six breakers shall be wired and routed per the Option One Line Diagram. The breaker auxiliary switch circuit shall be open when the breaker is in ON Position. The auxiliary circuits shall be wired in parallel so that any tripped breaker shall energize the Solid State Relay input, Flash Transfer Relay Coils and the "FLASH ON" Indicator. The Auxiliary Contacts shall be rated at 5 Amperes, 120 VAC Minimum (fast on type connection).

6.4.3.9.3 Terminals

Breaker switches shall be bussed using straight solid non-insulated bus wire which is soldered directly to the "fast-on" terminals.

6.4.3.11 Model 206 Power Supply Module

6.4.3.10.1 Requirements

The module shall meet the requirements specified in 6.4.2.1 and 6.4.2.3.

6.4.3.10.2 Module Chassis

The module chassis shall be vented. Its top and sides shall be open except for unit supports

6.4.3.10.3 PDA Assembly

When resident in the PDA assembly, the module shall be held firmly in place by its stud screw, assembly connector support panel and a wing nut.

6.4.3.10.4 Wire-Wound Power Resistors

Two 0.5 Ohm, 10 watt minimum wire-wound power resistors with a 0.2uH inductance shall be provided (1 on the AC+ power line and 1 on the AC- line). Three MOV surge arrestors rated for 20 Joules minimum shall be supplied between AC+ and EG, AC- and EG, and between AC+ and AC-. A 0.68uF capacitor shall be placed across AC+ and AC- between the two power resistors and the MOV's.

6.4.3.12 Terminal Screw Sizes

Terminal screw size shall be 10-32 for TBK T1, T2 & T4 and 6-32 for TBK T3.

6.4.4 Input File

6.4.4.1 Depth

The file shall have a maximum depth of 8.5 in and shall intermit with and support 14 two-channel detector sensor or isolator units.

6.4.4.2 Connectors

The file shall provide a PCB 22/44S connector centered vertically for each two-channel detector. The associated number and letter side connectors shall be shorted internally. Pins D, E, F, J, K, L and W shall be brought out to a 8 position terminal block on the back of the file. The output emitters shall be common grounded with the ground terminating at TB 15, Position 4. Position 8 of the terminal block is assigned to Equipment Ground and is used to terminate lead in shields.

6.4.4.3 Marker Strips

The input file shall be provided with marker strips to identify isolators and detectors in the file.

6.4.4.4 Screw Size

Terminal Block (TB) terminal screw size shall be 8-32.

6.4.5 Output File

6.4.5.1 General Requirements

6.4.5.1.1 Marker Strips

The Output File shall be provided with marker strips to identify switch packs when mounted in the file.

6.4.5.1.2 Connectors

Switch pack connectors, monitor unit connectors, flash transfer relay sockets and flash programming connectors shall be accessible from the back of the Output File without the use of tools or removal of any other equipment.

6.4.5.1.3 Terminal Positions

TBK O1 and O3 terminal positions shall be labeled functionally. A permanent label reading "Channels 9 & 10 Separated" placed on the right Output File mounting flange.

6.4.5.1.4 Field Wire

Field wire terminal blocks shall be mounted vertically on the back of the assembly. Output File #1 shall have 3 terminal blocks with 12 positions and Output File #2 shall have 3 terminal blocks with 6 positions. Terminal position screw size shall be 10-32.

6.4.5.1.5 Flash Transfer Relays

The Flash Transfer Relays shall be Heavy Duty Type. The coil of the relay shall be energized only when the signals are in flashing operation and the police panel ON/OFF switch is ON. The relay shall transfer the field outputs from switch pack output to flash control. The transfer shall not interrupt the controller unit operation.

6.4.5.1.6 Depth

The depth of the file shall not exceed 14.5 in.

6.4.5.1.7 Flash Programming Connectors

The flash programming connectors shall be Molex Type 1375 or equal. The receptacle shall be mounted on the file with a programmable plug connected. The plug connector, with programming jumpers, shall be furnished for each circuit to allow red or yellow flash programming. Plug pins shall be crimped and soldered.

6.4.5.1.8 TB O1,O2,O3& O4 Terminal Screw Sizes

Terminal Block (TB) O1 and O3 terminal screw size shall be 8-32 and TBK O2 & O4 shall be 6-32.

6.4.5.2 Output File #1

6.4.5.2.1 Containing

The output file shall be capable of containing 12 Model 200 Switch Packs, 4 Flash Transfer Relays, and the Model 210 Monitor Unit. Four Flash Transfer Relays and 1 Model 210 Monitor Unit shall be furnished with each output file.

6.4.5.2.2 Output Circuits

The red and yellow output circuits of switch packs 1, 2, 3, 4, 5, 6, 7 and 8 shall be made available at individual pack Molex receptacle /plug connection for flash selectability. Eight red & 4 yellow Molex Plugs shall be provided.

6.4.5.2.3 Model 210 Monitor Unit

It shall be possible to remove the Model 210 Monitor Unit without causing the intersection to go into flashing operation. The cabinet shall be wired so that with the front cabinet door closed and with the monitor unit removed, the intersection shall go into flashing operation (See One Line Diagram). The cabinet shall contain a conspicuous warning against operation with the Model 210 Monitor Unit removed.

6.4.5.2.4 Monitor Unit Compartment

The monitor unit compartment including the housed Model 210 Monitor Unit exclusive of handle shall extend no farther than 1.25 in front of the 19-in rack front surface. The switch pack socket connector front surface shall be no more than 8.5 inches in depth from the front surface of the output file.

6.4.5.3 Output File #2 (Model 420)

6.4.5.3.1 Switch Packs and Flash Transfer Relays

The Output File #2 shall be capable of containing 6 Model 200 Switch Packs and 2 Flash Transfer Relays. Two Flash Transfer Relays shall be provided with the file.

6.4.5.3.2 Output Circuits

The red and yellow output circuits of Switch Packs No. 1, 2, 4 and 5 shall be made available at a Molex receptacle/plug connection for flash select ability.

6.4.6 Heavy Duty Relay (Model 430)

6.4.6.1 Electromechanical Type

Heavy duty relays shall be the electromechanical type designed for continuous duty.

6.4.6.2 Enclosing

Each relay shall be enclosed in a removable, clear plastic cover. The manufacturer's name, electrical rating and part number shall be placed on the cover. They shall be permanent, durable and readily visible.

6.4.6.3 DPDT Contacts

Each relay shall be provided with DPDT contacts. Contact points shall be of fine silver, silver alloy or superior alternative material. Contact points and arms shall be capable of switching a 20 Amperes at 120 VAC tungsten load per contact once every 2 seconds with a 50% duty cycle for at least 250,000 operations without contact welding or excessive burning, pitting or cavitation.

6.4.6.4 Relay Coil

The relay coil shall have a power consumption of 10 Volt-Amperes maximum.

6.4.6.5 Potential & Surge Rating

Each relay shall withstand a potential of 1500 VAC at 60 Hz between insulated parts and between current carrying or non-carrying parts. Each relay shall have a 1 cycle surge rating of 175 Amperes RMS.

6.4.7 Side Panels

6.4.7.1 Viewing

Two panels shall be provided and mounted on the cage parallel to the cabinet sides. In viewing from the back door, the left side panel shall be designated as the "Input Panel" and the right side panel shall be designated as the "Service Panel".

6.4.8 Cabinet Harnesses

6.4.8.1 C1 Harness

The C1 Harness shall be a minimum of 4 ft in length. The harness wire bundle shall be provided with external protection and routed on the Input Panel Side of the cabinet. Adequate length shall be provided to allow the C1P Connector to properly connect any State Approved Model 170 Controller Unit mounted in the cabinet.

6.4.8.2 Ends

One end of the C1 Harness shall be the C1P Connector with pin contacts wired per the detail assignment. The other ends of the harnesses shall terminate as follows:

Harness #1 - C4S Connector (connected to C4P on Output File #1)

C5S Connector (connected to C5P on either the Input Panel or Output File #2)

Assigned Input Files I & J Positions and Logic Ground Bus

Harness #2 - C5S Connector (same as Harness #1)

C6S Connector (connected to C6P on Output/PDA Assembly)
Assigned Input File I Positions and Logic Ground Bus

Harness #3 - C4S Connector (same as Harness #1)
Assigned Input File I Positions
Input Panel Terminal Block and Logic Ground Bus

6.4.8.3 C1 Harness #3/Output File #2 Adaptor

C1 Harness #3/Output File #2 Adaptor shall be comprised of a C4P Connector on one end and a C5S on the other. The adaptor shall interface the first 24 pins of C4 Connector to the 24 pins of C5.

6.4.8.4 Conductors

Conductors between the C1 Connector and the Input File(s) shall be of adequate length to allow any conductor to be connected to any detector output terminal (Positions S, F, or W).

CHAPTER 6-SECTION 5 CABINET WIRING

6.5.1 Cabinet Wiring Diagram

6.5.1.1 Diagrams/Drawings Supply

Four sets of nonfading (comparable to Xerox 2080) cabinet wiring diagram and drawing sheets shall be supplied with each cabinet. The diagrams shall be nonproprietary. They shall identify all circuits in such a manner as to be readily interpreted. The cabinet drawing sheets shall show the equipment layout in an elevation view as viewed from the rear of the cabinet with the left and right cabinet walls shown in their relative positions.

The diagram and drawing sheets shall be placed in a heavy duty side opening clear plastic pouch and attached to the front cabinet door.

6.5.1.2 Pouch

A pouch that would hold the Cabinet Manuals, Cabinet Wiring and Drawing Sheets, and Cabinet Keys shall be provided as part of the Cabinet.

The pouch shall be of such design and material that it provides adequate storage and access to the wiring diagram sheets and cabinet manuals. The pouch shall be of size and strength to easily hold the documents and keys without tearing.

6.5.1.3 Manuals

Two cabinet manuals shall be provided in the pouch together with the wiring diagram and drawing sheets.

6.5.2 Conductors

6.5.2.1 General

All conductors used in cabinet wiring shall terminate with properly sized non-insulated (if used, for DC Logic Only) or clear insulated spring-spade type terminals except when soldered to a through-panel solder lug on the rear side of the terminal block or as specified otherwise. All crimp-style connectors shall be applied with a power tool which prevents opening of the handles until the crimp is completed.

6.5.2.2 Sizes

Conductors between the service terminal AC- and Equipment Ground and their associated bus, the equipment ground bus conductor to Power Distribution Assembly and cage rail, AC- Bus to Power Distribution Assembly shall be No. 8 or larger.

6.5.2.3 Types

All conductors unless otherwise specified shall be No. 22, or larger, with a minimum of 19 copper strands. Conductors shall conform to Military Specification: MIL-W-16878D, Type B, or better. The insulation shall have a minimum thickness of 10 mils and shall be nylon jacketed polyvinyl chloride except that Conductors No. 14 and larger may have Type THHN insulation (without Nylon Jacket), and shall be stranded with a minimum of 7 copper strands.

6.5.2.4 Labels

All conductors, except those which can be readily traced, shall be labeled. Labels attached to each end of the conductor shall identify the destination of the other end of the conductor.

6.5.2.5 Color-Code Requirements

All conductors shall conform to the following color-code requirements:

6.5.2.5.1 Grounded Conductors

The grounded conductors of AC circuits shall be identified by a solid white or solid gray color.

6.5.2.5.2 Equipment Grounding

The equipment grounding conductors shall be identified by a solid green color or by a continuous green color with 1 or more yellow stripes.

6.5.2.5.3 DC Logic Ground

The DC logic ground conductors shall be identified by a continuous white color with a red stripe.

6.5.2.5.4 Ungrounded AC+ Conductors

The ungrounded AC+ conductors shall be identified by a solid black or continuous black with colored stripe.

6.5.2.5.5 Logic Ungrounded Conductors

The logic ungrounded conductors shall be identified by any color not specified above.

6.5.2.6 DC Logic Ground and Equipment Ground

Within the cabinet, the DC logic ground and equipment ground shall be electrically isolated from the AC grounded conductor and each other by 500 Mega Ohms when tested at 250 VDC.

6.5.2.7 AC- Copper Terminal Bus

The AC- copper terminal bus shall not be grounded to the cabinet or connected to logic ground. Nylon screws with a minimum diameter of 0.25 in shall be used for securing the bus to the service panel.

6.5.2.8 Power Supply DC Ground

The cabinet power supply DC Ground shall be connected to the DC logic ground bus using a No. 14, or larger, stranded copper wire.

6.5.2.9 Input Terminal

Each detector lead-in pair, from the field terminals in the cabinet to the sensor unit rack connector, shall be a cable of UL Type 2092 or better. The stranded tinned copper drain wire shall be connected to a terminal on the input file terminal block. This input terminal shall be connected to the equipment grounding bus through a single conductor.

6.5.3 Terminal Blocks

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6.5.3.1 Terminal Screws

The terminal blocks shall be barrier type rated at 20 Amperes, 600 volts RMS minimum. The terminal screws shall be 0.3125 in minimum length nickel plated brass binder head type with screw inserts of same material. Screw size is called out under associated cabinet assembly, file or side panel.

CHAPTER 6-SECTION 6 SERVICE PANEL ASSEMBLY

6.6.1 General Requirements

A Service Panel Assembly shall be provided. The assembly shall function as the entry point for AC Power to the cabinet including main and secondary circuit breakers, cabinet transient and voltage surge protection, clean power filtering, and Raw and Clean AC Power Sources.

6.6.2 Location

The assembly shall be located on the lower right Cage when viewed from the back door.

6.6.3 Service Terminal Block

The terminals of the Block shall be labeled AC+, AC-, AC+ In , AC+ Out and EQ GND and shall be covered with a clear insulating material to prevent inadvertent contact. The Terminating Lugs shall be large enough to accommodate # 2 conductors. A AWG #8 Jumper Conductor shall be provided between AC+ In and AC+ Out.

6.6.4 Surge Protector

The surge protector shall be the EDCO Model SHA-1250 or equal.

6.6.4.1 Impulse Breakdown

Less than 1,000 volts in less than 0.1 us at 10 kilovolts/us.

6.6.4.2 Standby Current

Less than 1 mA.

6.6.4.3 Striking Voltage

Greater than 212 VDC.

6.6.4.4 Ranges

Capable of withstanding 15 pulses of peak current each of which will rise in 8 us and fall in 20 us to 0.5 of the peak voltage at 3-minute intervals. Peak current rating shall be 20,000 Amperes.

CHAPTER 6-SECTION 7
332L, 334L, & 336L CABINET DETAILS

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CHAPTER 7
REFER TO ITS CABINET STANDARD

CHAPTER 8
REFER TO CHANGEABLE MESSAGE
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CHAPTER 9
MODEL 2070 CONTROLLER
SPECIFICATIONS

CHAPTER 9-SECTION 1 GENERAL

9.1.1 Controller Unit

The Controller Unit shall be composed of the Unit Chassis, modules and assemblies per their version. The following is a list of 2070 Versions, their interface rolls and composition:

UNIT VERSION	DESCRIPTION
2070V UNIT	Provides directly driven VME and mates to 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1A TB, 2070-1A MCB, 2070-2A FI/O, 2070-3A FRONT PANEL, 2070-4 POWER SUPPLY, and 2070-5 VME CAGE ASSEMBLY.
2070L UNIT	LITE Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY
2070LC UNIT	LITE unit mates to ITS cabinets only. It consists of: UNIT CHASSIS, 2070-1E CPU, 2070-2B FI/O, 2070-3C FRONT PANEL and 2070-4 POWER SUPPLY
2070LX UNIT	LX Unit mates to the 170 & ITS cabinets. It consists of: UNIT CHASSIS, 2070-1C CPU, 2070-2A (2B if ITS CABINET), FI/O, 2070-3B FRONT PANEL and 2070- 4 POWER SUPPLY
Note: See Chapter 11 for 2070 NEMA Versions	

9.1.2 Communications and Option Modules

The communications and option modules shall be called out separately from the unit version. The composition weight shall not exceed 25 lbs.

9.1.3 Chassis

The Chassis top and Bottom, Internal Structure Supports, Back Plane Mounting Surface, Module Plates, Power Supply Enclosure, and Front Panel shall be made of minimum aluminum sheet. The Chassis Side panels shall be 0.090 inches minimum sheet

9.1.4 Power Failure Power Restoration Operations

It is noted that the Power Failure Power Restoration operations of this unit are specific to the requirements of the user. All associated modules shall comply to said operations.

9.1.5 2070 Unit Module

2070 UNIT module / assembly power limitations shall be as follows:

Models	+5VDC	+12VDC iso	+12VDC ser	-12 VDC ser
2070-1A MCB	750 mA	-----	-----	-----
2070-1A TB	750 mA	-----	-----	-----
2070-1E CPU	1.0 A	250 mA		
2070-1C, Host Board	2A	250mA		
2070-2A FI/O	250 mA	750 mA	-----	-----
2070-2B FI/O	250 mA	500 mA	-----	-----
2070-3A,B&D FPA	500 mA	-----	50 mA	50 mA
2070-3C FPA	500 mA	-----	50 mA	50 mA
2070-5 VME Cage	5.0 A	-----	200 mA	200 mA
2070-6A & Others	900mA	-----	300 mA	300 mA
2070-7 All Comm	250 mA	-----	50 mA	50 mA
.				

9.1.6 EIA-485 Communications Links

All circuitry associated with the EIA-485 Communications links shall be capable of reliably passing a minimum of 1.0 Mbps. Isolation circuitry shall be by optical isolator technologies.

9.1.7 EIA-485 Line Drivers/Receivers

The EIA-485 Line Drivers/Receivers shall be socket mounted or Surface mounted and shall not draw more than 35 mA in active state and 20 mA in inactive state. A 100-Ohm Termination Resistor shall be provided across each Differential Line Receiver Input. The MOTHERBOARD's control signals (e.g., SP1-RTS) shall be active, or asserted, when the positive terminal (e.g., SP1-RTS+) is a lower voltage than its corresponding negative terminal (e.g., SP1-RTS-). A control signal is inactive when its positive terminal voltage is higher than its negative terminal. Receive and transmit data signals shall be read as a "1" when the positive terminal's (e.g., SP1-TXD+) voltage is higher than its corresponding negative terminal (e.g., SP1-TXD-). A data value is "0" when its positive terminal's (e.g., SP1-TXD+) voltage is lower than its negative terminal (e.g., SP1-TXD-).

9.1.8 Sockets

Sockets for devices (called out to be socket mounted) shall be "xx" pin AUGAT 500/800 series AG10DPC or equal.

9.1.9 Frame Address

SP5 and SP3 SDLC frame address assignments (Command/Response) are as follows:

	SP 5	SP3
CPU 2070-1	"19"	"19"
FI/O 2070-2A	"20"	"NA"
Manufacturer Use	128 -254	128-254
CPU Broadcast to all	"255"	"255"

All other addresses are reserved or assigned by the Agency with the exception of NEMA TS2 Type 1 Requirements (See Chapter 11). The SDLC response shall contain the frame address of the Command sender.

CHAPTER 9-SECTION 2 MODEL 2070-1 CPU MODULE

9.2.1 Model 2070-1A CPU Module

The Model 2070-1A CPU Module shall consist of the Main Controller Board, Transition Board, Board Interface Harness, and CPU Module Software.

9.2.1.1 Main Controller Board (MCB)

The MCB shall be a 3U VME bus compliant board and contain a system controller, an A24-D16 interface, a Master & Slave bus interface, a Multilevel VMEbus Arbiter, a FAIR VMEbus Requester and BTO (64)

9.2.1.2 Controller

The Controller Device shall be a Motorola MC68360 or equal, clocked at 24.576 MHz minimum. The Fast IRQ Service System is reserved for State use only. The Interrupts shall be configured as follows:

Level 7 - VMEbus IRQ7	
Level 6 - VMEbus IRQ6	ACFAIL
Level 5 - VMEbus IRQ5	CPU: Module Counters Timers, LINESYNC (auto vectored), Serial Interface Interrupts
Level 4 - VMEbus IRQ4	
Level 3 - VMEbus IRQ3	
Level 2 - VMEbus IRQ2	
Level 1 - VMEbus IRQ1	

9.2.1.3 Memory Address Organization

8000 0000	80FF FFFF	STANDARD
9000 0000	9000 FFFF	SHORT

9.2.1.4 Transition Board

A Transition Board (TB) shall be provided to transfer serial communication and control signals between the MCB and the Interface Motherboard. Said signal and communication lines shall be driven/received off and on the module compliant to EIA-485. The Transition Board shall provide a 1 K-Ohm pull-up resistor for the A2 & A3 Installed lines. If the DC Ground is not present (slot not occupied) at the CPU EIA-485 line drivers/receivers, the drivers/receivers shall be disabled (inactive).

9.2.1.5 Shielded Interface Harness

A Shielded Interface Harness shall be provided. It shall include MCB and Transition Board connectors with strain relief, lock latch, mating connectors, and harness conductors. A minimum of 25 mm (0.984 in) of slack shall be provided. No power shall be routed through the harness. The harness shall be 100% covered by an aluminum Mylar foil and an extruded black 0.8 mm (0.0315 in) PVC jacket or equal.

9.2.2 Model 2070-1E CPU Module

The **Model 2070-1E** CPU Module shall be a single board module meeting the 2X WIDE Board requirements. The module shall be furnished normally resident in the Motherboard Slot A5. The module shall meet all the requirements listed under this section and Chapter Details Section 7. **The Model 2070-1E Module shall have a Motorola MC68EN360 CPU or equal, clocked at 24.576 MHz minimum.**

9.2.2.1 Dual SCC Device

A Dual SCC Device (asynch / synch) and associated circuitry shall be furnished to provide two additional system serial ports. The Dual SCC1 shall be assigned to the System Serial Port SP1 meeting all requirements called out for SP1 except where noted. The Dual SCC2 shall be assigned as System Serial Port SP8. The SP8 and associated circuitry shall interface with the MC68EN360 address and data structure and serially be connected to the external world via the DB 25 Pin C13S Connector located on the module front panel. **The SP8 shall meet all SP2 Port requirements except where noted, including EIA 485 drivers / receivers and synchronous data rate of 614.4 Kbps.**

9.2.2.2 68EN360 SCC1

The 68EN360 SCC1 shall be reassigned to Ethernet (ENET) Network meeting Ethernet **10 Mbps IEEE 802.3 (TP) 10 BASE T Standard Requirements, both hardware and software.** **The CPU network lines shall be connected to a port on the Network Switch. Four LEDs labeled "10/100 and Link/Act" shall be mounted on the front panel signifying Ethernet operational conditions between the CPU and the Network Switch.**

9.2.2.3 Module 2070 -1E Power Requirements.

The 2070-1E CPU Module shall not draw more than 1.00 A of +5VDC & 250 mA of ISO+12 VDC.

9.2.2.4 The C13S Connector

The C13S Connector shall be a DB25S connector and shall be located on the Module 2070 -1X CPU front panel and shall contain signals for SP8, LINESYNC, NRESET, POWERDOWN, and an isolated BIAS +5VDC as specified in the following subsections and as listed in A9-7. **TX and RX LEDs shall be provided as show in A9-7.**

9.2.2.4.1 Serial Port SP8

System Serial Port 8 (SP8) shall be isolated, converted to EIA-485, and then routed to Connector C13S. SP8 shall meet all SP2 Port requirements except where noted.

9.2.2.4.2 LINESYNC and POWERDOWN

LINESYNC and POWERDOWN lines shall each be isolated, converted to EIA-485, and then routed to connector C13S for external module use.

9.2.2.4.3 NRESET

CPU_Reset and POWER UP lines shall be isolated, then OR'd to form NRESET. NRESET shall then be converted to EIA-485 and routed to connector C13S for external module use.

9.2.3 Model 2070-1C CPU Module

The TYPE 2070-1C CPU Module shall be a single board module meeting the 2X WIDE board requirements. The module shall be furnished normally resident in MOTHERBOARD Slot A5. The module shall meet the requirements as listed in Section 9.2.2.4 of these specifications.

9.2.3.1 Engine Board

The TYPE 2070-1C CPU shall use an Engine Board compliant to the AASHTO/ITE/NEMA Next Generation ATC Standard with the exceptions as defined in Sections 9.2.5 and 9.2.8. The Engine Board shall be used for execution of the application software. No other microprocessor or memory of the 2070-1C CPU shall be used for execution of the application software.

9.2.3.2 Ethernet Ports

The ETHERNET ports of the Engine Board shall be brought out on RJ 45 Connectors mounted on the 2070-1C front panel. The front panel LED indicators for the two CPU Ethernet ports shall be provided as indicated in drawing A9-15.

9.2.3.3 Network Switches, Module 2070-1C

The Model 2070-1C CPU Module shall be provided with two integrated Store-and-Forward Network Switches per the IEEE 802.3, 802.3u and 802.3 x specifications. One switch shall be configured with port 1 and 2 connected to the front panel RJ-45 connectors and port 3 shall be connected to the CPU ENET 1 port. The second switch shall be configured with port 1 connected to the front panel RJ-45, port 2 shall be connected to the CPU ENET 2 port. Port 3 shall be used to route Ethernet across the Motherboard to the "A" Connectors. DC Grounding plane around the network connectors and lines shall be provided. Port 3 Network Lines shall be assigned to: NetP5 TX+, TX-, RX+ and RX- respectively.

9.2.3.4 Universal Serial Bus (USB)

The TYPE 2070-1C CPU Module shall include a USB port compliant to the AASHTO/ITE Next Generation ATC Standard with the exceptions that USB shall conform to the appropriate sections of the USB v2.0 specification for both hardware and software operations. USB shall be brought out from the Engine Board to a USB Connector mounted on the 2070-1C front panel.

9.2.3.5 Host Module

The 2070-1C CPU Module shall use a Host Module that provides the mechanical and electrical interfaces to the Engine Board and Motherboard.

The TYPE 2070-1C CPU Module shall implement the host module identification using the Engine Board SPI serial port, compliant to the AASHTO/ITE Next Generation ATC Standard.

9.2.4 Model 2070-1A and 2070-1E CPU Module

9.2.4.1 Contiguous Addresses

16 megabytes of contiguous address space for each specified memory (DRAM, SRAM and FLASH) shall be allocated on an even boundary. The SRAM and FLASH memories shall be accessed through the OS-9 Operating System's Supplied File Manager.

9.2.4.2 **Incoming +5 VDC**

When the incoming +5 VDC falls below its operating level, the SRAM shall drop to its standby state and the SRAM and TOD Clock shall shift to the +5 VDC Standby Power. A on-board circuit shall sense the +5 VDC Standby Power and shift to a On-board CPU Power Source. When the incoming +5 VDC rises to within its operating level, the appropriate MCB Circuitry shall shift from standby power to incoming +5 VDC.

9.2.4.3 **Ram Memory**

A minimum of 8 MB of DRAM memory, organized in 32-bit words, shall be provided. A minimum of 512 KB of SRAM will be available for agency use, organized in 16 or 32-bit words shall be provided. The time from the presentation of valid RAM address, select lines, and data lines to the RAM device to the acceptance of data by the RAM device shall not exceed 80 ns and shall be less as required to fulfill zero wait state RAM device write access under all operational conditions.

9.2.4.4 **Flash Memory**

A minimum of 8 MB of FLASH memory, organized in 16- or 32- bit words, shall be provided. The MCB shall be equipped with all necessary circuitry for writing to the FLASH memory under program control. No more than 2 MB of FLASH Memory shall be used for the Boot Image and a minimum of 6 MB shall be available for Agency use. A maximum of 2 MB of Flash Memory shall be reserved the Boot Image only. Flash memory shall have a minimum rated capacity of 100,000 read/write cycles and be industrial grade or better.”

9.2.4.5 **Time-of-day Clock**

A software settable hardware Time-of-Day (TOD) clock shall be provided. It shall, under on-board standby power maintain an accuracy of ± 1 minute per 30 days at 25°C. The clock shall provide a minimum fractional second resolution of 10 ms and shall track seconds, minutes, and hours, day of month, month, and year.

9.2.4.6 **CPU_Reset**

A software-driven CPU_Reset signal (Active LOW) shall be provided to reset other controller systems. The signal output shall be a driver capable of sinking 30 mA at 30 VDC. Execution of the program module “cpureset” in the boot image shall assert the CPU_Reset signal once. CPU_Reset shall be executed when the controller starts up or is rebooted using the OS-9 break command.

9.2.4.7 **CPU_ACTIVE LED Indicator**

An open-collector output, capable of sinking 30 mA at 30 VDC, shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED Indicator. The LED shall default to ON when the controller starts up.

9.2.4.8 **Tick Timer**

The OS-9 Operating System Tick Timer interrupt shall be derived from the each transition of LINESYNC signal, with a tick rate of 120 ticks per second.

9.2.4.9 SRAM and TOD Clock

The SRAM and TOD Clock Circuitry under Standby mode shall draw no more than 8uA at 2.5 VDC and 35 degrees C. An On board Capacitor supply shall hold up SRAM and TOD for a minimum of 7 days.

9.2.4.10 Network Switch, Model 2070 -1E

The Model 2070-1E CPU Module shall be provided with an integrated Store-and-Forward Network Switch per the IEEE 802.3, 802.3u and 802.3 x specifications. The switch shall be configured with two ports connected to the front panel RJ-45 connectors (C14S) and a third port shall be connected to the CPU. A fourth Port on the Network Switch shall be used to route Ethernet across the Motherboard to the "A" Connector's Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively.

9.2.5 Model 2070-1C CPU Engine Board

9.2.5.1 Model 2070-1C CPU Module Processor

The Model 2070-1C CPU Module Processor shall utilize a Freescale series MPC 82xx / 83xx with a minimum MIPS of 400 calculated using the Dhrystone v2.1 benchmark at 25°C.

9.2.5.2 Ram Memory (DRAM)

The Model 2070-1C CPU Module shall contain a minimum of 64Mbytes of DRAM or equivalent volatile memory for application and OS program execution.

9.2.5.3 Flash Memory

The Model 2070-1C CPU Module shall contain a minimum of 32Mbytes of FLASH for storage of OS Software and user application.

9.2.5.4 Static Memory (SRAM)

The Model 2070-1C CPU Module shall contain a minimum of 1MB minimum of SRAM memory for non-volatile parameter storage.

9.2.5.5 Standby Power

The Model 2070-1C CPU Module Engine Board shall provide the Standby Power required for supporting the SRAM and RTC.

9.2.5.6 Real-Time Clock (RTC)

The Model 2070 -1C Module shall be provided with a software settable, hardware RTC that meets the requirements of the ASHTO/ITE/NEMA ATC Standard except that in the absence of VPRIMARY, the RTC shall operate from VSTANDBY as listed

in A9-16 of these specifications. Also Operating System Time shall be maintained by utilizing the RTC and LINESYNC as defined in Section 9.5.5.3.

9.2.5.7 CPU_Reset

A software-driven CPU_Reset Signal (Active Low) shall be provided to reset other system devices and shall be accessible by application programs as well as by the command line as “cpureset”. CPU_Reset shall be executed when the Controller starts up or is rebooted using the reboot command.

9.2.5.8 CPU_ACTIVE

An Active Low signal shall be provided to drive the Front Panel Assembly CPU_ACTIVE LED indicator. This signal shall cause to the LED to default to ON when the controller starts up.

9.2.5.9 Application Program Interface (API)

The Model 2070-1C Module shall be fully compliant and shall be provided, upon request, with an installed copy of the Application Program Interface (API) compliant to the latest ASHTO/ITE ATC API Standard.

9.2.5.10 Integrated Security

The Model 2070-1C Module shall be implemented with integrated security support for DES, 3DES, MD-5, SHA-1, AES and ARC-4 encryption algorithms as well as a public key accelerator and an on-chip random number generator.

9.2.5.11 SD Card Support

The Model 2070-1C Module shall support SD Card Memory and shall be provided with an industry standard SD Card socket.

9.2.6 Data Key

A Datakey Keyceptacle™ (KC4210, KC4210PCB or equal) shall be mounted on the CPU module front panel (or the Transition Board of MODEL 1A). Power shall not be applied to the receptacle if the key is not present.

The contractor shall supply a 8Mb Memory Size Datakey (SFK8Mb or equal) with each MODEL 1A TB (Transition Board) or 1E and 1C CPU module unless specified otherwise. The Datakey shall be temperature rated for –40 °C to +85 °C (–40°F to 185 °F) operation, shall be blue in color, and shall be initialized to the format and default values defined below. External capability to program the CPU Datakey shall be provided by the contractor.

When programmed, the memory on the key of header shall be organized as follows:

Bytes	Description	Default Values
1-2	16 bit Frame Check Sequence (FCS) calculated as defined in clause 4.6.2 of ISO/IEC 3309. This FCS is calculated across bytes 3-64	
3	Key Type	See table below
4	Header Version	2

5-8	Latitude	0.0
9-12	Longitude	0.0
13-14	Controller ID	0xFFFF
15-16	Communication drop number	0xFFFF
17-20	IP Address	10.20.70.51
21-24	Subnet Mask	255.255.255.0
25-28	Default Gateway	10.20.70.254
29	Startup Override	0xFF
30-64	Reserved for Agency use	All bytes set to 0xFF
65 to End	User Data	All bytes set to 0xFF

When programmed, Byte 3 of the header shall contain the Key Type value as defined in the following table:

Key Type	Model No.	Memory Size	Sector Size	Part Number
1.	DK1000	1Kb	2 Byte	611-0006-002A
2.	LCK16000	16Kb	2 Byte	611-0070-008A
3.	SFK2Mb	2Mb	64KBytes	611-0089-004A
4.	SFK4Mb	4Mb	64KBytes	611-0104-002A
5.	SFK8Mb	8Mb	64KBytes	611-0132-006A
6.	SFK32Mb	32Mb	64KBytes	611-0164-005A

The data format in the CPU Datakey header for the Latitude and Longitude fields shall comply with IEEE/ANSI 754-1985 STD. All the other fields shall follow a Big Endian Format as implemented by Motorola CPUs.

The Startup Override byte, not the Key Type, may be used to override the default controller startup procedure, as described in section 9.2.7.3.3.

9.2.7 Model –1A and 2070-1E CPU Module Software

The following shall be supplied:

1. Operating System
2. Drivers and Descriptors
3. Application Kernel
4. Deliverables
5. Error Handler

9.2.7.1 Operating System

The CPU Module shall be supplied with Microware Embedded OS-9 Release 1.3 or later with kernel edition #376 or later. The following modules shall be included:

- 1 Embedded OS-9 Real Time Kernel
- 2 Sequential Character File Manager (SCF)
- 3 Stacked Protocol File Manager (SPF)
- 4 Pipe File Manager (PIPEMAN)
- 5 Random Block File Manager (RBF)
- 6 C Shared Library (CSL)

Boot Image shall include the following utility modules:

Break	Date	Deiniz	Devs	Free	Copy
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Dir	Tmode	Edt	List	Load	Deldir
Dump	Del	Ident	Iniz	Irqs	Events
Echo	Format	Dcheck	Login	Link	Kermit
Tsmon	Mdir	Mfree	Pd	Makdir	Save
Attr	Rename	Procs	Unlink	Sleep	Xmode
Shell	Build	Setime	Merge	Grep	
Tee	Printenv				

The Boot Image with the above utilities and including the network driver and descriptor shall be loaded into RAM as part of OS-9 initialization as defined in Section 9.2.7.3.2.

9.2.7.2 Drivers and Descriptors

9.2.7.2.1 Supplied Modules

Supplied modules shall be re-entrant, address independent, and shall not contain self-modifying code.

Device drivers which require extensions to the standard Microware libraries shall use the `_os_getstat()` and `_os_setstat()` functions.

A custom setstat code and parameter structure are defined as follows:

```
#define SS_2070    0x2070

error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);
error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);

typedef struct
{
    u_int32 code;
    u_int32 param1;

    union
    {
        u_int32 param;
        void *pointer;
    } param2;
} PB2070, *pb;
```

The following subcodes for use with PB2070.code are also defined:

```
#define GS2070_Status    0x1C
#define SS2070_SSig      0x1A
#define SS2070_IFC       0x22
#define SS2070_OFc       0x23
#define SS2070_Timer_Null 0x0000    (Default State)
#define SS2070_Timer_Sig  0x1000
#define SS2070_Timer_Cyc  0x1001
#define SS2070_Timer_Start 0x1002
#define SS2070_Timer_Stop  0x1003
#define SS2070_Timer_Reset 0x1004
```

Note: When PB2070.param2.pointer is used, PB2070.param1 should be loaded with the size of what PB2070.param2.pointer is referencing. When calling `_os_getstat()` or `_os_setstat()`, all reserved or unused parameters and fields in PB2070 should be loaded with 0 (zero).

9.2.7.2.2 Memory Drivers

Drivers shall be provided to access the FLASH, SRAM, and DRAM memories. The following descriptors shall apply:

/f0	FLASH drive	non-volatile, writeable
/dd	FLASH drive	OS-9 default device for /f0
/f0wp	FLASH Drive	as /f0 except write protected
/f0fmt	FLASH Drive	as /f0 except format enabled
/r0	SRAM Drive	non-volatile ramdisk
/r0fmt	SRAM Drive	as /r0 except format enabled
/r2	DRAM Drive	volatile 2 MB ramdisk, not automatically initialized

9.2.7.2.3 MC68360 Internal Timers

A driver to handle each of the four internal timers under the OS-9 Kernel shall be provided. **Timer resolution shall be one count equals 100 μ S and all timer periods shall be specified in units of hundreds of microseconds (μ S), i.e. a timer period of 7 = 700 μ S. The minimum allowed timer period shall be 500 μ S. The Maximum Timer Period for timers 1-4 shall be 6.5535 seconds (0xFFFF). The Maximum Timer Period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF). The driver shall return error E\$Param from `os_setstat()` if the requested timer period is outside the allowable range.**

A signal of "0" shall be an invalid signal and the driver shall return an E\$PARAM error if received.

Access to the MC68360 internal timers shall be through the following descriptors:

The timers should be set to SS2070_Timer_Null Mode upon initialization.

9.2.7.2.3.1 Descriptor

Descriptor names for each timer:

timer1	= access to MC68360's internal timer #1
timer2	= access to MC68360's internal timer #2
timer3	= access to MC68360's internal timer #3
timer4	= access to MC68360's internal timer #4
timer12	= access to MC68360's internal timer #1 & #2 [cascaded]
timer34	= access to MC68360's internal timer #3 & #4 [cascaded]

9.2.7.2.3.2 Timer Standard

Timer Standard OS-9 Function Calls:

```
error_code _os_open (char *timer_desc_name, path_id *path);
```

```
error_code _os_read (path_id path, void *timer_value, u_int32 *size);
```

Note: Prior to calling `_os_read()`, size must be loaded with the value 4 and timer value must be pointed to a `u_int32`. `_os_read()` shall read the current timer value and load it into `timer_value` as μ S x 100.

```
error_code _os_close (path_id path);
```

9.2.7.2.3.3 Time Extension

Timer Extension to Standard OS-9 Function Calls:

The timer drivers shall support the following modes using the following function with the SS_2070 option code and a custom parameter block structure:

```
error_code _os_setstat(path_id path, SS_2070, PB2070 *pb);
```

- a. Send signal after specified time interval. Sets timer to zero and schedules individual one-shot signal. After one-shot signal is sent, timer shall stop (SS2070_Timer_Stop).

```
pb→ code = SS2070_Timer_Sig;          /* request for one-shot signal */  
pb→ param1 = signal;  
pb→ param2.param = period;
```

- b. Send recurring periodic signal. Sets timer to zero and schedules repeating periodic signal.

```
pb→ code = SS2070_Timer_Cyc (0x1001); /* request for periodic signal */  
pb→ param1 = signal;  
pb→ param2.param = period;
```

- c. Start timer. Starts the timer if stopped or null. Timer will free run in a periodic mode, starting at the current timer value as its initial value and timer's maximum allowable time as its timer period. Timer will not send a signal and any pending signals will be cancelled.

```
pb→ code = SS2070_Timer_Start;      /* start timer if stopped */
```

- d. Stop timer. Leaves current value in timer. Cancels any pending signals.

```
pb→ code = SS2070_Timer_Stop;      /* stop timer if running */
```

- e. Reset timer. Stops timer if running, resets timer value to zero, and cancels any pending signals.

```
pb→ code = SS2070_Timer_Reset;     /* reset timer (stop and zero) */
```

9.2.7.2.3.4 Timer Extension

Timer Extension to Standard OS-9 Function Calls:

The timer driver shall support the following function with the SS_2070 option code and custom parameter block structure:

```
error_code _os_getstat(path_id path, SS_2070, PB2070 *pb);
```

- a. Retrieve current timer configuration.

```

typedef struct
{
    u_int32 value;
    u_int32 mode;
    u_int32 signal;
    u_int32 period;
} Timer_status;

pb→ code = GS2070_Status (0x1C) /* Request timer status data */
pb→ param1 = sizeof(Timer_status)
pb→ param2.pointer = &Timer_status *

```

Status data shall be returned in the structure pointed to by pb→param2.pointer as follows:

```

pb→ param2.pointer→value /* current timer value in μS x 100 */
pb→ param2.pointer→mode /* SS2070_Timer_Sig if one-shot signal pending,
SS2070_Timer_Cyc if periodic signal pending,
SS2070_Timer_Start if free running,
SS2070_Timer_Stop if not active
SS2070_Timer_Reset if timer is reset
SS2070_Timer_Null when timer is first
initialized */

pb→ param2.pointer→signal /* signal code pending if
SS2070_Timer_Sig or
SS2070_Timer_Cyc, 0 otherwise */

pb→ param2.pointer→period /* timer period in μS x 100 if
SS2070_Timer_Sig or
SS2070_Timer_Cyc and
Maximum Timer Period if
SS2070_Timer_Start
, 0 otherwise */

```

The following values shall be returned when the timer is in the SS2070_Timer_Null (Timer initialized) Mode:

```

Timer Mode = SS2070_Timer_Null
Timer Value = 0
Timer Period = 0
Timer Signal = 0

```

The following values shall be returned when the timer is in the SS2070_Timer_Start Mode:

```

Timer Mode = SS2070_Timer_Start
Timer Value = Running Timer Value
Timer Period = Maximum Timer Period
Timer Signal = 0

```

The following values shall be returned when the timer is in the SS2070_Timer_Stop Mode:

Timer Mode = SS2070_Timer_Stop
Timer Value = Current Timer Value
Timer Period = 0
Timer Signal = 0

The following values shall be returned when the timer is in the SS2070_Timer_Reset Mode:

Timer Mode = SS2070_Timer_Reset
Timer Value = 0
Timer Period = 0
Timer Signal = 0

9.2.7.2.3.5 Timer Period

All timer periods are specified in units of hundreds of microseconds (μ S), i.e. a timer period of 7 = 700 μ S. The minimum allowed timer period shall be 500 μ S. The maximum timer period for timers 1-4 shall be 6.5535 seconds (0xFFFF). The maximum timer period for timer12 and timer34 shall be 429496.7295 seconds (0xFFFFFFFF). The driver shall return error E\$Param from _os_setstat() if the requested timer period is outside the allowable range.

9.2.7.2.4 CPU Datakey

Access and control to the CPU Datakey shall be provided through the following descriptor name and OS-9 functions:

Descriptor name:

datakey = access to the CPU Datakey

Function Calls:

```
error_code = _os_open (char *datakey_desc_name, path_id *path);
```

```
error_code = _os_close (path_id path);
```

```
error_code = _os_read (path_id path, void *data_buffer, u_int32 *data_size);
```

```
error_code = _os_write (path_id path, void *control, u_int32 *data_size);
```

```
error_code = _os_seek(path_id path, u_int32 *position); sets read / write offset
```

```
error_code = _os_ss_erase(path_id path, u_int32 num_sec_erase); erases sector(s)  
if pointer is on a block boundary, returns E$PARAM error if not on a boundary */
```

```
error_code = _os_gs_pos(path_id path, u_int32 *position); /* gets current file  
pointer position */
```

```
error_code = _os_gs_size(path_id path, u_int32 *size); /* gets current datakey size  
*/
```

Error codes returned by Function calls:

E\$NotRdy if datakey is not inserted

E\$Seek if Offset plus *data_size is beyond end of CPU Datakey.

E\$EOF if upon read or write, the last byte of CPU Datakey has previously been processed.

Note: Use of SCF to implement the datakey driver is not allowed.

9.2.7.2.5 Flow Control Modes

The asynchronous serial communications device drivers shall support the six flow control modes (FCM#) described below:

FCM#	Description
1.	No Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed. This is the default mode. When user programs issue the first RTS related command, the driver switches to Manual Flow Control Mode (FCM# 1).
2.	Manual Flow Control Mode: The driver transmits data regardless of the state of CTS. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
3.	Auto-CTS Flow Control Mode: The driver transmits data only when CTS is externally asserted. The user program has absolute control of the RTS state. The driver doesn't automatically assert or de-assert RTS.
4.	Auto-RTS Flow Control Mode: The driver transmits data regardless of the state of CTS. Upon a write command, the driver asserts RTS, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If the user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
5.	Fully Automatic Flow Control Mode: The driver transmits data only when CTS is externally asserted. Upon a write command, the driver asserts RTS and waits for CTS, starts data transmission when CTS is asserted, and de-asserts RTS when data transmission is completed and any configured RTS extension is elapsed. If user program asserts RTS, then RTS remains on until the user program de-asserts RTS. If the user program de-asserts RTS before the transmission buffer is empty, the driver holds RTS on until the transmission buffer is empty and any configured RTS extension is elapsed.
6.	Dynamic Flow Control Mode: The driver transmits data only when CTS is externally asserted. The driver controls RTS based on the status of its receiving buffer. The driver asserts RTS continuously as long as its receiving buffer has sufficient capacity to store incoming data. If the receiving buffer approaches full, the driver de-asserts RTS until enough data has been read from the buffer to create sufficient receive capacity.

9.2.7.2.5.1 Serial Device Driver

The serial device driver shall be able to set user options via `_os_setstat()` and return status via `_os_getstat()`. To support legacy application programs, the device driver shall also be able to set user options via `_os_ss_size()` and to return status via `_os_gs_size()`:

```
error_code _os_setstat(path_id path, SS_2070, void *pb);
error_code _os_getstat(path_id path, SS_2070, void *pb);
error_code _os_ss_size(path_id path, u_int32 size);
error_code _os_gs_size(path_id path, u_int32 *size);
```


Note: The preferred method of accessing serial device drivers is through `_os_setstat()` and `_os_getstat()`. The `_os_ss_size()` and `_os_gs_size()` interface may not be required by future versions of this specification and is therefore not recommended for new development.

The option subcodes to be passed in `pb→code` and the data to be contained in `pb→param1` are defined as follows. `pb→param2` is unused here and should be set to 0 (zero). For `_os_ss_size()` and `_os_gs_size()`, the size argument is the same format as `pb→param1`.

9.2.7.2.5.2 Supported Setstat

The supported `_os_setstat()` / `_os_ss_size()` options shall be as follows.

- a. **Subcode passed in `pb→code` is `SS2070_OFC (0x23)`.**

Data passed in `pb→param1` is defined as follows:

Bits	Description
31-24	Auto RTS turn-off extension in number of characters (range:0-255, 0=default).
23-14	Reserved for future use.
13	Inhibit return of error E\$Write from <code>_os_write()</code> when transmit buffer full in FCM# 2, 4, 5 (default=0, 0=error, 1=block)
12	Inhibit variable SCC MRBLR (default =0; 0=NO; 1=inhibit).
11	Inhibit SCC TODR (default=0; 0=NO; 1=inhibit).
10-8	Flow Control Mode Number (FCM#) (range:0-5).
7-0	Subcode <code>SS2070_OFC (0x23)</code> .

Variable MRBLR (68360 SCC)

To reduce the IRQ handler overhead, the 68360 SCC driver shall use variable MRBLR as follows. If `SS2070_OFC` bit 12 is set to 1, the MRBLR shall be fixed at 16 for all baud rates. Variable MRBLR is not required for SP1 or SP8 on the 2070-1B CPU Module.

Baud Rate	MRBLR Setting
1200	1
2400	2
4800	4
9600	8
19200 & Higher	16

TODR (68360 SCC)

TODR requests processing a new TX buffer immediately. To reduce impact on other serial channel operations, `SS2070_OFC` bit 11 may be set to 1 to prevent assertion of TODR. TODR is not required for SP1 or SP8 on the 2070-1B CPU Module.

- b. Subcode passed in `pb→code` is `SS2070_IFC (0x22)`.
Data passed in `pb→param1` is defined as follows:

Bits	Description
31-11	Reserved for Future Use.
10	DCD must be asserted to receive data (default=0; 0=NO; 1=YES).
9-8	Reserved for Future Use.
7-0	Subcode = SS2070_IFC (0x22).

c. **Subcode passed in pb→code is SS2070_SSig (0x1A).**

1. If CTS is currently negated and bits 16-31 are not all 0:
Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal as soon as CTS is asserted.
Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot signal immediately.
2. If CTS is currently asserted and bits 16-31 are not all 0:
Setting the SS2070_SSig parameter block bit 11 (send when CTS is asserted) will cause the controller to send a one-shot signal immediately.
Setting the SS2070_SSig parameter block bit 12 (send when CTS is negated) will cause the controller to send a one-shot as soon as CTS is negated.
3. If both bits 11 and 12 of the SS2070_SSig parameter block are set, and bits 16-31 are not all 0:
The controller will send a one-shot signal upon the next change of CTS state

Data passed in pb→param1 is defined as follows:

Bits	Description
31-16	A signal number to be sent to calling process when the state of an input changes.
15-13	Reserved for Future Use.
12	Send signal when CTS is de-asserted.
11	Send signal when CTS is asserted.
10-8	Reserved for Future Use.
7-0	Subcode = SS2070_SSig (0x1A).

9.2.7.2.5.3 Supported Getstat

The supported `_os_getstat()` / `_os_gs_size()` options shall be as follows.

- a. **Subcode passed in pb→code is GS2070_Status (0x1C).**
Data returned in pb→param1 is defined as follows:

Bits	Description
31-16	Current unfilled transmit buffer character count of the serial device driver.
15-11	Reserved for Future Use.
10-8	Current Flow Control Mode Number (FCM#).

7	Reserved for Future Use.
6	Overrun error –0=no error; 1=error has occur since last GS2070_Status call.
5	Frame error –0=no error; 1=error has occur since last GS2070_Status call.
4	Parity error –0=no error; 1=error has occur since last GS2070_Status call.
3-2	Reserved for Future Use.
1	DCD state –0=de-asserted; 1=asserted.
0	CTS state –0=de-asserted; 1=asserted.

9.2.7.2.6 Device Drivers Compliant

Device drivers compliant with the OS-9 SCFMAN shall be provided for CPU Activity LED Indicator and Day Light Savings time correction features. The descriptor names shall be as follows:

led = access to CPU Activity LED Indicator

dstclock = access to Daylight Savings Time Clock correction

The standard OS-9 SCFMAN library calls and their functions are as follows:

```
error_code _os_open (char *desc_name, path_id *path);          //open descriptor for command
error_code _os_close (path_id path);                          //close descriptor
error_code _os_write (path_id path, void *value, u_int32 *data_size); //set value of function
*value = 1, turn on LED or enable DST correction (default)
*value = 0, turn off LED or disable DST correction set u_int32*data_size to 1
error_code _os_read (path_id path, void *value, u_int32 *data_size ); //get current state set
u_int32*data_size to 1
```

9.2.7.2.7 Manufacturer Support

The manufacturer shall provide the following features to support the TOD operation and synchronization.

9.2.7.2.7.1 Leap Year and Daylight Savings Time

Leap Year and Daylight Savings Time (DST) Adjustments - The OS-9 System clock / calendar shall automatically be adjusted to account for DST and leap years.

9.2.7.2.7.2 Setting Hardware Clock

Setting Hardware Clock from OS-9 System Clock - A device driver compatible with the OS-9 SCFMAN shall be provided to allow the hardware TOD clock/calendar to be updated from the OS-9 system clock under application control. The descriptor name shall be “ClockUpdate.” Opening the descriptor shall cause the driver to synchronize the clock to a minimum of 10 ms resolution. The driver shall compensate for any time elapsed during the process of updating the hardware clock.

9.2.7.2.7.3 Setting OS-9 System Clock

Setting OS-9 System Clock from Hardware Clock - At system power up, the OS-9 system TOD clock/calendar shall automatically be updated from the hardware TOD clock. The clocks shall be synchronized to a minimum of 10 ms resolution.

9.2.7.2.8 Flash Ram Drive

The FLASH drive shall be protected from corruption. It shall be protected using the Write Protect (WP) bit of the Base Register. When writing to the FLASH drive the

current sector of FLASH being written shall first be backed up in SRAM. The backup sector copy shall be invalidated when FLASH write operation is completed. In case of power failure, the FLASH driver shall detect the presence of the valid backup sector copy in SRAM and shall read sector data from the valid backup sector copy.

A user write operation shall restore the valid backup sector copy first. Execution of the program module, "FLRESTORE," in the Boot Image shall also restore the valid backup sector copy to FLASH drive after a specified delay. "FLRESTORE" shall accept a delay parameter in seconds ranging from 0 to 600 seconds. The default delay factor is 30 seconds.

9.2.7.3 OS-9 Application Kernel

9.2.7.3.1 Boot Sysreset

The provided software shall boot OS-9 from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the default parameters as listed in A9-16.

9.2.7.3.2 Hardware Initialization

Hardware initialization, preliminary self-test, OS-9 initialization (except Extended Memory Test), and forking OPEXEC shall be completed in less than 4 seconds. This startup time shall be measured from the release of SYSRESET to the turn on of the CPU_ACTIVE LED using a user level program named ONLED. The ONLED program shall be the last module loaded into RAM and executed using opexec or a startup file.

9.2.7.3.3 Startup Procedure

The boot image init module shall be configured with the default directory name as /f0wp and sysgo as the first executable module.

Sysgo shall operate as follows:

1. Sysgo shall set the execution directory to /f0wp/CMDS
2. Sysgo shall check if the backspace key (0x08) is being received on /sp4 (c50j). If received, Sysgo shall:
 - a. Fork a shell with no arguments on /sp4 using the current directory.
 - b. Remain an active process and monitor the shell for termination. If the shell does terminate, Sysgo shall fork another shell with no arguments on /sp4. Unless Sysgo dies, a shell shall always be provided on /sp4.
3. If the backspace key was not received, Sysgo shall check for the presence of a Datakey. If present and valid (Datakey Header Version 2 or greater), Sysgo shall check the Startup Override Byte in the Datakey header.

If Startup Override is 0x01, Sysgo shall:

- a. Fork a shell that executes a shell script stored on the Datakey in the following format. Immediately following the key header shall be a 2-byte value indicating the length of the script. The script shall immediately follow the length value, and shall be stored as ASCII text.
 - b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.
- If Startup Override is 0x02, Sysgo shall:
- a. Fork an executable module stored on the Datakey immediately following the header.
 - b. If there is any error loading or forking the module, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking the module, Sysgo shall then exit without forking a shell.
4. If the backspace key was not received and Startup Override Byte is 0xFF:
 - a. Sysgo shall fork the module named /f0wp/OPEXEC if present at /f0wp.
 - b. If there is any error loading or forking OPEXEC, Sysgo shall display an error message on /sp4 and fork a shell as described in step 2. If there are no errors forking OPEXEC, Sysgo shall then exit without forking a shell.
 5. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC file:
 - a. Sysgo shall fork a shell that executes a shell script named /f0wp/startup if present at /f0wp.
 - b. If there is any error reading or starting the script or if the shell terminates with an error, Sysgo shall display an error message on /sp4 and fork another shell as described in step 2. If there are no errors executing the script, Sysgo shall exit without forking another shell.
 6. If the backspace key was not received, Startup Override Byte is 0xFF, and there is no OPEXEC and no startup file:
 - a. Sysgo shall fork a shell as described in step 2.

9.2.7.3.4 Short Out

A Short Out is defined as the period of time between ACFAIL/POWER DOWN transition to LOW and back to HIGH without a SYSRESET transition to LOW. ACFAIL/POWER DOWN transitions shall generate an interrupt. The interrupt shall update an OS-9 event named "ACFAIL". The "ACFAIL" event shall set a value 1 indicating an ACFAIL condition occurred for the DOWN transition and set 0

indicating non-ACFAIL condition for the HIGH transition. The IRQ7 and auto-vector 31(7) shall not be used to update the "ACFAIL" event.

In addition, the ACFAIL condition shall generate the OS-9 auto-vector 30(6) interrupt service. Each interrupt service installed shall exit with the "Carry Bit" set allow OS9 to propagate the ACFAIL interrupt. The Contractor shall supply an interrupt handler at priority 255 that acknowledges and clears the interrupt.

Priority 1 shall be reserved for the OS-9 system.

9.2.7.3.5 Long Out

A Long Out is defined as ACFAIL transition to LOW follow by a SYSRESET going LOW. The SYSRESET going HIGH shall be followed by an operating system reboot.

9.2.7.4 Error Handler

9.2.7.4.1 Initialization and Power-Up Test

A manufacturer may include an error handling routine to save troubleshooting data regarding initialization, power-up test abnormalities and other error conditions. If used, the error report shall be stored in the file /r0/ErrorReport and shall not exceed 11kb in size.

9.2.7.5 Network Requirements

On the MODEL 2070-1E CPU module, an OS-9 SPF Ethernet hardware driver and descriptor for the 68360 (SCC1) shall be provided in the operating system Boot Image. The descriptor shall be named spqe0.

9.2.7.5.1 BOOTOBS

The following OS-9 modules should be included in the /f0/CMDS/BOOTOBS flash disk directory to allow for standard TCP/IP network communications using Ethernet Protocol over Ethernet hardware and/or Serial Line Internet Protocol (SLIP) or Point-to-Point Protocol over serial links:

1. Drivers and Descriptors for PPP.
2. Drivers and Descriptors for SLIP.
3. LAN Comm Pak modules: spenet, enet, spip, ip0, sptcp, tcp0, spudp, udp0, spraw, raw0, sproute, route0, spicp, ipc0, splcp, lcp0, sphdlc, hdlc0, spslip, sps10
4. Network modules pkman, pkdvr, pk, pks
5. Network Trap Handler: netdb_local, netdb_dns
6. NFS Modules: nfs, nfsnul and nfs_devices.

The PPP and SLIP descriptors shall have baud rates and ports set as follows and be stored in the /f0/CMDS/BOOTOBS directory,

hdlc0 and sps10 configured to use /sp1 and 38400 bps

hdlc1 and sps11 configured to use /sp2 and 115200 bps

hdlc2 and sps12 configured to use /sp3 and 115200 bps

hdlc3 and sps13 configured to use /sp4 and 38400 bps

9.2.7.5.2 CMDS

The following Network utilities shall be included and shall reside in the /f0/CMDS directory as identified in this specification.

arp, dhcp, tftp, tftpd, ftp, ftpd, ftpdc, idbdump, idbgen, rpcdbgen, ifconfig, inetd, ipstart, ndbmod, netstat, ping, route, routed, telnet, telnetdc, hostname, nfsc, mount, rpdump, nfsstat, exportfs, portmap, pppd, chat, pppauth, nfsd, mountd, and showmount.

9.2.7.5.3 Multi-user functionality

The boot image init module shall be configured with a “default directory name” as /f0wp. This will allow login and tsmon to provide the user with login prompt from the terminal port or from the network via a telnet session.

The following OS-9 modules should be included in the operating system boot image for the implementation of multi-user mode.

login, tsmon

9.2.7.5.4 Network Configuration

The modules inetdb, inetdb2 and rpcdb shall be generated by the make utility via the use of a makefile and the network configuration files residing the /f0/ETC directory. The generated inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The modules shall be configured with the network default values as defined in Section 9.2.6 (Data Key) via the interfaces.conf shell script.

9.2.7.5.5 Netcfg

A Utility Program named netcfg shall be provided that reads the CPU Datakey for an IP Address, Subnet Mask and Default Gateway. If the Datakey is present and valid (**Datakey Header Version 2 or greater**), netcfg shall set the IP Address, Subnet Mask and Default Gateway of the Model 2070 Controller when executed by a user at the command line. The netcfg utility shall create a new inetdb, inetdb2 and rpcdb database module based on the Datakey network parameters or network parameters from the command line. The new inetdb, inetdb2 and rpcdb modules should be re-located to the /f0/CMDS/BOOTOBJS directory where they will be pick-up by the network configuration shell scripts located at /f0/SYS. The netcfg shall also allow the user to read, write and display network parameters to and from the Datakey via the command line prompt. If the Datakey is not present or invalid and the flag option is not “n” netcfg shall display an error and exit without altering the network configuration. The netcfg utility shall reside in /f0/CMDS.

Netcfg options:

a= Write IP Address in Datakey
m= Write Netmask Address in Datakey
g= Write Gateway Address in Datakey

If the checksum is incorrect when executing the -a, -m or -g option the following will occur:

1. The default Datakey data will be loaded.
2. The networking changes will be made to the default networking parameters.
3. The CRC will be recalculated.
4. The networking parameters will be written to the Datakey.

This option loads default networking parameters into the Datakey.

-d= Write Default Networking Parameters in the Datakey

This option will display the networking information contained in the Datakey.

-i= Reads Networking Parameters from the Datakey

This option will set the networking parameters permanently on the controller using values from the Datakey

-c= Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.

Normal operation of this option will be:

1. Read the Datakey networking parameters
2. Delete interfaces.conf and routes.conf from /f0/etc
3. Write new interfaces.conf and routes.conf in /f0/etc.
4. Execute idbgen to create new inetdb and inetdb2
5. Executes rpcdbgen to create a new rpcdb
6. Delete inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.
7. Relocate inetdb, inetdb2 and rpcdb in /f0/cmds/bootobjs.

This option will display the current Controller Network Parameters such as the IP Address, Netmask , Gateway and **MAC Address**. This requires the network Stack to be initialized.

-r= Reads current Networking Configuration.

This option will set the networking parameters dynamically on the controller using values from the Datakey

-s= Sets Network Configuration Dynamically from the Datakey.

This option will set the networking parameters permanently on the controller using values from the command line. The option will do the same functions as option “c” with network parameters from the command line.

n= Set Controller Network Parameters without the Datakey

The **netcfg -n -a [opts] -m [opts] -g [opts]** shall allow the user to permanently set the IP Address, Subnet Mask and Gateway of the Model 2070 Controller when executed by the user at the command line using parameters provided by the user at the command line.

Where **opts** may be IP Address in the format **xxx.xxx.xxx.xxx**, **netmask** in the format **xxx.xxx.xxx.xxx** and **gateway** as **xxx.xxx.xxx.xxx**.

Example, the following sets the IP Address, Netmask and Gateway permanently in the Model 2070 Controller to 10.20.70.51, 255.255.255.0 and 10.20.70.254:

```
netcfg -n -a 10.20.70.51 -m 255.255.255.0 -g 10.20.70.254
```

These options will display the help menu on how to use the netcfg utility.

h, ?, blank = displays the help menu

The help menu shall consist of the following:

Netcfg Usage:

```
netcfg [- a ] [-m ] [-g ] [-n ] [-d ] [- i ] [- r ] [- s ]
```

-a follows Ip Address ; Write IP Address in Datakey
-m follows Netmask ; Write Netmask Address in Datakey
-g follows Gateway ; Write Gateway Address in Datakey

-d ;Write Default Networking Parameters in the Datakey

- i ;Reads Networking Parameters from the Datakey
- c ;Changes interfaces.conf and builds inetdb, inetdb2 and rpcdb.
- r ;Reads current Controller Networking Configuration.
- s ;Sets Network Configuration Dynamically from the Datakey.
- n <network parameters> ;Set Controller Network Parameters without Datakey

Example of option -n:

```
netcfg -n -a 10.20.70.51 -m 255.255.255.0 -g 10.20.70.254
```

See Section 9.2.6 for additional information.

9.2.7.5.6 ETC

A set of example configuration files consistent with the above networking modules shall be provided in the /f0/ETC directory. This directory shall contain the following text files.

hosts, hosts.equiv, networks, protocols, services, inetd.conf, resolv.conf, hosts.conf, rpc, interfaces.conf, routes.conf, makefile, nfs.map, nfsd.map

9.2.7.6 Standard Microware File System Configuration

9.2.7.6.1 Directories

The 2070 shall follow Standard Microware File System Configuration. A /f0/CMDS, /f0/CMDS/BOOTOBS, /f0/ETC and /f0/SYS directories shall be implemented. Execute permission shall be included in the attributes of files in the /f0/CMDS directory. Sysgo should set its execution directory to /f0wp/CMDS prior to spawning opexec or other processes. The /f0/CMDS/BOOTOBS shall contain the modules as identified above and other customizable descriptors and modules. The /f0/SYS shall also contain the following four standard OS-9 network configuration shell script files: startspf, startnfs, loadspf and loadnfs.

9.2.7.6.2 Password

The /f0/SYS shall contain a "password" file. The password file should follow Microware's password file format for the addition and configuration of multiuser functionality and password protection. A user name "super" with password as "user" shall be defined in the password file.

A Termcap text file shall be include in the /f0/SYS directory. This Termcap file shall contain description fields defining the capability names and values of the front panel DISPLAY.

9.2.7.6.3 utilities

The utilities tar, make, fixmod , mshell and vi shall be included in the /f0/CMDS directory.

9.2.7.6.4 Ver

A Ver utility shall be provided as part of the OS-9 Image and shall allow access to Controller's Manufacturer Name, Image Build Number, TEES Version, Image Build Date and CPU Module Type. Ver should display the contents of a data module named "bootid" which contains in it's data area the following structure:

```
/* bootid_body*/
Struct bootid_body {

char *mfgrname;           /* Manufacturer Name */
char *cpumoduletype;     /* CPU Module Type */
char *teesrelease;       /* TEES Release */
char *imagebuilddate;    /* Image Build Date */
u_int 16 majv;           /* Major Version*/
u_int 16 minv;           /* Minor Version */
u_int 16 sv1;            /* Sub-Version 1 */
u_int 16 sv2;            /* Sub-Version 2 */
u_int 16 sv3             /* Sub-Version 3 */
u_int 16 dv;             /* Development Version */
};
```

When run via the command line the Ver utility shall display the following:

Ver options:

```
-a   Shows all information
-b   CPU Module Type
-d   Image Build Date
-m   Controller's Manufacturer Name
-t   TEES Version
-v   Image Build Version Number
-?   Display Help
```

CPU Type shall display 2070-1A, 2070-1E or 2070-1C.

Image Build Date shall be in the form of mm/dd/yyyy

Manufacturer's name shall be shown as one word only.

TEES Version shall be "TEES XXXX EY" where XXXX is the is the year of the TEES and Y is any Errata if applicable.

Ver without an option shall be the same as Ver -a.

Ver -a shall display all information as shown by the following example:

```
2070 -1E
03/06/2008
Vendor Name
TEES 2008 E5 ; E5 Would be blank if there are no Erratas.
Build 2.7.3.0.0.0
```

The help menu shall consist of the following:

Ver Usage:

```
Ver [- a ] [-b ] [-d ] [-m ] [-t ] [- v ] [-? ]
```

```
-a    Shows all information
-b    CPU Module Type
-d    Image Build Date
-m    Controller's Manufacturer Name
-t    TEES Release
-v    Image Build Version Number
-?    Display Help
```

9.2.8 Model 2070-1C CPU Software

9.2.8.1 Operating System

The model 2070-1C CPU Module shall be supplied with Linux 2.6.18 kernel or later. Platform specific options shall be selected by the manufacturer based on the requirements of the MPC 82xx/ 83xx and the Model 2070-1C CPU options selected by the agency.

The items marked with an asterisk (*) shall be the minimum Linux kernel configuration features that shall be included in the kernel build; others shall be included when possible:

```
#
# Automatically generated make menuconfig
# Linux kernel version: 2.6.18
# Tue Nov 7 11:57:18 2006
#
#
# Code maturity level options
#
CONFIG_BROKEN_ON_SMP=y
CONFIG_LOCK_KERNEL=y
CONFIG_INIT_ENV_ARG_LIMIT=32

#
# General setup
```

```

#
CONFIG_LOCALVERSION=""
CONFIG_SWAP=y
CONFIG_SYSVIPC=y *
CONFIG_IKCONFIG=y *
CONFIG_IKCONFIG_PROC=y *
CONFIG_INITRAMFS_SOURCE=""
CONFIG_EMBEDDED=y *
CONFIG_SYSCTL=y *
CONFIG_HOTPLUG=y *
CONFIG_PRINTK=y
CONFIG_BUG=y
CONFIG_ELF_CORE=y *
CONFIG_BASE_FULL=y
CONFIG_FUTEX=y
CONFIG_EPOLL=y
CONFIG_SHMEM=y
CONFIG_VM_EVENT_COUNTERS=y
CONFIG_RT_MUTEXES=y
CONFIG_BASE_SMALL=0
CONFIG_SLOB=y

#
# Loadable module support
#
CONFIG_MODULES=y *
CONFIG_MODULE_UNLOAD=y *
CONFIG_MODVERSIONS=y
CONFIG_MODULE_SRCVERSION_ALL=y
CONFIG_KMOD=y *

#
# Processor type and features
#

CONFIG_PREEMPT=y *
CONFIG_PREEMPT_BKL=y

#
# Bus options (PCI, PCMCIA, EISA, MCA, ISA)
#
CONFIG_PCI=y
CONFIG_PCI_GOANY=y
CONFIG_PCI_BIOS=y
CONFIG_PCI_DIRECT=y

#
# Executable file formats
#
CONFIG_BINFORMAT_ELF=y *
CONFIG_BINFORMAT_AOUT=m *

#
# Networking
#
CONFIG_NET=y

```

```

#
# Networking options
#
CONFIG_PACKET=y *
CONFIG_PACKET_MMAP=y *
CONFIG_UNIX=y *
CONFIG_INET=y *
CONFIG_IP_MULTICAST=y *
CONFIG_IP_FIB_HASH=y
CONFIG_IP_PNP=y *
CONFIG_IP_PNP_DHCP=y *
CONFIG_IP_PNP_BOOTP=y *
CONFIG_IP_PNP_RARP=y
CONFIG_SYN_COOKIES=y *
CONFIG_TCP_CONG_BIC=y

#
# IP: Virtual Server Configuration
#
CONFIG_IPV6=y
CONFIG_NETFILTER=y *

#
# Device Drivers
#

#
# Generic Driver Options
#
CONFIG_STANDALONE=y
CONFIG_PREVENT_FIRMWARE_BUILD=y
CONFIG_FW_LOADER=m

#
# Block devices
#
CONFIG_BLK_DEV_FD=y
CONFIG_BLK_DEV_LOOP=y *
CONFIG_BLK_DEV_NBD=m
CONFIG_BLK_DEV_RAM=y *
CONFIG_BLK_DEV_RAM_COUNT=16
CONFIG_BLK_DEV_RAM_SIZE=4096
CONFIG_BLK_DEV_RAM_BLOCKSIZE=1024
CONFIG_BLK_DEV_INITRD=y *

#
# SCSI device support
#
CONFIG_SCSI=y *
CONFIG_SCSI_PROC_FS=y *

#
# SCSI support type (disk, tape, CD-ROM)
#

```

```

CONFIG_BLK_DEV_SD=y *
#

#
# Network device support
#
CONFIG_NETDEVICES=y
CONFIG_DUMMY=y
#
# Ethernet (10 or 100Mbit)
#
CONFIG_NET_ETHERNET=y *
CONFIG_MII=y
#
# Wan interfaces
#
CONFIG_WAN=y
CONFIG_PPP=y
CONFIG_PPP_FILTER=y
CONFIG_PPP_ASYNC=y
CONFIG_PPP_SYNC_TTY=y
CONFIG_PPP_DEFLATE=y
CONFIG_PPP_BSDCOMP=y
CONFIG_SLIP=y
CONFIG_SLIP_COMPRESSED=y
CONFIG_SLIP_MODE_SLIP6=y
#
# Input device support
#
CONFIG_INPUT=y
#
# Serial drivers
#
#
# Non-8250 serial port support
#
CONFIG_UNIX98_PTYS=y *
CONFIG_LEGACY_PTYS=y *
CONFIG_LEGACY_PTY_COUNT=256 *

#
#
#
CONFIG_RTC=y
#
#
# I2C support
#
CONFIG_I2C=y
#
# I2C Algorithms
#
CONFIG_I2C_ALGOBIT=m
CONFIG_I2C_ALGOPCF=m
#
# SPI support
#
CONFIG_SPI=y

```

```

CONFIG_SPI_MASTER=y
#
# USB support
#
CONFIG_USB_ARCH_HAS_HCD=y
CONFIG_USB_ARCH_HAS_OHCI=y
CONFIG_USB_ARCH_HAS_EHCI=y
CONFIG_USB=y *
#
# Miscellaneous USB options
#
CONFIG_USB_DEVICEFS=y *

#
# NOTE: USB_STORAGE enables SCSI, and 'SCSI disk support'
#
# may also be needed; see USB_STORAGE Help for more information
#
CONFIG_USB_STORAGE=y *
CONFIG_USB_STORAGE_FREECOM=y *
CONFIG_USB_STORAGE_ISD200=y *
CONFIG_USB_STORAGE_DPCM=y *

#
# USB Input Devices
#
CONFIG_USB_HID=y
CONFIG_USB_HIDINPUT=y

#
#

#
# File systems
#
CONFIG_EXT2_FS=y *
CONFIG_EXT3_FS=y
CONFIG_JBD=y
CONFIG_INOTIFY=y
CONFIG_INOTIFY_USER=y
CONFIG_DNOTIFY=y

#
# DOS/FAT/NT Filesystems
#
CONFIG_FAT_FS=y *
CONFIG_MSDOS_FS=y *
CONFIG_VFAT_FS=y *
CONFIG_FAT_DEFAULT_CODEPAGE=437 *
CONFIG_FAT_DEFAULT_IOCHARSET="iso8859-1" *
CONFIG_NTFS_FS=m
CONFIG_NTFS_RW=y

#
# Pseudo filesystems
#
CONFIG_PROC_FS=y *
# CONFIG_PROC_KCORE is not set

```



```

CONFIG_SYSFS=y *
CONFIG_TMPFS=y *
CONFIG_RAMFS=y *

#
# Miscellaneous filesystems
#

#
# Network File Systems
#
CONFIG_NFS_FS=y *
CONFIG_NFS_V3=y *
CONFIG_NFSD=y *
CONFIG_NFSD_V3=y *
CONFIG_NFSD_TCP=y *
CONFIG_ROOT_NFS=y *
CONFIG_LOCKD=y *
CONFIG_LOCKD_V4=y *
CONFIG_EXPORTFS=y *
CONFIG_NFS_COMMON=y *
CONFIG_SUNRPC=y *

#
# Native Language Support
#
CONFIG_NLS=y
CONFIG_NLS_DEFAULT="iso8859-1" *

#
# Kernel hacking
#
CONFIG_TRACE_IRQFLAGS_SUPPORT=y
# CONFIG_PRINTK_TIME is not set
# CONFIG_MAGIC_SYSRQ is not set
# CONFIG_UNUSED_SYMBOLS is not set
# CONFIG_DEBUG_KERNEL is not set
CONFIG_LOG_BUF_SHIFT=14
# CONFIG_DEBUG_BUGVERBOSE is not set
# CONFIG_DEBUG_FS is not set
# CONFIG_UNWIND_INFO is not set
CONFIG_EARLY_PRINTK=y
# CONFIG_DOUBLEFAULT is not set

#
# Security options
#
# CONFIG_KEYS is not set
# CONFIG_SECURITY is not set

#
# Cryptographic options
#
CONFIG_CRYPTODEV=y *
CONFIG_CRYPTODEV_DMABUF=y *
CONFIG_CRYPTO_MD4=y
CONFIG_CRYPTO_MD5=y *

```

```
CONFIG_CRYPT_SHA1=y
CONFIG_CRYPT_DES=y
CONFIG_CRYPT_AES=y
CONFIG_CRYPT_ARC4=y

#
# Library routines
#
CONFIG_CRC_CCITT=y
CONFIG_CRC32=y *
CONFIG_ZLIB_INFLATE=y *
CONFIG_ZLIB_DEFLATE=y *
```

9.2.8.2 Linux Drivers

All Linux Drivers provided in the Model 2070-1C CPU shall be compliant to AASHTO, ITE and NEMA ATC Standard V. 5.2.b Annex B and as defined in these specifications. In case of conflict these specifications shall govern over ATC Standard V.5.2b.

9.2.8.2.1 GPIO

The GPIO driver allows the user to control the CPU active LED, determine if the Datakey is present, reset peripheral devices, and power down peripheral devices.

open()

The following dev entries shall exist:

```
/dev/datakeypresent
/dev/cpuactive
/dev/powerdown
/dev/cpureset
```

read()

```
int read(int filp, void *buf, int count);
```

This allows for reading the state of the power down pin and for reading the state of the whether the Datakey is inserted. The value passed in the count parameter must be 1 or no bytes will be read.

write()

```
int write(int filp, void *buf, int count);
```

Allows changing the state of the CPU Active LED and the CPU reset signal. Writing a single nonzero character to the /dev/cpuactive device shall turn on the CPU active LED and writing zero will turn off the LED.

close()

Closes the file descriptor.

9.2.8.2.2 Timers

This driver provides an abstraction for controlling up to 16 timers with 100µs resolution simultaneously. A timer can be used to send a one-shot or periodic signal to a process. A timer can be used in a free running mode where the timer is either restarted (stopped and cleared), started (running), or stopped. When the timer device node is opened, a timer is assigned automatically to the caller if one is available, thus eliminating the need for user applications to know which timers the other applications are using to avoid collisions.

Supported Device File Operations:

```
open();
close();
read();
ioctl();
```

open()

The dev entry for the timer driver shall be /dev/timers. When the device is opened, a timer is automatically assigned to the caller if there is one available; otherwise an error is returned to the caller.

close()

Closes the file descriptor and reinitializes the timer, making it available to be reused.

read()

A call to read with a count of at least 4 bytes will read a binary 32-bit unsigned integer containing the current value of the open timer.

ioctl()

```
ioctl(int fd, unsigned int cmd, unsigned long params);
```

This ioctl passes a parameter structure for the parameters. The structure used is defined as follows:

```
typedef struct {
    u32 code;
    u32 param1;
    union {
        u32 param;
        void *pointer;
    } param2;
} timing_params_t;
```

The ioctl supports getting and setting a timer status structure defined as follows:

```
typedef struct {
    u32 value;
    u32 mode;
    u32 signal;
    u32 period;
```

```
} Timer_status;
```

Command Definitions:

```
ATC_TIMER_GET_PARAMS  
ATC_TIMER_SET_PARAMS
```

ATC_TIMER_GET_PARAMS

When this command is issued, a `timing_params_t` shall be passed as the parameter. The `params.code` value shall be set to `ATC_TIMER_GET_STATUS`, `params.param2.pointer` shall point to a `Timer_status` structure, and `params.param1` shall be the number of bytes allocated for the `Timer_status` structure. The current timer status shall be copied into the location at `params.param2.pointer` or an error will be returned if an invalid length or invalid pointer was passed to the `ioctl`.

```
timing_params_t params;
```

Parameter Code Definitions:

```
ATC_TIMER_GET_STATUS
```

Example for retrieving timer configuration:

```
params.code = ATC_TIMER_GET_STATUS;  
params.param1 = sizeof(Timer_status);  
params.param2.pointer = &Timer_status;  
  
ioctl(fd, ATC_TIMER_GET_PARAMS, &params);
```

Status data should be returned in the structure pointed to by `params.param2.pointer` as follows:

```
params. param2.pointer→value // current timer value in μS x 100  
params. param2.pointer→mode // ATC__TIMER_SIG if one-shot signal pending,  
                             ATC_TIMER_CYC if periodic signal pending,  
                             ATC_TIMER_START if free running,  
                             ATC_TIMER_STOP if not active  
                             ATC_TIMER_RESET if timer is reset  
                             ATC_TIMER_NULL when timer is first  
                             initialized  
  
params. param2.pointer→signal // signal code pending if  
                             ATC_TIMER_SIG or  
                             ATC_TIMER_CYC, 0 otherwise  
  
params. param2.pointer→period // timer period in μS x 100 if  
                             ATC_TIMER_SIG or  
                             ATC_TIMER_CYC and  
                             Maximum Timer Period if  
                             ATC_TIMER_START
```

, 0 otherwise

The following values shall be returned when the timer is in the ATC_TIMER_NULL (Timer initialized) Mode:

Timer Mode = ATC_TIMER_NULL
Timer Value = 0
Timer Period = 0
Timer Signal = 0

The following values shall be returned when the timer is in the ATC_TIMER_START Mode:

Timer Mode = ATC_TIMER_START
Timer Value = Running Timer Value
Timer Period = Maximum Timer Period
Timer Signal = 0

The following values shall be returned when the timer is in the ATC_TIMER_STOP Mode:

Timer Mode = ATC_TIMER_STOP
Timer Value = Current Timer Value
Timer Period = 0
Timer Signal = 0

The following values shall be returned when the timer is in the ATC_TIMER_RESET Mode:

Timer Mode = ATC_TIMER_RESET
Timer Value = 0
Timer Period = 0
Timer Signal = 0

ATC_TIMER_SET_PARAMS

This function sets the mode of the timer based on the parameter code value in the structure of type `timing_params_t` that is passed as the parameter. As an example in the explanation of the parameter code definitions, the following variable will be used:

```
timing_params_t params;
```

Parameter Code Definitions:

```
ATC_TIMER_SIG  
ATC_TIMER_CYC  
ATC_TIMER_START  
ATC_TIMER_STOP  
ATC_TIMER_RESET  
ATC_TIMER_NULL
```

```
ATC_TIMER_SIG
```

This command sends a one-time signal to the caller process after a specified time.

Example to set up a one-time signal to be sent after 1/10 of a second:

```
params.code = ATC_TIMER_SIG;
params.param1 = SIGALRM; // signal code
params.param2 = 1000; // 1/10 of a second period
ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_CYC

This command sets up a one-shot signal to be sent to the caller process after a specified time. While in this mode, the current timer value can be read at any time by calling the read() function.

Example to set up cyclical signal to occur every 1/10 of a second:

```
params.code = ATC_TIMER_CYC;
params.param1 = SIGALRM; // signal code
params.param2 = 1000; // 1/10 of a second period
ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_START

This command starts the timer without clearing its value. The timer value will be incremented every 100us. The current value can be read by calling read() or by calling the ioctl with command ATC_TIMER_GET_PARAMS, and read the period member of the Timer_status structure.

Example:

```
params.code = ATC_TIMER_START;
ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_STOP

This command stops the timer without clearing its value. The current value can still be read while the timer is stopped.

Example:

```
params.code = ATC_TIMER_STOP;
ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

ATC_TIMER_RESET

This command stops the timer and resets the timer value. The timer value will read as 0 when in reset state.

Example:

```
params.code = ATC_TIMER_RESET;
ioctl(fd, ATC_TIMER_SET_PARAMS, &params);
```

9.2.8.2.1 Time of Day

The Time of Day driver overrides the operating system internal time of day to utilize AC line sync pulses or square wave pulses from the RTC. The time source can be changed via an ioctl command.

Supported Device File Operations:

```
open();  
close();  
read();  
write();  
ioctl();
```

open()

The dev entry for the timer driver shall be /dev/tod. The device can be opened for read, write, or read/write.

close()

Closes the file descriptor.

read() / write()

```
int read(int filp, void *buf, int count);  
int write(int filp, void *buf, int count);
```

Reads / Writes the current time of day value in the following format:

YYYYMMDDHHMMSSFFF

Y = year M = month D = day H = hour M = minute S = second F = fraction

The fractional field shall be a value from 0 to 127 in RTC Square Wave Mode and a value from 0 to 2 * AC Line Sync Frequency - 1 in AC Line Sync Mode.

If the *count* passed to the read() function is greater than 18, only 18 bytes will be read. A read always starts with the 4 byte year in ASCII decimal. If the count is less than 18, then read shall modify *count* bytes in *buf*.

If the *count* passed to write() is less than 17 or the data in *buf* is not in the proper format, then write shall return an error of EINVAL.

```
ioctl()  
ioctl(int fd, unsigned int cmd, unsigned long param);
```

The `ioctl` function supports multiple different commands, each described separately.

Command Definitions:

```
    ATC_TOD_SET  
    ATC_TOD_GET  
    ATC_TOD_SET_TIMESRC  
ATC_TOD_GET_TIMESRC  
ATC_TOD_GET_INPUT_FREQ  
ATC_TOD_REQUEST_TICK_SIG  
ATC_TOD_CANCEL_TICK_SIG  
ATC_TOD_REQUEST_ONCHANGE_SIG  
ATC_TOD_CANCEL_ONCHANGE_SIG  
ATC_DST_ENABLE  
ATC_DST_DISABLE  
    ATC_DST_SET_INFO  
ATC_DST_GET_INFO
```

ATC_SET and ATC_GET

These commands get and set the time and time zone atomically. The parameter to both functions is the same and defined below:

Parameter Data:

```
typedef struct {  
    struct timeval *tv;  
    int *tzsec_offset;  
    int *dst_offset;  
} atc_time_tz_t
```

The `ATC_SET` command is only concerned with the `tv` and `tzsec_offset` parameters. If the `tv` member is non-zero and the command is `ATC_SET`, then the time is set according to the `tv_sec` and `tv_usec` members of the struct `timeval *tv`. Additionally if the `tzsec_offset` parameter is non-zero the time zone offset is also set. The `ATC_GET` command sets the data pointed to by the `tv`, `tzsec_offset`, and `dst_offset` for each of those members that are non-zero.

ATC_SET_TIMESRC and ATC_GET_TIMESRC

Parameter Definitions:

```
ATC_TIMESRC_LINESYNC  
    ATC_TIMESRC_RTCQWR  
    ATC_TIMESRC_CRYSTAL  
    ATC_TIMESRC_EXTERNAL1  
    ATC_TIMESRC_EXTERNAL2
```

These commands get and set the time source. The time source may use AC line sync pulses or the RTC square wave output.

ATC_TOD_GET_INPUT_FREQ

This command gets the current frequency that is driving the time of day clock.

ATC_TOD_REQUEST_TICK_SIG

This command requests a signal to be sent at each tick of the time of day clock as long as the file device remains opened. The *param* value passed to `ioctl` is the signal number that should be sent to the calling process at each time of day clock tick.

ATC_TOD_CANCEL_TICK_SIG

This releases the signal from being sent when the time of day clock ticks. If the file device is closed, the signal is automatically released.

ATC_TOD_REQUEST_ONCHANGE_SIG

This command requests a signal to be sent each time the time of day clock is changed by more than one tick. The *param* value passed to `ioctl` is the signal number that should be sent to the calling process.

ATC_TOD_CANCEL_ONCHANGE_SIG

This releases the signal from being sent when the time of day is changed by more than one tick. If the file device is closed, the signal is automatically released.

These commands allow setting the daylight savings time information, which shall be used when daylight savings time is enabled.

Parameter Data:

```
typedef struct dst_info {
    char type;
    union dst_types_u {
        struct dst_absolute_struct {
            int secs_from_epoch_to_transition;
            int seconds_to_adjust;
        } absolute;
        struct dst_generic_struct {
            char month;
            char dom_type;
            union dst_gen_dom_union {
                char dom;
                // ex: second Saturday of month
                // ex: first Sunday on or after oct. 9
                struct dst_gen1_struct {
                    char dow; // day of week (sun-sat)
                    char occur; // number of occurrences
                    char on_after_dom; // day of month
                } week_and_day;
                // ex: second to last Thursday of month
                // ex: first Sunday on or before oct. 9
                struct dst_gen2_struct {
                    char dow; // day of week (sun-sat)
                    char occur; // number of occurrences
                    char on_before_dom // day of month
                } reverse_occurrences_of_day;
            } gendom;
            int seconds_to_adjust;
        } generic;
    } begin, end;
    unsigned char begin_has_occurred_flag;
    unsigned char end_has_occurred_flag
} dst_info_t;
```

The daylight saving time information contains two identical unions named begin and end. The begin union contains the information necessary to determine when daylight saving should begin going into effect by adjusting the time, and end union contains the information necessary to determine when daylight saving should end by re-adjusting the time. The unions contain two structures named absolute and generic. The type member of the struct dst_info shall be 0 for absolute or 1 for generic. The absolute structure contains the exact date and time the beginning/ending adjustment should be made, and by how many seconds the time should be adjusted. The generic structure contains information that can be valid for a number of years, by containing the month in which the beginning/ending adjustment should be made and a union named gendom (short for generic day of month), that contains the information to determine the day of the month on which the beginning/ending adjustment will take place for any particular year. The information in the generic day of month

union determines a particular day of the month by finding the specific day of the week that occurs a specific number of times before or after a specific day of the month. The `dom_type` member of the union `dst_gen_dom_union` shall be a 0, 1, or 2 determining whether the `dom` member, `dst_gen1_struct` member or `dst_gen2_struct` union member respectively is used. The `dom`, `on_after_dom`, and `on_before_dom` members specify a day of the month from 1 to 31 inclusive. The `occur` member of these structures shall be 1 or greater, determining the number of times the particular day of the week, in the `dow` member (0 – 6, 0 being Sunday) shall occur to determine the day of the month when the daylight saving adjustment shall take place.

ATC_DST_ENABLE and ATC_DST_DISABLE

These commands enable and disable daylight saving time to be in effect.

9.2.8.2.2 EEPROM

The EEPROM driver provides full capability for reading and writing to EEPROM.

Supported Device File Operations:

```
open();
close();
read();
write();
lseek();
ioctl();
```

open()

The `dev` entry for the host EEPROM shall be `/dev/eeprom`. The EEPROM can be opened for Read, Write, or Read/Write.

Examples:

```
fd = open("/dev/eeprom", O_RDONLY);
fd = open("/dev/eeprom", O_WRONLY);
fd = open("/dev/eeprom", O_RDWR);
```

close()

Closes the file descriptor.

read()

```
int read(int filp, void *buf, int count);
```

Reads up to *count* bytes into *buf* and returns the number of bytes read. The read occurs at the current position within the device.

Note: The current position can be determined using the `ioctl`. The current position can be changed using the `lseek()` function.

Possible Errors:

EIO if end of file condition has already been reached

```
write()  
int write(int filp, void *buf, int count);
```

Writes *count* bytes to the device at the current file position within the device. If all of the bytes specified by *count* cannot be written before the end of the device no bytes shall be written and an error shall be returned. The number of bytes written shall be returned. If the value returned is less than *count*, then the returned value of bytes were written correctly, but the remaining bytes contain errors. In this case it is necessary to try the write again for the remaining bytes or repeat the same write again until the number of bytes returned matches the *count*.

Possible Errors:

EIO if end of file condition would occur writing the number of bytes specified.

```
lseek()  
lseek(int fd, int pos, int type);
```

Seeks to a specified position in the device. Both absolute and relative types of seeking are supported. If relative seeking is specified the *pos* value may be positive or negative. If absolute seeking is specified the file position is assigned to the *pos* value. If seeking outside the device size is attempted an error is returned and no change to the file position takes place.

```
Type Definitions:  
ATC_EEPROM_SEEK_ABS  
ATC_EEPROM_SEEK_REL
```

```
ioctl()  
ioctl(int fd, unsigned int cmd, unsigned long param);
```

The `ioctl` function supports multiple different commands, each described separately.

```
Command Definitions:  
    ATC_EEPROM_GET_FILE_POS  
    ATC_EEPROM_GET_DEVICE_SIZE
```

```
ATC_EEPROM_GET_FILE_POS
```

Returns the current file position. The *param* value is ignored.

```
ATC_EEPROM_GET_DEVICE_SIZE
```

Returns the size of the EEPROM device in bytes. The *param* value is ignored.

9.2.8.2.3 Datakey

This driver provides full capability for manipulating Datakey devices. Datakeys of sizes as listed in Section 9.2.6 of these specifications shall be supported.

Supported Device File Operations:

```
open();  
close();  
read();  
write();  
lseek();  
ioctl();
```

```
open()
```

The dev entry for the Datakey shall be /dev/datakey. The Datakey can be opened for Read, Write, or Read/Write.

Examples:

```
fd = open("/dev/datakey", O_RDONLY);  
fd = open("/dev/datakey", O_WRONLY);  
fd = open("/dev/datakey", O_RDWR);
```

```
read()
```

```
int read(int filp, void *buf, int count);
```

Reads up to *count* bytes into *buf* and returns the number of bytes read. The read occurs at the current position within the device.

Note: The current position can be determined using the ioctl. The current position can be changed using the lseek() function.

Possible Errors:

- ENXIO if Datakey is not present
- EBUSY if the signature changes
- EIO if end of file condition has already been reached

```
write()
```

```
int write(int filp, void *buf, int count);
```

Writes *count* bytes to the device at the current file position within the device. If all of the bytes specified by *count* cannot be written before the end of the device no bytes shall be written and an error shall be returned. The number of bytes written shall be returned. If the value returned is less than *count*, then the returned value of bytes were written correctly, but the remaining bytes contain errors. In this case it is necessary to try the write again for the remaining bytes or repeat the same write again until the number of bytes returned matches the *count*.

Possible Errors:

- ENXIO if Datakey is not present
- EBUSY if the device signature changes (ie. Someone switched devices really fast)
- EIO if end of file condition would occur writing the number of bytes specified.

```
close()
```

Closes the file descriptor.

lseek()

`lseek(int fd, int pos, int type);`

Seeks to a specified position in the device. Both absolute and relative types of seeking are supported. If relative seeking is specified the *pos* value may be positive or negative. If absolute seeking is specified the file position is assigned to the *pos* value. If seeking outside the device size is attempted an error is returned and no change to the file position takes place.

Type Definitions:

`ATC_DATAKEY_SEEK_ABS`

`ATC_DATAKEY_SEEK_REL`

ioctl()

`ioctl(int fd, unsigned int cmd, unsigned long param);`

The `ioctl` function supports multiple different commands, each described separately. If the Datakey is not inserted ENXIO is returned as the error code.

Command Definitions:

`ATC_DATAKEY_GET_FILE_POS`

`ATC_DATAKEY_ERASE_ALL`

`ATC_DATAKEY_ERASE_SECTOR`

`ATC_DATAKEY_READ_PROTECT_BITS`

`ATC_DATAKEY_WRITE_PROTECT_BITS`

`ATC_DATAKEY_GET_DEVICE_SIZE`

`ATC_DATAKEY_GET_SECTOR_SIZE`

`ATC_DATAKEY_GET_FILE_POS`

Returns the current file position. The *param* value is ignored.

`ATC_DATAKEY_ERASE_ALL`

Erases all data on the Datakey. The *param* value is ignored. The CPU active light blinks with high frequency during erasure. Always returns 0.

Note: When data is erased, all values are read as 0xFF.

`ATC_DATAKEY_ERASE_SECTOR`

Erases all data in the sector containing the address specified by *param*. The CPU active light blinks at high frequency during erasure. Returns 0 on success or EINVAL on invalid address. The sector size can be determined using the appropriate `ioctl()` in order to know what address ranges will be erased by this command.

`ATC_DATAKEY_READ_PROTECT_BITS`

Returns the value of the protect bits directly read from the Datakey. The data format will be in accordance with the datasheet for the Datakey being used (not the same for different device sizes). This function is provided so the user can ensure that the device is not protected. The *param* value is ignored.

ATC_DATAKEY_WRITE_PROTECT_BITS

Writes the value specified in *param* directly to the Datakey protection byte. The data format varies in accordance with the datasheet for the Datakey being used. This function is provided primarily so that the user can remove protection if writing is being prevented.

ATC_DATAKEY_GET_DEVICE_SIZE

Returns the size of the Datakey device in bytes. The *param* value is ignored.

ATC_DATAKEY_GET_SECTOR_SIZE

Returns the sector size of the Datakey in bytes. The *param* value is ignored.

9.2.8.2.4 Constants Defined by this specification

The content of `atc_spxs.h` is displayed on this page.

```
#ifndef __ATC_SPXS_H
#define __ATC_SPXS_H

#define ATC_SPXS_WRITE_CONFIG    0
#define ATC_SPXS_READ_CONFIG    1

#define ATC_SDLC                 0
#define ATC_SYNC                 1
#define ATC_HDLC                 2

#define ATC_B1200                0
#define ATC_B2400                1
#define ATC_B4800                2
#define ATC_B9600                3
#define ATC_B19200               4
#define ATC_B38400               5
#define ATC_B57600               6
#define ATC_B76800               7
#define ATC_B115200              8
#define ATC_B153600              9
#define ATC_B614400              10
const int ATC_B[] = { 1200, 2400, 4800, 9600, 19200, 38400,
                    57600, 76800, 115200, 153600, 614400 };

#define ATC_CLK_INTERNAL         0
#define ATC_CLK_EXTERNAL        1
```

```
#define ATC_GATED                0
#define ATC_CONTINUOUS           1

typedef struct atc_spcx_config_t {
    unsigned char protocol;
    unsigned char baud;
    unsigned char transmit_clock_source;
    unsigned char transmit_clock_mode;
} atc_spxs_config;

#endif
```


The content of atc.h is displayed on the following two pages.

```
#ifndef __ATC_H
#define __ATC_H

// Device File Names
#define ATC_HOST_EEPROM_DEV "/dev/eeprom"
#define ATC_ENGINE_EEPROM_DEV "/dev/engine_eeprom"
#define ATC_DATAKEY_DEV "/dev/datakey"
#define ATC_GPIO_POWERDOWN_DEV "/dev/powerdown"
#define ATC_GPIO_DATAKEY_DEV "/dev/datakeypresent"
#define ATC_GPIO_CPUACTIVE_DEV "/dev/cpuactive"
#define ATC_GPIO_CPURESET_DEV "/dev/cpureset"
#define ATC_TIMING_TOD_DEV "/dev/tod"
#define ATC_TIMING_TIMERS_DEV "/dev/timers"

#define ATC_SP1 "/dev/sp1"
#define ATC_SP2 "/dev/sp2"
#define ATC_SP3 "/dev/sp3"
#define ATC_SP4 "/dev/sp4"
#define ATC_SP5 "/dev/sp5"
#define ATC_SP6 "/dev/sp6"
#define ATC_SP8 "/dev/sp8"

#define ATC_SP1S "/dev/sp1s"
#define ATC_SP2S "/dev/sp2s"
#define ATC_SP3S "/dev/sp3s"
#define ATC_SP4S "/dev/sp4s"
#define ATC_SP5S "/dev/sp5s"
#define ATC_SP6S "/dev/sp6s"
#define ATC_SP8S "/dev/sp8s"

// DATAKEY IOCTL CONSTANTS
#define ATC_DATAKEY_GET_FILE_POS 3
#define ATC_DATAKEY_ERASE_ALL 6
#define ATC_DATAKEY_ERASE_SECTOR 7
#define ATC_DATAKEY_READ_PROTECT_BITS 8
#define ATC_DATAKEY_WRITE_PROTECT_BITS 9
#define ATC_DATAKEY_GET_DEVICE_SIZE 10
#define ATC_DATAKEY_GET_SECTOR_SIZE 11

// DATAKEY LSEEK CONSTANTS
#define ATC_DATAKEY_SEEK_REL 0
#define ATC_DATAKEY_SEEK_ABS 1

// EEPROM IOCTL CONSTANTS
#define ATC_EEPROM_GET_FILE_POS 3
#define ATC_EEPROM_GET_DEVICE_SIZE 10

// EEPROM LSEEK CONSTANTS
#define ATC_EEPROM_SEEK_REL 0
#define ATC_EEPROM_SEEK_ABS 1

// Time of Day driver Definitions
#define ATC_TOD_SET_TIMESRC 1
```

```

#define ATC_TOD_GET_TIMESRC 2
#define ATC_TOD_GET_INPUT_FREQ 3
#define ATC_TOD_REQUEST_TICK_SIGNAL 5
#define ATC_TOD_CANCEL_TICK_SIGNAL 6
#define ATC_TOD_DST_ENABLE 10
#define ATC_TOD_DST_DISABLE 11
#define ATC_TOD_DST_SETINFO 12
#define ATC_TOD_DST_GETINFO 13

// TIMING Driver Definitions
#define ATC_TIMER_GET_STATUS      0x1C
#define ATC_TIMER_NULL           0x0000 // When timer is initialized
#define ATC_TIMER_SIG            0x1000 // If one-shot signal is
pending */
#define ATC_TIMER_CYC            0x1001 // If periodic signal is
pending */
#define ATC_TIMER_START          0x1002 // If free running
#define ATC_TIMER_STOP           0x1003 // If not active
#define ATC_TIMER_RESET          0x1004 // If timer is reset

typedef struct
{
    unsigned int value;
    unsigned int mode;
    unsigned int signal;
    unsigned int period;
} Timer_status;

typedef struct
{
    unsigned int code;
    unsigned int param1;

    union
    {
        unsigned int param;
        void __user *pointer;
    } param2;
} timing_params;

#define ATC_TIMER_SET_PARAMS      0
#define ATC_TIMER_GET_PARAMS     1

#define ATC_SET_TIMESRC 1
#define ATC_TIMESRC_LINESYNC 0
#define ATC_TIMESRC_RTCSQWR 1

typedef struct atc_datakey_t {
    unsigned int16 fcs;
    unsigned int8 type;
    unsigned int8 version;
    unsigned int32 latitude;

```

```
    unsigned int32 longitude;  
    unsigned int16 id;  
    unsigned int16 drop;  
    unsigned int32 ipaddress;  
    unsigned int32 subnet;  
    unsigned int32 gataway;  
} atc_datakey;  
  
#endif
```

9.2.8.3 Linux Application Kernel

9.2.8.3.1 Boot Sysreset

The provided software shall boot Linux from SYSRESET. The entire program shall be resident in FLASH Memory. The serial port descriptors shall be configured with the defaults parameters as listed in A9-16.

9.2.8.3.2 Hardware Initialization

The Engine Board low-level hardware and O/S software initialization shall be completed within a maximum of 4.5 seconds from the release of STARTUP/SYSRESET as shown in A9-17. This startup time shall be measured from the release of STARTUP/SYSRESET to the turn on of the ACTIVE LED using a user level program named ONLED.

9.2.8.3.3 Startup Procedure

The Linux boot image shall startup as described in the AASHTO, ITE and NEMA ATC Standard V. 5.2.b Section 5.3.5.1. The boot up process shall be completed within the time period specified in Section 9.2.8.3.2 of these specifications.

Linux startup shall be configured to auto run scripts or execute Linux binaries residing in the USB Memory upon power up with USB Memory inserted. If there is no USB Memory inserted in the Model 2070-1C Module, Linux shall boot normally as defined above.

9.2.8.4 Linux Utilities

The following Linux utilities shall be provided resident in the Model 2070-1C CPU Module:

Ver , fl, onled

A Ver utility shall be provide in the /bin directory and shall meet the requirement as defined in Section 9.2.7.6.4 of this specification and as applicable for the Linux OS.

Re-Flash (fl) utility shall be provided in the /bin directory and shall meet the requirements as defined in Section 9.2.9 of this specification and as applicable for the Linux OS.

ONLED (onled) program shall be provided in the /bin directory. The onled program shall be a Linux binary and shall toggle the ACTIVE LED when executed.

9.2.8.5 Linux Network Requirements

The following Network utilities not listed under FHS-2.3 shall be provided resident in the Model 2070-1C CPU Module:

vi, arp, telnet, ftp, ifconfig, netstat, ping, showmount, ntpdate, ntpq, ntp-time ntp-wait, and rpcinfo

The Model 2070 -1C CPU shall have full support for NFS and shall have the following daemons resident:

rpc.mountd, and rpc.nfsd

The Model 2070 -1C CPU shall have full support for FTP and shall have the following daemons resident:

vsftpd

The Model 2070 -1C CPU shall have full support for NTP and shall have the following daemons resident:

ntpd and ntpdc

9.2.8.6 Linux File System Configuration

The Model 2070-1C CPU Module Linux File System Configuration shall meet the requirements and guidelines for files, directories and utility commands as per the Filesystem Hierarchy Standard (FHS-2.3) dated January 28, 2004.

9.2.9 Re-Flash Utility

A Utility Program shall be provided that would allow the user to upgrade (re-flash) the Boot Image for the Model 2070-1A and E CPU as defined in section 9.2.7 and the Linux Kernel as defined in Section 9.2.8 for the Model 2070-1C CPU. This utility shall provide the capabilities for upgrading the Operating System and drivers when available by the manufacturer. The Utility Program shall provide the capability for the user to dynamically upgrade the Boot Image via the command prompt. The contractor shall also provide a copy in CD-ROM Memory of all files originally stored in the flash drive /f0 so that they can be reloaded as needed.

9.2.10 Communications Loading Test

The Model 2070 Controller using the Model 2070-1A and 1E CPU shall pass a Communications Loading Test consisting of Serial and Network Communications. The test shall run Sp1, Sp2, Sp3, and Sp8 at 9600 bytes per second in a continuous full duplex asynchronous/synchronous communications loop with the network stack initialized and a telnet session established for each port with standard out, in and standard error directed to the telnet session port. The test shall not exceed a maximum CPU load of 30% during test duration of 96 hours for Model 2070 -1E Module. The controller using Model -1C Module shall have a maximum CPU load of 10% for the above test and shall meet all test requirements as defined in Section 9.1.1 of the ATC v.5.2.b.

9.2.11 Diagnostic Acceptance Test (DAT)

The standard Caltrans DAT Program shall be provided resident in the 2070 Unit as the application program.

9.2.12 QPL or Purchasing Agency

Source and object Software shall be provided to the QPL or Purchasing Agency on both document listing and CD-ROM Memory. It shall provide user descriptions of test logic and reports. The Agency shall possess non- exclusive rights to this program suite.

9.2.13 Deliverables

9.2.12.1 Copies Delivery

Two copies of the following items will be provided to the purchasing AGENCY on a CD disk readable by a PC compatible computer.

1. Specific hardware memory addresses, including FLASH, SRAM, and DRAM starting addresses, shall be specified and provided. Written documentation of addresses shall be in PDF form and will have the file name of “Memory Map.pdf”
2. Copies of the vendor kernel, platform drivers and OS-9 utility executable modules.
3. Copy of all provided written manuals in PDF form.
4. RE-FLASH Utility and the procedures for its use in PDF form. The PDF documentation of the procedures shall have the file name of “Reflash Utility Procedures.pdf”.

9.2.12.2 Software Delivery

All Linux Software, **except for loadable modules**, shall be compliant to the GPL license as published by the Free Software Foundation.

CHAPTER 9-SECTION 3

MODEL 2070-2 FIELD I/O MODULE (FI/O)

9.3.1 Model 2070-2A Module

The Model 2070-2A Model shall consist of the Field Controller Unit; Parallel Input/Output Ports; other Module Circuit Functions (includes muzzle jumper); Serial Communication Circuitry; Module Connectors C1S, C11S, and C12S mounted on the module front plate; VDC Power Supply (+12VDC to +5VDC); and required software.

9.3.2 Model 2070-2B Module

The Model 2070-2B Model shall consist of the Serial Communication Circuitry, DC Power Supply, and Module Connector C12S mounted on the module front plate only.

9.3.3 Field I/O Controller Unit (FCU)

The FCU shall include a programmable microprocessor/controller unit together with all required clocking and support circuitry. **The FCU shall be provided with in-circuit re-programmability via a JTAG or BDM port.**

9.3.4 Parallel Input Ports

The Parallel Input Ports shall provide 64 bits of input using ground-true logic. Each input shall be read logic "1" when the input voltage at its field connector input is less than 3.5 VDC, and shall be read logic "0" when either the input current is less than 100 μ A or the input voltage exceeds 8.5 VDC. Each input shall have an internal pull-up to the isolated +12 VDC and shall not deliver greater than 20 mA to a short circuit to ground. **The pull-up resistance shall not be less than 10K or more than 50K Ohms.**

9.3.4.1 Parallel Output Ports

The **Parallel Output Ports** shall provide 64 bits of output. Each output written as a logic "1" shall have a voltage at its field connector output of less than 4.0 VDC. Each output written as a logic "0" shall provide an open circuit (1 Mega Ohm or more) at its field connector output. Each output shall consist of an open-collector capable of driving 40 VDC minimum and sinking 100 mA minimum. Each output circuit shall be capable of switching from logic "1" to logic "0" within 100 μ s when connected to a load of 100 K-Ohms minimum. Each output circuit shall be protected from transients of 10 \pm 2 μ s duration, \pm 300 VDC from a 1 K-Ohm source, with a maximum rate of 1 pulse per second.

9.3.4.2 Output Operation

Each output shall latch the data written and remain stable until either new data is written or the active-low reset signal. Upon an active-low reset signal, each output shall latch a **LOGIC "0"** and retain that state until a new writing. The state of all output circuits at the time of **POWER UP** or in Power Down state shall be open. It shall be possible to simultaneously assert all outputs within 100 μ s of each other. An output circuit state not changed during a new writing shall not glitch when other output circuits are updated.

9.3.5 Other Module Circuit Functions

9.3.5.1 Maximum Capacitive Load

A maximum capacitive load of 100 pF shall be presented to the LINESYNC input signal. The EIA-485 compliant differential LINESYNC signals shall be derived from the LINESYNC signal.

9.3.5.2 External WDT “Enable” Shunt/Toggle Switch

An External WDT “Enable” Shunt/Toggle Switch shall be provided on the board. With the jumper IN and NRESET transitions HIGH (FCU active), the FCU shall output a state change on Output 39 (Monitor Watchdog Timer Input) every 100 ms for 10 seconds or due to Set Output Command. When the shunt is missing, the feature shall not apply. This feature is required to operate with the Model 210 Monitor Unit only.

9.3.5.3 Watchdog Circuit

An FCU Watchdog Circuit shall be provided. It shall be enabled by the Filed I/O firmware at Power Up with a value of 100 ms. Its enabled state shall be machine readable and reported in the FI/O status byte. Once enabled, the watchdog timer shall not be disabled without resetting the FI/O. Failure of the FI/O to reset the watchdog timer within the prescribed timeout shall result in a hardware reset.

9.3.5.4 One KHz Reference

A synchronizable 1 KHz time reference shall be provided. It shall maintain a frequency accuracy of $\pm 0.01\%$ (± 0.1 counts per second).

9.3.5.5 32 Bit Millisecond Counter

A 32-bit Millisecond Counter (MC) shall be provided for “time stamping.” Each 1 KHz reference interrupt shall increment the MC.

9.3.5.6 Power Up

At Power Up, the FCU loss of communications timer shall indicate loss of communications until the user program sends the Request Module Status message to reset the “E” Bit.

9.3.5.7 Logic Switch

A LOGIC Switch shall be provided resident on the module board. The switch shall function to disconnect Serial Port 3 (SP3) from the external world, Connector C12S. Its purpose is to prevent multiple use of SP3. An LED shall be provided on the module front panel labeled “SP3 ON”. If LED light is ON, SP3 is active and available at C12S.

9.3.6 Serial Communications/Logic Circuitry

9.3.6.1 System Serial Port 5 (SP5) EIA 485 Signal

System Serial Port 5 (SP5) EIA 485 signal Lines shall enter the Field I/O Module and be split into two multi-drop isolated ports. One shall be routed to the FCU and the other converted to EIA 485, then routed to Connector C12S.

9.3.6.2 System Serial Port 3 (SP3) EIA 485 Signal

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System Serial Port 3 (SP3) EIA 485 signal lines shall enter the **Field I/O Module** and be isolated, converted back to EIA 485 and then routed to Connector C12S.

9.3.6.3 Linesync and Power Down Lines

Linesync and Power Down Lines shall be split and isolated, one routed to FCU for shut down functions and the other changed to EIA 485; then routed to connector 12S for external module use.

9.3.6.4 CPU_Reset and Power Up

CPU_Reset and Power Up (SysReset) Lines shall be isolated and “OR’d” to form NReset. NReset shall be used to reset the FCU and other module devices. NReset shall also, be converted to EIA 485, and then routed to Connector C12S.

9.3.6.5 Module 2070-2B

If the module is 2070-2B, routing to FCU doesn’t apply.

9.3.6.6 Internal Isolation

Isolation between internal +5DC / DCG#1 and +12 DC ISO/DCG#2 and +12 DC ISO shall be used for board power and external logic.

9.3.7 Buffers

A Transition Buffer shall be provided capable of holding a minimum of 1024 recorded entries. The Transition Buffer shall default to empty. There shall be two entry types: Transition and Rollover. The inputs shall be monitored for state transition. At each transition (If the input has been configured to report transition), a transition entry shall be added to the Transition Buffer. The MC shall be monitored for rollover. At each rollover transition (\$xxxx FFFF - \$xxxx 0000), a rollover entry shall be added to the Transition Buffer. For rollover entries, all bits of byte 1 are set to indicate that this is a rollover entry. Transition Buffer blocks are sent to the CPU **Module** upon command. Upon confirmation of their reception, the blocks shall be removed from the Transition Buffer.

9.3.8 I/O Functions

9.3.8.1 Inputs

Input scanning shall begin at I0 (bit 0) and **proceed to the highest input I63**, ascending from **lsb to msb in increasing input number**. Each complete input scan shall finish within 100 μ s. Once sampled, the Logic State of input shall be held until the next input scan. Each input shall be sampled 1,000 times per second. The time interval between samples shall be 1 ms \pm 100 μ s. If configured to report, each input that has transitioned since its last sampling shall be identified by input number, transition state, and timestamp (at the time the input scan began) and shall be added as an entry to the Transition Buffer. If multiple inputs change state during one input sample, these transitions shall be entered into the Input Transition Buffer by increasing number. The MC shall be sampled within 10 μ s of the completion of the input scan.

9.3.8.2 Data Filtering

If configured, the inputs shall be filtered by the FCU to remove signal bounce. The filtered input signals shall then be monitored for changes as noted. The filtering

parameters for each input shall consist of Ignore Input Flag and the On and Off filter samples. If the Ignore Input flag is set, no input transitions shall be recorded. The On and Off filter samples shall determine the number of consecutive samples an input must be on and off, respectively, before a change of state is recognized. If the change of state is shorter than the specified value, the change of state shall be ignored. The On and Off filter values shall be in the range of 0 to 255. A filter value of 0, for either or both values, shall result in no filtering for this input. The default values for input signals after reset shall be as follows:

Filtering	Enabled
On and off filter values shall be set to	5
Transition monitoring	Disabled (Timestamps are not logged)

9.3.8.3 Outputs

Simultaneous assertion of all outputs shall occur within 100 μ s. Each output shall be capable of being individually configured in state to ON, OFF, or a state synchronized with either phase of LINESYNC. The condition of the outputs shall only be "ON" if the FI/O continues to receive active communications from the CPU Module. If there is no valid communications with the CPU Module for 2.0 seconds, all outputs shall revert to the OFF condition, and the [Module Status Byte](#) shall be updated to reflect the loss of communication from the CPU Module.

9.3.8.4 Standard Function

Each output shall be controlled by the data and control bits in the CPU Module Field I/O frame protocol as follows:

Output Bit Translation

Case	Output Data Bit	Output Control Bit	Function
A	0	0	Output in the OFF state
B	1	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is OFF, and when LINESYNC is OFF (0), the output is ON.
C	0	1	Output is a square wave, synchronized to the LINESYNC signal. When LINESYNC is ON (1), the output is ON, and when LINESYNC is OFF (0), the output is OFF
D	1	0	Output is in the ON state.

9.3.8.4.1 Case A

In Case A above, the corresponding output shall be turned OFF if previously ON and if previously OFF remain OFF until otherwise configured. For half-cycle switching (cases B and C), all outputs to be changed shall be changed within 50 μ s after the corresponding LINESYNC transition and shall remain in the same state during the entire half cycle. In Case D above, the corresponding output shall be turned ON if

previously OFF and if previously ON remain ON until otherwise configured. All outputs shall neither glitch nor change state unless configured to do so.

9.3.8.5 Interrupts

All interrupts shall be capable of asynchronous operation with respect to all processing and all other interrupts. MILLISECOND Interrupt shall be activated by the 1 KHz reference once per ms. A timestamp rollover flag set by MC rollover shall be cleared only on command. **LINESYNC Interrupt - both the 0-1 and 1-0 transitions of the LINESYNC signal shall generate this interrupt.** The LINESYNC interrupt shall monitor the MC interrupt and set the MC error flag if there has not been an interrupt from the 1 KHz source for 0.5 seconds (≥ 60 consecutive LINESYNC interrupts). The LINESYNC interrupt shall synchronize the 1 KHz time reference with the 0-1 transition of the LINESYNC signal once a second. A LINESYNC error flag shall be set if the LINESYNC interrupt has not successfully executed for 0.5 seconds or longer (≥ 500 consecutive millisecond interrupts).

9.3.8.6 Communication Service Routine

A low-level communication service routine shall be provided to handle reception, transmission, and EIA-485 communication faults. The communication server shall automatically:

For Transmission:

- Generate the opening and closing flags
- Generate the CRC value
- Generate the abort sequence (minimum of 8 consecutive '1' bits) when commanded by the FCU
- Provide zero bit insertion

For Receiving:

- Detect the opening and closing flags
- Provide address comparison, generating an interrupt for messages addressed to the **Field** I/O Module, and ignoring messages not addressed to the **Field** I/O Module
- Strip out inserted zeros
- Calculate the CRC value, compare it to the received value, and generate an interrupt on an error
- Generate an interrupt if an abort sequence is received

9.3.8.7 Communication Processing

This task shall be to process the command messages received from the CPU Module, prepare, and start **the** response transmission. The response message transmission shall begin within 4 ms of the receipt of the received message. Message type processing time constraints shall not exceed 70 ms per message.

9.3.8.8 Input Processing

This task shall process the raw input data scanned in by the 1 ms interrupt routine, perform all filtering, and maintain the transition queue entries.

9.3.9 Data Communication Protocols

9.3.9.1 Communications Protocol

Protocol - All communications between the CPU Module and the Field I/O shall be SDLC-compatible command-response, support 0 bit stuffing, and operate at a data rate of 614.4 Kbps. The CPU Module shall always initiate the communications and if the command frame is incomplete or there is an error, no Field FI/O response shall be transmitted. The number of bytes of a command or response is dependent upon the Field I/O Module identification.

9.3.9.1.1 Frame Types

The frame type shall be determined by the value of the first byte of the message. The command frames type values 112 – 127 (\$70 - \$7F) and associated response frame type values 240 – 255 (\$F0 - \$FF) are allocated for **Manufacturer diagnostics**. All other frame types not called out are reserved. The command-response Frame Type values and message times shall be as follows:

Frame Types

Module Command	I/O Module Response	Description	Minimum Message Time	Maximum Message Time
0-43	128-171	Reserved for NEMA TS-2		
44-48	172-176	Reserved		
49	177	Request Module Status	250 μ s	275 μ s
50	178	MC Management	222.5 μ s	237.5 μ s
51	179	Configure Inputs	344.5 μ s	6.8750 ms
52	180	Poll Raw Input Data	317.5 μ s	320 μ s
53	181	Poll Filtered Input Data	317.5 μ s	320 μ s
54	182	Poll Input Transition Buffer	300 μ s	10.25 ms
55	183	Set Outputs	405 μ s	410 μ s
56	184	Configure Input Tracking	340 μ s	10.25 ms
57	185	Configure Complex Outputs	340 μ s	6.875 ms
58	186	Reserved / Optional (Configure Watchdog)	222.5 μ s	222.5 μ s
59	187	Controller Identification	222.5 μ s	222.5 μ s
60	188	I/O Module Identification	222.5 μ s	222.5 μ s
61-62	189-190	Reserved (see Section 9.3.9.1.2)	---	---
63	191	Poll variable length raw input (see Section 9.3.9.1.2)	317.5 μ s	320 μ s
64	192	Variable length command outputs	405 μ s	410 μ s
65	193	Reserved (see Section 9.3.9.1.2)	---	---
67	195	Reserved (see Section 9.3.9.1.2)	---	---
68-111	196-239	Reserved	---	---
112-127	240-255	Manufacturer Diagnostics	---	---

9.3.9.1.2 ITS Cabinet Monitor

Messages 61/189, and 62/190, and 65/193 are for ITS Cabinet Monitor Unit. See ITS Cabinet Monitor System Serial Bus #1 for Command and Response Frames (See Chapter 3). [Message 63 /191](#) shall be the same as Message 52/180 except Byte 2 of [Message 63](#) response shall denote the following number of input data bytes:

Message 64/192 shall be the same as Message 55/183 except Byte 2 of the Message 64 Command shall denote the number of output data bytes plus the following output control bytes:

9.3.9.2 Request Module Status

The Command shall be used to request [FI/O Module](#) status information response.

Command/response frames are as follows:

Request Module Status Command

Description	Msb							lsb	Byte Number
(Type Number = 49)	0	0	1	1	0	0	0	1	Byte 1
Reset Status Bits	P	E	K	R	T	M	L	W	Byte 2

Request Module Status Response

Description	Msb							lsb	Byte Number
(Type Number = 177)	1	0	1	1	0	0	0	1	Byte 1
System Status	P	E	K	R	T	M	L	W	Byte 2
SCC Receive Error Count	Receive Error Count								Byte 3
SCC Transmit Error Count	Transmit Error Count								Byte 4
Timestamp MSB	Timestamp MSB								Byte 5
Timestamp NMSB	Timestamp NMSB								Byte 6
Timestamp NLSB	Timestamp NLSB								Byte 7
Timestamp LSB	Timestamp LSB								Byte 8

9.3.9.2.1 Status Bits

The response Status Bits are defined as follows:

- P - Indicates FI/O hardware reset
- E - Indicates a communications loss of greater than 2 seconds
- M - Indicates an error with the MC interrupt
- L - Indicates an error in the LINESYNC
- W - Indicates that the FI/O has been reset by the Watchdog
- R - Indicates that the [SCC Receive Error](#) count byte has rolled over
- T - Indicates that the [SCC Transmit Error](#) count byte has rolled over
- K - Indicates the Datakey has failed or is not present

9.3.9.2.2 Request Module Status

Each of these bits shall be individually reset by a '1' in the corresponding bit of any subsequent Request Module Status frame, and the response frame shall report the current status bits. The SCC error count bytes shall not be reset. When an SCC error count rolls over (255 - 0), its corresponding roll-over flag shall be set.

9.3.9.3 MC Management

MC Management frame shall be used to set the value of the MC. The 'S' bit shall return status '0' on completion or '1' on error. The 32-bit value shall be loaded into the MC at the next 0-1 transition of the LINESYNC signal. The frames are as follows:

MC Management Command

Description	msb								Lsb	Byte Number
(Type Number = 50)	0	0	1	1	0	0	1	0		Byte 1
New Timestamp MSB	x	x	x	x	x	x	x	x		Byte 2
New Timestamp NMSB	x	x	x	x	x	x	x	x		Byte 3
New Timestamp NLSB	x	x	x	x	x	x	x	x		Byte 4
New Timestamp LSB	x	x	x	x	x	x	x	x		Byte 5

MC Management Response

Description	msb								Lsb	Byte Number
(Type Number = 178)	1	0	1	1	0	0	1	0		Byte 1
Status	0	0	0	0	0	0	0	S		Byte 2

9.3.9.4 Configure Inputs Command

The Configure Inputs command frame shall be used to change input configurations. The command-response frames are as follows:

Configure Inputs Command

Description	msb								Lsb	Byte Number
(Type Number = 51)	0	0	1	1	0	0	1	1		Byte 1
Number of Items (n)	n	n	n	n	n	n	n	n		Byte 2
Item # - Byte 1	E	Input Number								Byte 3(I-1)+3
Item # - Byte 2	Leading edge filter (e)									Byte 3(I-1)+4
Item # - Byte 3	Trailing edge filter (r)									Byte 3(I-1)+5

Configure Inputs Response

Description	msb								Lsb	Byte Number
(Type Number = 179)	1	0	1	1	0	0	1	1		Byte 1
Status	0	0	0	0	0	0	0	S		Byte 2

Block field definitions shall be as follows:

- E - Ignore Input Flag. "1" = do not report transitions for this input, "0" = report transitions for this input
- e - A one-byte leading edge filter specifying the number of consecutive input samples which must be "0" before the input is considered to have entered to "0" state from "1" state (range 1 to 255, 0 = disabled)
- r - A one-byte trailing edge filter specifying the number of consecutive input samples which must be "1" before the input is considered to have entered to "1" state from "0" state (range 1 to 255, 0 = disabled)
- S - return status S = '0' on completion or '1' on error

9.3.9.5 Poll Raw Input Data

The Poll Raw Input Data frame shall be used to poll the FI/O for the current unfiltered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current input status. The frames are as follows:

Poll Raw Input Data Command

Description	Msb								lsb	Byte Number
(Type Number = 52)	0	0	1	1	0	1	0	0		Byte 1

Poll Raw Input Data Response (2070-2A)

Description	msb								lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0		Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x		Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x		Bytes 3 to 9
Timestamp MSB	x	x	x	x	x	x	x	x		Byte 10
Timestamp NMSB	x	x	x	x	x	x	x	x		Byte 11
Timestamp NLSB	x	x	x	x	x	x	x	x		Byte 12
Timestamp LSB	x	x	x	x	x	x	x	x		Byte 13

Poll Raw Input Data Response (2070-8 via 2070-2B)

Description	msb								lsb	Byte Number
(Type Number = 180)	1	0	1	1	0	1	0	0		Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x		Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x		Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x		Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x		Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x		Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x		Byte 20

9.3.9.6 Poll Filtered Input Data

The Poll Filtered Input Data frame shall be used to poll the FI/O for the current filtered status of all inputs. The response frame shall contain 8 bytes (2A) or 15 bytes of information indicating the current filtered status of the inputs. Raw input data shall be provided in the response for inputs that are not configured for filtering. The frames are as follows:

Poll Filter Input Data Command

Description	Msb								lsb	Byte Number
(Type Number = 53)	0	0	1	1	0	1	0	1		Byte 1

Poll Filter Input Data Response (2070-2A)

Description	msb								lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1		Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x		Byte 2
Inputs I8 to I63	x	x	x	x	x	x	x	x		Bytes 3 to 9
Timestamp MSB	x	x	x	x	x	x	x	x		Byte 10

Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 11
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 12
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 13

Poll Filter Input Data Response (2070-8 via 2070-2B)

Description	msb								lsb	Byte Number
(Type Number = 181)	1	0	1	1	0	1	0	1		Byte 1
Inputs I0 (lsb) to I7 (msb)	x	x	x	x	x	x	x	x		Byte 2
Inputs I8 to I119	x	x	x	x	x	x	x	x		Bytes 3 to 16
Timestamp MSB	x	x	x	x	x	x	x	x		Byte 17
Timestamp NMSB	x	x	x	x	x	x	x	x		Byte 18
Timestamp NLSB	x	x	x	x	x	x	x	x		Byte 19
Timestamp LSB	x	x	x	x	x	x	x	x		Byte 20

9.3.9.7 Poll Input Transition Buffer

The Poll Input Transition Buffer frame shall poll the FI/O for the contents of the input transition buffer. The response frame shall include a three-byte information field for each of the input changes that have occurred since the last interrogation. The frames are as follows:

Poll Input Transition Buffer Command

Description	msb								lsb	Byte Number
(Type Number = 54)	0	0	1	1	0	1	1	0		Byte 1
Block Number	x	x	x	x	x	x	x	x		Byte 2

Input Transition Buffer Response

Description	msb								lsb	Byte Number
(Type Number = 182)	1	0	1	1	0	1	1	0		Byte 1
Block Number	x	x	x	x	x	x	x	x		Byte 2
Number of Entries (n)	x	x	x	x	x	x	x	x		Byte 3
Item #	S	Input Number								Byte 3(I-1)+4
Item # Timestamp NLSB	x	x	x	x	x	x	x	x		Byte 3(I-1)+5
Item # Timestamp LSB	x	x	x	x	x	x	x	x		Byte 3(I-1)+6
Status	0	0	0	0	C	F	E	G		Byte 3(n-1)+7
Timestamp MSB	x	x	x	x	x	x	x	x		Byte 3(n-1)+8
Timestamp NMSB	x	x	x	x	x	x	x	x		Byte 3(n-1)+9
Timestamp NLSB	x	x	x	x	x	x	x	x		Byte 3(n-1)+10
Timestamp LSB	x	x	x	x	x	x	x	x		Byte 3(n-1)+11

The entry types are depicted as follows:

Input Transition Entry

Description	msb								lsb	Byte Number	
Transition Entry Identifier	S	Input Number									1
Timestamp NLSB	x	x	x	x	x	x	x	x	x	2	
Timestamp LSB	x	x	x	x	x	x	x	x	x	3	

MC Rollover Entry

Description	msb								lsb	Byte Number
Rollover Entry Identifier	1	1	1	1	1	1	1	1	1	1
Timestamp MSB	x	x	x	x	x	x	x	x	x	2
Timestamp NMSB	x	x	x	x	x	x	x	x	x	3

9.3.9.7.1 Active Input

Each detected state transition for each active input (see configuration data) is placed in the queue as it occurs. Bit definitions are as follows:

- S Indicates the state of the input after the transition
- C Indicates the 255 entry buffer limit has been exceeded
- F Indicates the transition buffer limit has been exceeded
- G Indicates the requested block number is out of monotonic increment sequence
- E Same block number requested, E is set in response

9.3.9.7.2 Block Number Byte

The Block Number byte is a monotonically increasing number incremented after each command issued by the CPU Module. When the FI/O Module receives this command, it shall compare the associated Block Number with the Block Number of the previously received command. If it is the same, the previous buffer shall be re-sent to the CPU Module and the 'E' flag set in the status response frame. If it is not equal to the previous Block Number, the old buffer shall be purged and the next block of data sent. If the block number is not incremented by one, the status G bit shall be set. The block number received becomes the current number (even if out of sequence). The Block Number byte sent in the response block shall be the same as that received in the command block. Counter rollover shall be considered as a normal increment.

9.3.9.8 Set Outputs

The Set Outputs frame shall be used to command the FI/O to set the Outputs according to the data in the frame. If there is any error configuring the outputs, the 'E' flag in the

response frame shall be set to “1”. If the LINESYNC reference has been lost, the 'L' bit in the response frame shall be set to “1”. Loss of LINESYNC reference shall also be indicated in [Module Status Response Frame](#). The output bytes depend upon field I/O module. These command and response frames are as follows:

Set Outputs Command (2070-2A)

Description	Msb								lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O63 Data	x	x	x	x	x	x	x	x	x	Bytes 3 to 9
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	x	Byte 10
Outputs O8 to O63 Control	x	x	x	x	x	x	x	x	x	Bytes 11 to 17

Set Outputs Command (2070-8 via 2070-2B)

Description	Msb								lsb	Byte Number
(Type Number = 55)	0	0	1	1	0	1	1	1	1	Byte 1
Outputs O0 (lsb) to O7 (msb) Data	x	x	x	x	x	x	x	x	x	Byte 2
Outputs O8 to O103 Data	x	x	x	x	x	x	x	x	x	Bytes 3 to 14
Outputs O0 (lsb) to O7 (msb) Control	x	x	x	x	x	x	x	x	x	Byte 15
Outputs O8 to O103 Control	x	x	x	x	x	x	x	x	x	Bytes 16 to 27

Set Outputs Response

Description	Msb								lsb	Byte Number
(Type Number = 183)	1	0	1	1	0	1	1	1	1	Byte 1
Status	0	0	0	0	0	0	L	E		Byte 2

9.3.9.9 Configure Input Tracking Functions

The Configure Input Tracking Functions frame shall be used to configure outputs to respond to transitions on a specified input. Each Output Number identified by Item Number shall respond as configured to the corresponding Input Number identified by the same Item Number. Input to Output mapping shall be one to one. If a command results in more than 8 input tracking outputs being configured, the response V bit shall be set to ‘1’ and the command shall not be implemented. The command and response frames are as follows:

Configure Input Tracking Functions Command

Description	msb								lsb	Byte Number
(Type Number = 56)	0	0	1	1	1	0	0	0	0	Byte 1
Number of Items	Number of Items									Byte 2
Item # - Byte 1	E	Output Number								Byte 2(I-1)+3
Item # - Byte 2	I	Input Number								Byte 2(I-1)+4

Configure Input Tracking Functions Response

Description	msb							lsb	Byte Number
(Type Number = 184)	1	0	1	1	1	0	0	0	Byte 1
Status	0	0	0	0	0	0	0	V	Byte 2
Timestamp MSB	x	x	x	x	x	x	x	x	Byte 3
Timestamp NMSB	x	x	x	x	x	x	x	x	Byte 4
Timestamp NLSB	x	x	x	x	x	x	x	x	Byte 5
Timestamp LSB	x	x	x	x	x	x	x	x	Byte 6

9.3.9.9.1 Definitions are as follows:

- E '1' - Enable input tracking functions for this output
- '0' - Disable input tracking functions for this output
- I '1' - The output is OFF when input is ON, ON when input OFF
- '0' - The output is ON when input is ON, OFF when input is OFF
- V '1' - The max. number of 8 configurable outputs has been exceeded
- '0' - No error

Number of Items - The number of entries in the frame. If zero, all outputs currently configured for input tracking shall be disabled.

9.3.9.9.2 Timestamp Value

The timestamp value shall be sampled prior to the response frame.

9.3.9.9.3 Outputs Tracks Inputs

Outputs which track inputs shall be updated no less than once per ms. Input to output signal propagation delay shall not exceed 2 ms.

9.3.9.9.4 Number of Item

The “Number of Item” field is valid from 0 to 16 (most that is sent at one time is 8 enables and 8 disables). If processing a command resulting in more than 8 Input Tracking functions being enabled, none of the command shall be implemented and response message “V” bit set to 1. If an invalid output or input number is specified for a function, the FIO software shall not do that function definition. It shall also not be counted toward the maximum of 8 input tracking function allowed. The rest of the message shall be processed. When an Input Tracking function is disabled, the output is set according to the most recently received Set Outputs Command. When an input tracking function for an output is superseded (redefined as either another input tracking function or as a complex output function) nothing shall be done with the output. The most recent value remains until the new function changes it.

9.3.9.10 Configure Complex Output Functions

The Configure Complex Output Functions frame shall be used to specify a complex output for one to eight of any of the outputs. If a Configure Complex Output Function command results in more than eight outputs being configured, the 'V' bit in the response message shall be set to a '1', and the command shall not be implemented. Two output forms shall be provided, single pulse and continuous oscillation. These

output forms shall be configurable to begin immediately or on a specified input trigger and, in the case of continuous oscillation, to continue until otherwise configured or to oscillate only while gated active by a specified input. If the command gate bit is active, the command trigger bit shall be ignored and the specified input shall be used as a gate signal. The command and response frames are as follows:

Configure Complex Output Functions Command

Description	msb								lsb	Byte Number
(Type Number = 57)	0	0	1	1	1	0	0	1		Byte 1
Number of Items	Number of Items									Byte 2
Item # - Byte 1	0	Output Number								Byte 7(I-1)+3
Item # - Byte 2	Primary Duration (MSB)									Byte 7(I-1)+4
Item # - Byte 3	Primary Duration (LSB)									Byte 7(I-1)+5
Item # - Byte 4	Secondary Duration (MSB)									Byte 7(I-1)+6
Item # - Byte 5	Secondary Duration (LSB)									Byte 7(I-1)+7
Item # - Byte 6	0	Input Number								Byte 7(I-1)+8
Item # - Byte 7	P	W	G	E	J	F	R	L		Byte 7(I-1)+9

Configure Complex Output Functions Response

Description	msb								lsb	Byte Number
(Type Number = 185)	1	0	1	1	1	0	0	1		Byte 1
Status	0	0	0	0	0	0	0	V		Byte 2
Timestamp (MSB)	x	x	x	x	x	x	x	x		Byte 3
Timestamp (NMSB)	x	x	x	x	x	x	x	x		Byte 4
Timestamp (NLSB)	x	x	x	x	x	x	x	x		Byte 5
Timestamp (LSB)	x	x	x	x	x	x	x	x		Byte 6

9.3.9.10.1 Bit Field

The bit fields of the command frame are defined as follows:

E	'1'	- enable complex output function for this output
	'0'	- disable complex output function for this output
J	'1'	- During the primary duration, the output shall be written as a logic '1'. During the secondary duration, the output shall be written as a logic '0'.
	'0'	- During the primary duration, the output shall be written as a logic '0'. During the secondary duration, the output shall be written as a logic '1'.
		Output Number - 7-bit output number identifying outputs
		Primary Duration - For single pulse operation, this shall determine the number of 'ticks' preceding the pulse. For continuous oscillation, this shall determine the length of the inactive (first) portion of the cycle.
		Secondary Duration - For single pulse operation, this shall determine the number of 'ticks' the pulse is active. Subsequent to the secondary duration, the output shall return to the state set according to the most recently received Set Outputs command. For continuous oscillation, this shall determine the length of the active (second) portion of the cycle. 0 = hold output state until otherwise configured.
F	'1'	- The trigger or gate shall be acquired subsequent to filtering the specified input. The raw input signal shall be used if filtering is not enabled for the specified input.
	'0'	- The trigger or gate shall be derived from the raw input.
R	'1'	- For triggered output, the output shall be triggered by an ON-to-OFF transition of the specified input and shall be triggered immediately upon command receipt if the input is OFF. For gated output, the output shall be active while the input is OFF.
	'0'	- For triggered output, the output shall be triggered by an OFF-to-ON transition of the specified input and shall be triggered immediately upon command receipt if the input is ON. For gated output, the output shall be active while the input is ON.
		Input Number - 7-bit input number identifying inputs 0 Up.
P	'1'	- The output is configured for single-pulse operation. Once complete, the complex output function shall be disabled.
	'0'	- The output is configured for continuous oscillation.
W	'1'	- It is triggered by the specified input. Triggered complex output shall commence within 2 ms of the associated trigger.
	'0'	- Operation shall begin within 2 ms of the command receipt.
G	'1'	- Operation shall be gated active by the specified input.
	'0'	- Gating is inactive.
L	'1'	- The LINESYNC based clock shall be used for the time ticks.
	'0'	- The MC shall be used for the time ticks.
V	'1'	- Indicates maximum number of configurable outputs is exceeded.
	'0'	- No error
		Number of items - The number of entries in the frame. If 0, all outputs currently configured as complex outputs shall be disabled.

9.3.9.10.2 Controlling Input Signals

Controlling input signals shall be sampled at least once per millisecond.

9.3.9.10.3 Number of Items

The “Number of Items” field is valid from 0 to 16. Zero means disable all Complex Output functions. Sixteen is the maximum because the most that is sent at one time is 8 enables and 8 disables. If processing a command results in more than 8 Complex Output functions being enabled, none of the command shall be implemented and the response message “V” bit shall be set to 1. If an invalid output or input number (the “G” or “W” bits being set to 1 is specified for a function, that function definition is not done by the FIOM software. It shall also not be counted towards the maximum of 8 Complex Output functions allowed. The rest of the message shall be processed. When a Complex Output function is disabled, the output is set according to the most recently received Set Outputs command. When a complex output function for an output is superseded, that is, redefined as wither another Complex Output function, or as an Input Tracking function, nothing special is done with the output. The most recent value remains until the new function changes it. The “G” bit (gating) set to 1 takes precedence over the “W” bit (triggering). If gating is ON, triggering is turned OFF, regardless of the value of the “W” bit in the command message. If a Complex Output is configured with the “G” bit set to 1 (gating) and the “P” bit set to 0 (continuous oscillation), the output is set to OFF (0) whenever the specified input changes state so that the oscillation should cease (output inactive). For a single pulse operation (“G” bit set to 1), after the secondary duration completes the Complex Output function shall be disabled, and the output shall be set according to the most recently received Set Outputs command.

9.3.9.11 Configure Watchdog

The Configure Watchdog frames shall be used to change the software watchdog timeout value. The Command and response frames are as follows:

Configure Watchdog Command

Description	msb								lsb	Byte Number
(Type Number = 58)	0	0	1	1	1	0	1	0		Byte 1
Timeout Value	x	x	x	x	x	x	x	x		Byte 2

Configure Watchdog Response

Description	msb								lsb	Byte Number
(Type Number = 186)	1	0	1	1	1	0	1	0		Byte 1
Status	0	0	0	0	0	0	0	0	Y	Byte 2

9.3.9.11.1 Timeout Value

The timeout value shall be in the range between 10 to 100 ms. If the value is lower than 10, 10 shall be assumed. If the value is greater than 100, 100 shall be assumed.

9.3.9.11.2 Watchdog Timeout Value

On receipt of this frame, the watchdog timeout value shall be changed to the value in the message and the “Y” bit set. The response frame bit (Y) shall indicate a '1' if the watchdog has been previously set and a '0' if not.

9.3.9.12 Controller Identification

This is a legacy message command / response for FI/O modules with Datakey resident. Upon command, a response frame containing the 128 bytes of the Datakey. On NRESET transition to High or immediately prior to any interrogation of the Datakey, the FI/O shall test the presence of the Key. If absent, the FI/O Status Bit “K” shall be set and no interrogation shall take place. If an error occurs during the interrogation, Bit “K” shall be set. If “K” bit set, only the first two bytes shall be returned. The Command Response frames are as follows:

Controller Identification Command

Description	msb								lsb	Byte Number
(Type Number = 59)	0	0	1	1	1	0	1	1		Byte 1

Controller Identification Response

Description	msb								lsb	Byte Number
(Type Number = 187)	1	0	1	1	1	0	1	1		Byte 1
Status	0	0	0	0	0	0	0	K		Byte 2
Datakey	x	x	x	x	x	x	x	x		Byte 3 to 130

9.3.9.13 Module Identification

The **Field** I/O Identification command frame shall be used to request the FI/O Identification. A value Response of “1” for the 2070-2A, “2” for the 2070-8, and “3” for 2070-2N. Response values 32 to 40 are reserved for the ITS Cabinet (See Chapter 3). The command and response frames are shown as follows:

I/O Module Identification Command

Description	msb								lsb	Byte Number
(Type Number = 60)	0	0	1	1	1	1	0	0		Byte 1

I/O Module Identification Response

Description	msb								lsb	Byte Number
(Type Number = 188)	1	0	1	1	1	1	0	0		Byte 1
FI/O ID byte	x	x	x	x	x	x	x	x		Byte 2

CHAPTER 9-SECTION 4

MODEL 2070-3 FRONT PANEL ASSEMBLY (FPA)

9.4.1 Model 2070-3 Front Panel Assembly

The Model 2070-3 Front Panel Assembly shall be delivered with one of the three options as called out under Chapter 9, Section 1 or in the contract's special provisions (governs). All options shall consist of a panel with latch assembly and two TSD #1 hinge attaching devices, assembly PCB, external serial port connectors (DB9 and RJ-45), CPU_ACTIVE LED indicator, and FP Harness Interface. The options shall include the additional features, as follows:

OPTION 3A- FPA controller, two keyboards, AUX switch, alarm bell & Display A.

OPTION 3B - FPA controller, two keyboards, AUX switch, alarm bell & Display B.

OPTION 3C - System Serial Port 6 Lines, isolated and vectored to Connector C60P.

OPTION 3D- FPA controller, two keyboards, AUX switch, alarm bell & Display D

9.4.2 Keyboards

Two Keyboards shall be provided, one with sixteen keys for hexadecimal alphanumeric entry and the other with twelve keys to be used for cursor control and action symbol entry. Each key shall be engraved or embossed with its function character. Each key shall have an actuation force between 1.764 ounce and 3.527 ounce and provide a positive tactile indication of contact closure. Key contacts shall be hermetically sealed, have a design life of over one million operations, shall be rated for the current and voltage levels used, and shall stabilize within 5 ms following contact closure.

9.4.3 CPU_ACTIVE LED Indicator

The cathode of the CPU_ACTIVE LED Indicator shall be electrically connected to the CPU_ACTIVE signal and shall be pulled up to +5 VDC.

9.4.4 Display Liquid Crystal Display (LCD)

The Display shall consist of a Liquid Crystal Display (LCD), a backlight, and a contrast potentiometer control. Display A shall have 4 lines of 40 characters each with minimum character dimensions of 0.197 in. wide by 0.411 in. high and an electro-luminescent (EL) backlight. Display B shall have 8 lines of 40 characters each with minimum dimensions of 0.104 in. wide by 0.167 in. high and either LED or EL backlight. Display D shall have 16 lines of 40 characters each with minimum dimensions of 0.104 in wide by 0.167 in high and either LED or EL backlight.

9.4.4.1 Characters and Angles of Liquid Crystal Display (LCD)

Each character shall be composed of a 5x7 dot matrix with a underline row or a 5x8 dot matrix. The viewing angle of the LCD shall be optimized for direct (90°) viewing, ±35° vertical, ±45° horizontal. The LCD shall have variable contrast with a minimum ratio of 4:1. The LCD shall be capable of displaying, at any position on the Display, any of the standard ASCII characters as well as user-defined characters.

9.4.4.2 Backlight

The backlight shall be turned on and off by the Controller Circuitry. The backlight and associated circuitry shall consume no power when in off state. A potentiometer shall control the LCD contrast with clockwise rotation increasing contrast. The contrast

shall depend on the angular position of the potentiometer, which shall provide the entire contrast range of the LCD.

9.4.4.3 Cursor Display

Cursor display shall be turned ON and OFF by command. When ON, the cursor shall be displayed at the current cursor position. When OFF, no cursor shall be displayed. All other cursor functions (positioning, etc.) shall remain in effect.

9.4.5 FPA Controller

The FPA Controller shall function as the Front Panel Device controller interfacing with the CPU Module.

9.4.5.1 FPA Reset

A FPA Reset Switch shall be provided on the Assembly PCB. The momentary Control switch shall be logic OR'd with the **CPU_Reset** Line, producing a FPA Reset Output. Upon FPA Reset being active or receipt of a valid Soft Reset display command, the following shall occur:

Auto-repeat, blinking, auto-wrap, and auto-scroll shall be set to OFF.

Each special character shall be set to ASCII SPC (space).

The tab stops shall be set to columns 9, 17, 25, and 33.

The backlight timeout value shall be set to 6 (60 seconds).

The backlight shall be extinguished.

The display shall be cleared (all ASCII SPC).

The cursor display shall be turn OFF

The FPA module shall transmit a power up string through /sp6 to the CPU once power is applied to the FPA, or the FPA hardware Reset Button is pushed.

The string is "ESC [PU", hex value "1B 5B 50 55".

9.4.5.2 Key Press

When a key press is detected, the appropriate key code shall be transmitted to SP6-RxD. If two or more keys are depressed simultaneously, no code shall be sent. If a key is depressed while another key is depressed, no additional code shall be sent.

9.4.5.3 Auto Repeat

Auto-repeat shall be turned ON and OFF by command. When ON, the key code shall be repeated at a rate of 5 times per second starting when the key has been depressed continuously for 0.5 second, and shall terminate when the key is released or another key is pressed.

9.4.5.4 AUX

When the AUX Switch is toggled, the appropriate AUX Switch code shall be transmitted to the CPU.

9.4.5.5 Controller Circuitry

The controller circuitry shall be capable of composing and storing eight special graphical characters on command, and displaying any number of these characters in combination with the standard ASCII characters. Undefined characters shall be ignored. User-composed characters shall be represented in the **communication command codes on Page A9-12**. P1 represents the special character number (1-8). Pn's represent columns of pixels from left to right. The most significant bit of each Pn represents the top pixel in a column and the least significant bit shall represent the bottom pixel. A logic '1' shall turn the pixel ON. There shall be a minimum of 5 Pn's for 5 columns of pixels in a command code sequence terminated by an "f." If the number of Pn's are more than the number of columns available on the LCD, the extra

Pn's shall be ignored. P1 and all Pn's shall be in ASCII coded decimal characters without leading zero.

9.4.5.6 Character Overwrite

Character Overwrite mode shall be the only display mode supported. A displayable character received shall always overwrite the current cursor position on the Display. The cursor shall automatically move right one character position on the Display after each character write operation. When the rightmost character on a line (position 40) has been overwritten, the cursor position shall be determined based on the current settings of the auto-wrap mode.

9.4.5.7 Auto Wrap

Auto-Wrap shall be turned ON & OFF by command. When ON, a new line operation shall be performed after writing to position 40. When OFF, upon reaching position 40, input characters shall continue to overwrite position 40.

9.4.5.8 Cursor Positioning

Cursor positioning shall be non-destructive. Cursor movement shall not affect the current display, other than blinking the cursor momentarily and periodically hiding the character at that cursor position.

9.4.5.9 Blinking Characters

Blinking characters shall be supported, and shall be turned ON and OFF by command. When ON, all subsequently received displayable characters shall blink at the rate of 1 Hz with a 60% ON / 40% OFF duty cycle. It shall be possible to display both blinking and non-blinking characters simultaneously.

9.4.5.10 Tab Stops

Tab stops shall be configurable at all columns. A tab stop shall be set at the current cursor position when a SetTabStop command is received. Tab Stop(s) shall be cleared on receipt of a ClearTabStop command. On receipt of the HT (tab) code, the cursor shall move to the next tab stop to the right of the cursor position. If no tab stop is set to the right of the current cursor position, the cursor shall not move.

Tab stops shall be set based only upon the column (horizontal) position of the cursor; the row position shall be ignored. Each tab that is set shall apply to all rows of the display. In this way, tabs shall operate similarly to a typewriter or line printer. For example, if the cursor is positioned at column 21, row 3 when a Set Tab Stop command (ESC H) is received, a tab stop is placed at column 21 and applies to every row of the display. If the cursor is then positioned to column 21, row 5, and a Clear Tab Stop command (ESC[0g) is received, the tab stop on column 21 is removed and there will be no tab stop on any row of the display at that column position.

9.4.5.11 Auto Scroll

Auto-scroll shall be turned ON and OFF by command. When ON, a Line Feed or new line operation from the bottom line shall result in the display moving up one line. When OFF, a Line Feed or new line from the bottom line shall result in the top line clearing, and the cursor being positioned on the top line.

9.4.5.12 Displayable Characters

Displayable characters shall be refreshed at least 20 times per second.

9.4.5.13 Display Back Light Illuminate

The Display back light shall illuminate when any key is pressed and shall illuminate or extinguish by command. The backlight shall extinguish when no key is pressed for a specified time. This time shall be program selected by command, by a number in the range 0 to 63 corresponding to that number of 10-second intervals. A value of 1 shall correspond to a timeout interval of 10 seconds. A value of 0 shall indicate no timeout.

9.4.5.14 Command Codes

The Command Codes shall use the following conventions:

1. Parameters and Options: Parameters are depicted in both the ASCII and hexadecimal representations as the letter 'P' followed by a lower-case character or number. These are interpreted as follows:

Pn: Value parameter, to be replaced by a value, using one ASCII character per digit without leading zeros.

P1: Ordered and numbered parameter. One of a listed known parameters with a specified order and number (Continues with P2, P3, etc.)

Px: Display column number (1-40), using one ASCII character per digit without leading zero.

Py: Display line (1-4) one ASCII character

...: Continue the list in the same fashion

Values of 'h' (\$68) and 'l' (\$6C) are used to indicate binary operations. 'h' represents ON (high), 'l' represents OFF (low).

2. ASCII Representation: Individual characters are separated by spaces; these are not to be interpreted as the space character, which is depicted by SPC.
3. Hexadecimal Representation: Characters are shown as their hexadecimal values and will be in the range 00 to 7F (7 bits).

9.4.5.15 Controller Circuit

The Controller Circuit shall communicate via a SP6 asynchronous serial interface. The interface shall be configured for 38.4 Kbps, 8 data bits, 1 stop bit, and no parity.

C50 Enable Function

C50 ENABLE function when grounded by Connector C50 Pins 1 and 5 shall be brought to Connector A1 Pin B21 for the purpose of disabling the module Channel 2.

9.4.6 Front Panel

The Front Panel shall include an electronic bell to signal receipt of ^G (hex 07). The bell shall sound at 2,000 Hz, with a minimum output rating of 85 dB at a distance of 4 feet, for 350±100 ms upon receipt of ^G (hex 07). Receipt of all other characters and ESC codes shall continue during the time the bell sounds.

CHAPTER 9-SECTION 5

MODEL 2070-4 POWER SUPPLY MODULE

9.5.1 Model 2070-4 Power Supply Module

The Model 2070-4 Power Supply Module shall be independent, self contained Module, vented, and cooled by convection only. The Module shall slide into the unit's power supply compartment from the back of the Chassis and be attached to the Backplane Mounting Surface by its four TSD #3 Devices.

9.5.2 On/Off Power Switch

An "On/Off" POWER Switch, four LED DC Power Indicators, PS Receptacle POWER Connectors, and the Incoming AC Fuse protection shall be provided on the Module Front. The LED DC POWER Indicators shall indicate all required DC voltages meet the following conditions: the +5 VDC and 12 VDC are within 5% and of their nominal levels.

9.5.3 Input Protection

Two 0.5-Ohm, 10-watt wire-wound power resistors with a 0.2 μ H inductance shall be provided (one on the AC+ Line & on the AC- Line). Three 20 Joule surge arresters shall be provided between AC+ to AC-, AC+ to EG, and AC- to EG. A 0.68 μ F capacitor shall be placed between AC+ & AC- (between the resistor & arresters).

9.5.4 +5 VDC Standby Power

+5 VDC Standby Power shall be provided to hold up specified circuitry during the power down period. It shall consist of the monitor circuitry; hold up capacitors, and charging circuitry. A charging circuit shall be provided, that under normal operation, shall fully charge and float the capacitors consistent with the manufacturers' recommendations. The Hold Up power requirements shall be a minimum constant drain of 600 μ A at a range of +5 to +2 VDC for over 600 minutes.

9.5.5 Monitor Circuitry

Monitor Circuitry shall be provided to monitor incoming AC Power for Power Failure and Restoration and LINESYNC generation.

9.5.5.1 AC Fail/Power Down Output Lines

The AC Fail/Power Down Output Lines shall go Low (ground true) immediately upon Power Failure. The Lines shall transition to High within 50 ms after both Power Restoration and supply is fully recovered. The Lines shall be driven separately. The Sysreset/Powerup Output Lines shall transition to Low 525 +/-25 ms after AC Fail/Power Down transition to Low. The Lines shall transition to HIGH 225 +/- 25 ms after both Power Restoration and the supply is fully recovered. The Lines shall be driven separately.

9.5.5.2 Monitor Circuitry

The monitor circuitry shall switch the +5 VDC Standby ON immediately upon Power Failure and isolate (OFF) the line at Power Up.

9.5.5.3 60 Hz Square Wave Linesync

The 60 Hz Square Wave Linesync signal shall be generated by a crystal oscillator, which shall synchronize to the 60-Hz VAC incoming power line at 120 and 300 degrees. A continuous square wave signal shall be +5 VDC amplitude, 8.333 ms half-cycle pulse duration, and $50 \pm 1\%$ duty cycle. The output shall have drive sink capability of 16 mA. A 2 K-Ohm pull-up resistor shall be connected between the output and +5 VDC. The monitor circuit shall compensate for missing pulses and line

noise during normal operation.

9.5.5.4 Linesync

The Linesync shall continue until Sysreset transitions Low and begin then Sysreset transitions High.

9.5.6 Power Supply Requirements

Voltage	Minimum Load	Maximum Load	Load Reg.	Line Reg.	Ripple & Noise
+5 VDC	0.0 Amp	10.0 Amp	± 5%	± 1%	50mV P-P
+12 VDC Serial	0.0 Amp	0.5 Amp	± 5%	± 1%	50mV P-P
-12 VDC Serial	0.0 Amp	0.5 Amp	± 5%	± 1%	50mV P-P
+12 VDC	0.0 Amp	1.0 Amp	± 5%	± 1%	50mV P-P

9.5.6.1 Line / Load Regulation

The Power Supply Module shall meet Line/Load Regulation for input voltage range of 90 to 135 VAC, minimum and maximum loads called out in the table including ripple and noise.

9.5.6.2 Efficiency

70 % minimum.

9.5.6.3 Ripple & noise

Less than 0.2% rms, 1% peak to peak or 50 mV, whichever is greater.

9.5.6.4 Voltage Overshoot

No greater than 5 %, all outputs.

9.5.6.5 Over voltage Protection

130% Vout for all outputs.

9.5.6.6 Circuit Protection

Automatic recovery upon removal of fault.

9.5.6.7 Inrush Current

Cold Start Inrush shall be less than 25 Amperes at 115VAC.

9.5.6.8 Transient response

Output voltage back to within 1% in less than 500 μ s on a 50% Load change. Peak transient not to exceed 5%.

9.5.6.9 Holdup Time

The power supply shall supply 30 watts minimum for 550 ms after ACFAIL going LOW. The supply shall be capable of holding up the Unit for two 500 ms Power Loss periods occurring in a 1.5-second period.

9.5.6.10 Remote Sense

+5 VDC compensates 250 mV total line drop. Open sense load protection required.

CHAPTER 9-SECTION 6
UNIT CHASSIS AND MODEL 2070-5
VME CAGE ASSEMBLY

9.6.1 General

The Chassis shall consist of the metal housing, Serial Motherboard, Back-plane Mounting Surface, Power Supply Module Supports, slot card guides, Wiring Harnesses, and Cover Plate(s). All external screws shall be countersunk and shall be Phillips flat head stainless steel type. The housing shall be treated with clear chromate and the slot designation labeled on the back-plane mounting surface above the upper slot card guide. The Chassis shall be cooled by convection only. The top and bottom pieces of the housing shall be slotted for vertical ventilation.

9.6.2 Serial Motherboard

Serial Motherboard shall function as support for its connectors, A1 to A5 and FP, and as the interface between the CPU and the dedicated modules/Front Panel carrying both serial communications, logic, and power circuits. The PCB shall be multi-layered, with one layer plane assigned to DC Ground. A wiring harness PS2 shall be provided between the Model 2070-4 Power Supply and the Motherboard PCB (provide strain relief). Test points shall be provided on the FPA side of the Motherboard for PS2 lines. A wiring harness FP shall be provided, linking the Motherboard with the FPA.

9.6.3 Model 2070-5 VME Cage Assembly

MODEL 2070-5 VME Cage Assembly shall consist of 3U five slot/connector VME Cage, Front Mounting Plate, and PS1 Harness. **The VME Cage shall conform to VME Standard IEEE P1014/D12 and ANSI/VITA 1-1994 for 3U Cage.** All slot/connectors shall be A24: D16 Interface.

9.6.4 Model 2070-1A

The Model 2070 – 1A CPU Main Controller Board shall either be affixed to the Transition Board via at least four stand-off devices or mounted in a one slot VME board assembly (removable). A PS1L Harness shall be supplied with one end mating to the PS1 power supply connector and the other end mated to the MCB DIN Connector. The VME bus lines shall be terminated by a 100-Ohm resistor per line.

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CHAPTER 10
MODEL 2070 PERIPHERAL
EQUIPMENT SPECIFICATIONS

CHAPTER 10-SECTION 1
MODEL 2070-6 A & B, AE & BE ASYNC/MODEM SERIAL
COMMUNICATION MODULES

10.1.1 Fuse Isolation

A fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use.

Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse allowed.

10.1.2 Half & Full Duplex Switch

A switch shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.1.3 Circuits

Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-6x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.1.4 Modem

Each circuit shall have a common power independent Modem with the following requirements:

Modulation: Phase coherent frequency shift keying (FSK).

Data Format: Asynchronous, serial by bit.

Line & Signal Requirements: Type 3002 voice-grade, unconditioned Tone Carrier Frequencies (Transmit and Receive), MARK and SPACE: $\pm 1\%$ tolerance. The operating band shall be (half power, -3 dB) between 1.0 KHz & 2.4 KHz for 2070-6A and 9.9 KHz & 18.9 KHz for 2070-6B.

Transmitting Output Signal Level: 0, -2, -4, -6, and -8 dB (at 1.7 KHz for 2070-6A, 3.4 KHz for 2070-6AE, 14.7 KHz for 2070-6B and 28.8 KHz for 2070-6BE) continuous or switch selectable.

Receiver Input Sensitivity: 0 to -40 dB.

Receiver Bandpass Filter: Shall meet the error rate requirement specified below and shall provide 20dB/octave, minimum active attenuation for all frequencies outside the operating band.

Clear-to-Send (CTS) Delay: 11 ±3 ms.

Receive Line Signal Detect Time: 8 ±2 ms mark frequency.

Receive Line Squelch: 6.5 (±1) ms, 0 ms (OUT).

Soft Carrier Turn Off Time: 10 ±2 ms. When the RTS is unasserted; the carrier shall turn off or go to soft carrier frequency.

Modem Recovery Timer: Capable of receiving data within 22 ms after completion of transmission.

Error Rate: Shall not exceed 1 bit in 100 Kbits, with a signal-to-noise ratio of 16 dB measured with flat-weight over a 300 to 3,000 Hz band.

Transmit Noise: Less than -50 dB across 600-Ohms resistive load within the frequency spectrum of 300 to 3,000 Hz at maximum output.

Modem interface: EIA-232 Standards.

Frequencies and Data Rates:

Model	Mark Hz	Space Hz	Soft Carrier Hz	Data Rate bps
2070-6A	1200	2200	900	300 - 1200
2070-6AE	2400	4400	1800	300 - 2400
2070-6B	11200	17600	7800	300 - 9600
2070-6BE	19200	38400	13800	300 - 19200

10.1.5 Enable/Disable Feature

The 2070-6x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

10.1.6 Hot Swappable

The 2070-6x module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

CHAPTER 10-SECTION 2
MODEL 2070-7A & 7B ASYNC / SYNC
SERIAL COMM MODULE

10.2.1 Circuits

Two opto-isolated independent circuits designated circuits #1 (Channel 1) and circuits #2 (Channel 2), shall be provided. Their functions are identical, except for the CPU Serial Communications Port and external connector (circuits #1 to SP1 [or SP3] and Connector C21S and circuits #2 to SP2 [or SP4] and Connector C22S). Line drivers/receivers shall be socket or surface mounted.

The 2070-7x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.2.2 2070 -7A

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground; and drive / receive external EIA-232 devices via C21 / C22 Connectors. Connectors shall be DB-9S type.

10.2.3 2070 - 7B

Each circuit EIA -485 signal lines, (RX, TX, TXC (I), TXC (O) and RXC) and associated signal ground shall be board terminated to matching drivers/receivers; isolated both signal and ground, and drive/receiver external EIA-485 devices via C21/C22 Connectors. Connectors shall be DB-15S type.

10.2.4 LED Indicator

Each circuit signal TX and RX line shall have an LED Indicator mounted on the front plate and labeled according to function.

10.2.5 Enable/Disable Features

The 2070-7x modules shall provide circuitry to disable their Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

The 2070-7x modules shall provide circuitry to manually disable Channel 1. When Channel 1 is manually disable, the "Ch. A Disable" LED indicator shall be turn ON.

10.2.6 Hot Swappable

The 2070-7x module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

CHAPTER 10-SECTION 3 MODEL 2070-6D FIBER OPTIC MODULE

10.3.1 Model 2070-6D Fiber Optics Module

The Model 2070-6D Fiber Optics Module shall provide an RS232/485 Asynchronous communications channel. The FO Module shall be a Plug-in Card style version for the 2070 Controller. The Model 2070-6D Fiber Optics Module (FO Module) shall operate over Singlemode Fiber.

10.3.2 Mechanical/Electrical Requirements.

The Plug-in Card FO Module shall have a protective cover or enclosure.

The FO Modules card edge connector shall be fully compatible with the 2070 Controller's Modem card slot.

The Auxiliary Data port shall be a RJ45 connector.

The Serial Port shall be a RJ45 connector.

All DIP Switches shall be accessed externally without disassembly of the FO Module.

The FO Module shall be powered direct from the 2070 Controller's edge connector.

All electro/optical communications circuitry shall be implemented using digital electronics utilizing packetizing techniques, no analog circuitry or adjustable potentiometers is allowed.

10.3.3 FO Module Requirements

All Electro Optics shall be physically protected from external damage and contamination by isolating them from the FO Modules Optical Ports by means of internal replaceable mini patch-cords that connect between the Electro Optics and the Optical Bulkhead Adapters (FO Modules Optical Ports).

The FO Modules Optical Ports (Bulkhead Adapters) shall be metal and shall be ST style and interchangeable with SC and FC style connectors when required.

The Plug-in optical FO Module shall provide Optical Continuity between other FO Modules on either side should external power fail.

10.3.3.1 Network Topologies

The FO Module shall be capable of operating on Single Mode Fiber in all of the following Switch Selectable Topologies:

Self-Healing Fault Tolerant Dual Counter Rotating Rings.

Defined as 2 Fiber Rings (closed loop cable ring), one fiber transmitting data clockwise, the other fiber anti-clockwise. Every FO Module will have 4 fibers

attached to it, the incoming cable utilizes R1/T2 fiber pair and the outgoing cable utilizes T1/R2 fiber pair. Should an optical communications failure occur, such as a single or dual fiber cut or FO Module failure, the system will automatically fold back on both sides of the failure point to form a new ring and restore communications. The system shall automatically restore when there is no longer a failure point.

Single Ring.

Defined as a Single Fiber Ring (closed loop), only one fiber transmitting data clockwise. Every FO Module will have 2 fibers attached to it R1 & T1, the incoming cable utilizes R1 fiber and the outgoing cable utilizes the T1 fiber. Each fiber starts as transmit and ends as receive.

Daisy Chain.

Defined as an “open ended chain of FO Modules”. The designated Master, Auxiliary Master and Slave FO Modules may be placed anywhere in the Daisy Chain, i.e., at the beginning, at the end or anywhere in between.

The FO Module shall be immune to optical overloads thus requiring no optical attenuators.

The FO Modules optical output level shall be non-adjustable.

10.3.3.2 Modes of Operation

The FO Module shall support the following modes of operation:

Master

When the optical FO Module is set as a Master, the FO Module supervises the Slave FO Modules and provides an asynchronous, bi-directional communications channel between the Master and the Slave FO Modules.

Auxiliary Master, Co- or Remote Located Master (Disaster Recovery)

When set as an Auxiliary Master, the optical FO Module will monitor optical data transmissions from the Master, should the Master fail, the Auxiliary Master will automatically take over as a temporary Master. Control of the ring will be automatically transferred back to any optical FO Module that is designated as a Master.

Slave

When the optical FO Module is set as a Slave, the FO Module will provide repeater, drop and insert capabilities between the data ports and the optical transport layer.

Display

All FO Modules shall have a Dual Seven Segment Display that graphically indicates the switching status of the transport layer of the fiber system. Switch status information shall graphically show:

Normal Operation
Dual Ring Operation
Single Ring Operation
Daisy Chain Operation
All Optical Routing Conditions
Separate LOS Alarm indication for R1 or R2

10.3.3.3 Fiber Identification

The FO Module shall be capable of Fiber Identification by means of indicating numeral 1 or 2 on the Dual Seven Segment Display to identify which circuit the fiber belongs to.

10.3.3.4 Auxiliary Data Port

The FO Module shall have an Auxiliary Data Port with the following capabilities:

The Auxiliary Data Port shall be capable of being switched to operate as a **DCE** in parallel with the Card Edge Port; communications shall originate to and from the fiber.

The Auxiliary Data Port shall be capable of being switched to operate as a **DTE**. This permits any host attached to the card edge port to appear at the Auxiliary port as a DTE with full handshaking; communications shall originate from the card edge port to and from the auxiliary port and the fiber.

The Auxiliary Ports Carrier Detect (CD) shall be capable of being switched to operate in the following modes:

The Auxiliary Data Port is designed to emulate FSK FO Module handshaking

The Card Edge (EIA-485), Auxiliary Data Port (EIA-232) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200, 2400, 9600, 19.2Kbp/s, 38.4Kbt/s, 56Kbt/s and 115.2Kbp/s.

The RTS/CTS handshaking function shall be switch selectable:

Off position allows the FO Module to stream **transmit** data without RTS handshaking. On position requires RTS to be asserted to enable data transmission.

The Card edge and Auxiliary Data Ports shall have a switch selectable RTS to CTS Delay of 0ms and 8ms.

10.3.3.5 Anti-Streaming

The FO Module shall include a switch selectable Anti-Streaming (anti-babbling) logic control over electrical to optical signal transmission with a time out changeable by the user, the time-outs shall be switch selectable from 2, 4, 8, 16, 32 & 64 seconds, all times are additive to a max of 126 seconds.

The Anti-Streaming logic shall detect the presence of an RTS signal from the attached device. Should the transmission time from the attached device exceed the selected time, the Anti-Streaming logic will cause the CTS control line to go low, this signals the attached device to stop the transmitting data. At the same time the transmission path from the data port to the optical ring will be disconnected. The circuit will automatically reset should RTS go low and data stops babbling.

When the Anti-Streaming logic has automatically disabled the port it shall then turn on the Anti-Streaming Alarm (LED), this alarm is latched ON until manually reset.

10.3.4 Electro Optical Requirements

The FO Module Optical Transmitting Device shall use a 1310nm Singlemode Laser.

Optical Budget

The FO Module shall support a minimum of 20dB Optical budget with a maximum of 1×10^{-9} Bit Error Rate (BER).

M.T.B.F.

Shall be in excess of 100, 000 Hrs.

Optical Ports

Optical Ports shall be Metal Bulkheads, ST style, optional SC or FC.

Data Interfaces

Card Edge	EIA-485
Front Panel Serial Port	EIA-232 (RJ45 EIA 561 Pin Out)
Auxiliary Data Port	EIA-232 (RJ45 EIA 561 Pin Out)

Switch Selections are as follows:

Battery	ON or OFF
Master or Slave	Selection
Auxiliary Master	ON or OFF
Ring Topologies	Single Ring Dual Counter Rotating Ring (Self Healing) Daisy Chain

RS232 or RS422	Selection
Baud Rates	1200, 2400, 9600, 38400, 5760, 115200 bps
Parity Selections	None, Odd, Even
RTS/CTS Handshaking	ON or OFF
RTS to CTS Delay Timing	0 or 8ms
Anti Streaming	ON or OFF
Anti-Streaming Delay Times	2, 4, 8, 16, 32 & 64 seconds or any addition.
Auxiliary Port	DCE or DTE Selection

Indicators shall be Super Bright LED

TX DATA	Green	Transmit EIA-232/485 Data
RX DATA	Green	Transmit EIA-232/485 Data
ANTI- STRM	Red	Anti- Streaming
RING STATUS DISPLAY	Red	Dual Seven Segment Display
PWR Fail	Red	Dual Seven Segment Display

10.3.5 Form Factor

See A10-3 for Details

10.3.6 Power Requirements

The power requirements of the FO Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.3.7 Environmental

The FO Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 4

MODEL 2070-FX NETWORK COMMUNICATIONS MODULE

10.4.1 Model 2070-Fx Network Module

The Model 2070-Fx Module shall provide 5 ports for Network Communications to and from the Model 2070 Controller.

An integrated 5-Port Store-and-Forward Network Switch shall be used as the core for the Model 2070-Fx Module. A network port shall be used to route Ethernet Traffic across the Motherboard to the “A” Connector’s Network Lines. DC Grounding around the network connectors and lines shall be provided. The Network Lines shall be assigned as: NetP5 TX+, TX-, RX+ and RX- respectively. Two network ports shall be brought to RJ-45 Connectors on the Front Panel and two network ports shall be routed to 100Base-FX modules.

The 10/100Base-FX Module outputs shall be optically linked through short patch cords (Mini Patch Cords) to ST connectors on the Front Panel. The 10/100Base-FX modules shall operate over Single Mode Fiber.

The Model 2070-Fx Module shall be a Plug-in Card style version for the 2070 Controller.

10.4.2 Mechanical/Electrical Requirements.

The Model 2070-Fx Modules card edge connector shall be fully compatible with the 2070 Controller’s Motherboard Ax Card Slots.

The Model 2070-Fx Module shall be powered direct from the 2070 Controller’s edge connector.

10.4.3 Model 2070-Fx Module Requirements

The 10/100Base-FX modules of the Model 2070-Fx Module shall be connected by means of internal replaceable Mini Patch-Cords that connects between the 10/100Base-FX modules and the Optical Bulkhead Adapters (Model 2070-Fx Module Ports).

Model 2070-Fx Modules Optical Ports (Bulkhead Adapters) shall be metal and shall be ST style and interchangeable with SC and FC style connectors when required.

10.4.4 Network Standards

The Model 2070-Fx Module shall meet the IEEE802.3 10Base-T, IEEE 802.3u, IEEE 802.3x, 100Base-TX, and 100Base-FX Standards.

The Model 2070-Fx Module shall have 10/100Base-TX auto-negotiation on all RJ-45 ports and Auto-negotiation 10/100Mbps connection speed and Half/Full-Duplex mode on all 10/100Base-TX ports.

The Model 2070-Fx Module shall have MDIX for all 10/100Base-TX ports.

10.4.5 Modes of Operation

The Model 2070-Fx Module shall have Half/Full-Duplex mode selection on the fiber ports.

10.4.6 Network Media Support

The Model 2070-Fx Module shall be configured as a Multiple Channel Media Converter to route network traffic between the Model 2070 CPU, Two RJ-45 Front Panel Connectors and the two 10/100Base-FX Front Panel Ports.

The Model 2070-Fx Module shall support the following Media:

100Base-FX: Single-Mode fiber optic cable 9/125 μm .

100Base-TX: Cat. 5, EIA/TIA-568 100-Ohm UTP cable.

10.4.7 Electro Optical Requirements

The 10/100Base-FX Modules shall use a 1300nm Single Mode Lasers.

M.T.B.F.

Shall be in excess of 100, 000 Hrs.

Optical Ports

Optical Ports shall be Metal Bulkheads, ST style, optional SC or FC.

10.4.8 Form Factor

See A10-4 for Details

10.4.9 Power Requirements

The power requirements of the 2070-Fx Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.4.10 Environmental

The 2070-Fx Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

CHAPTER 10-SECTION 5

MODEL 2070-6W WIRELESS MODEM COMM MODULE

10.5.1 Model 2070-6W Wireless Modem

The Model 2070-6W Wireless Modem shall provide two EIA-485/ EIA-232 Asynchronous communications channels. The Model 2070-6W Wireless Modem shall be a 2070 plug-in module with EIA-232 activity LEDs on the front edge. The Model 2070-6W Wireless Modem shall convert EIA-485 data to frequency hopping spread spectrum data.

10.5.2 Circuits

Two circuits, designated Circuits #1 and Circuits #2, shall be provided. Both circuits functions shall be identical, except for Circuit #1 which shall be routed to a Spread Spectrum Radio and Circuit #2 shall routed directly to the front panel's DB-9 connector. Each circuit shall provide full isolation from the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The Model 2070-6W Wireless Modem's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.5.3 Mechanical/Electrical Requirements

The Model 2070-6W Wireless Modem shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-6W Wireless Modem shall be provided with LED indicators for as shown in details A10-5 of these specifications.

The User Serial port shall be a DB9 Female connector accessible from the front and shall be used to configure the Spread Spectrum Radio and as Serial Port Com2..

The Model 2070-6W Wireless Modem shall be powered direct from the 2070 Controller's edge connector.

The Model 2070-6W Wireless Modem shall have a MTBF of over 60,000 hours.

10.5.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200 bps, 2400 bps, 9600 bps, 19.2 Kbps, 38.4 Kbps, 56 Kbps and 115.2 Kbps.

10.5.5 Local Mode

The Model 2070-6W Wireless Modem shall be provided with a switch allowing the user to switch Com 2 into local mode. Local mode shall allow the user to perform modem configuration on the Spread Spectrum Radio. On non-local mode, Com 2 shall meet the requirements as specified for the Model 2070-7A Module as specified elsewhere in these specifications.

10.5.6 Spread Spectrum Radio

The Model 2070-6W Wireless Modem shall meet the following Spread Spectrum Radio requirements:

Frequency Range	902-928 MHz
Output Power	1mW, 10mW,100mW,1000mW
Software Programmable	Yes
Min Hop Patterns	62
Number of RF Channels	139
RF Channel Spacing	200kHs
Error Checking	16Bit-CRC
Encryption	32 Bit
Receiver Sensitivity/BER	-110dBm @ 10-6 BER
System Gain	152 dBm
Antenna Port	RP TNC-F
Certification	FCC Approved
Operation Mode	Transceiver
Error Correction	Forward Error Correction
System Configuration	Point-to-Point, Point-to-Multipoint

10.5.7 Data Interfaces

Channel 1 and 2 Model 2070 Card Edge Connector

User Serial Port EIA-232 (DB9 Female)

10.5.8 LED Indicators

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

Multiple Mini-LEDs indicating Field Strength.

10.5.9 Power Requirements

The power requirements of the Model 2070-6W Wireless Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.5.10 Environmental

The Model 2070-6W Wireless Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.5.11 Form Factor

See A10-5 Details

CHAPTER 10-SECTION 6
MODEL 2070-9A, B & E FSK/DIAL-UP MODEM COMM
MODULES

10.6.1 2070-9A, B & E Modem

The Model 2070-9x Modem shall consist of a Dial-Up and an FSK Modem. The 9x Modem Module shall be a Plug-in Card style version for the 2070 Controller.

10.6.2 Dial-Up Modem

The Dial-Up Modem shall consist of a 33.6Kbps dial-up modem meeting the V.34 AT Command set standard. The Modem shall contain two RJ-11 connectors, one designated as the Line and the second as Phone. An internal speaker shall be provided as an indicator for phone call progress. The speaker shall be controlled through AT standard commands. Front Panel LED indicators shall also be provided as shown in the A10-6 of these specifications.

10.6.2.1 Modem default configuration

The Dial-Up Modem shall contain the following default configurations:

ACTIVE PROFILE:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0
&T5 &X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:007
S08:002	S48:007
S09:006	S95:000
S10:014	

STORED PROFILE 0:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0
&T5 &X0

S00:001	S12:050
S02:043	S18:000
S06:002	S36:007
S07:050	S40:104

S08:002	S41:195
S09:006	S46:138
S10:014	S95:000
S11:095	

Profile 0 should be configured as shown above and default as the active profile on wake up. Factory default shall wake up at 2400 Baud, Parity 8, N, 1 and no handshaking.

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Dumb
2	“SMART Modem DB-9 Aux” Sel	DTE	DCE
3	RTS Override	Normal	RTS High
4	“Modem /DB9 DTE Serial” Sel	Modem	DB9-DTE

All switches shall be OPEN as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity. In SMART Mode the user shall have the ability to set the baud rate, handshaking and parity.

10.6.2.2 Modulation

The Dial-Up Modem shall use Quadrature Amplitude Modulation and Operate within the following frequencies:

Data Carrier 1800 ± 0.5 Hz
 Calling Tone 1300 ± 10 Hz
 Answering Tone 2100 ± 15 Hz

The Modem shall have Receiver Frequency Tolerance of ± 14 Hz

10.6.2.3 Modem Standards

The Dial-Up Modem shall be ITU V.90, V.34 and Rockwell V.FC compatible. It shall meet the standards:

V.90, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, V.21, Bell 212, Bell 103, V.33, V.17, V.29, V.27 ter, and V.21 Channel 2.

10.6.2.4 Data Rates

The Dial-Up Modem shall support the following data rates:

33.6Kbps, 31.3Kbps, 28.8Kbps, 26.4Kbps, 24.0Kbps, 21.6Kbps, 19.2Kbps, 16.8Kbps, 14.4Kbps, 12.0Kbps, 9.6Kbps, 7.2Kbps, 4.8Kbps, 2.4Kbps, 1.2Kbps, and 300 baud.

The Modem shall automatically select the best operating speed as indicated in Section 10.6.2.1 of these specifications.

10.6.2.5 Error Correction & Data Compression

The Modem shall use V.42 LAPM, MNP2-4 and MNP 10 for error correction and V.42 Bis, MNP 5 for Data Compression.

10.6.2.6 Tx/Rx Power Level

The transmit level shall be fixed at -11 ± 2 dB and the receiver shall have a S/N Ratio of -26 dB with a Dynamic Range of 12 dBm to -42 dBm.

The Ring detect Sensitivity shall be 38 VRMS.

10.6.2.7 Line Interface

The Dial-Up Modem shall have a Ring Equivalent of 1 Bel and a terminating Impedance of 600 Ohms. It shall have return loss of better than 14 dB.

10.6.3 FSK Modem

10.6.3.1 Fused Isolated +5 VDC

A fused isolated +5 VDC with a of 100 mA power supply shall be provided for external use.

Option – BOURNS MF – MSMD020 PTC (Positive Temperature Coefficient) Resettable Fuse allowed.

10.6.3.2 Half & Full Duplex Switch

A switch on for FSK modem shall be used to vertically switch between Half-Duplex (Down) and Full-Duplex (Up). In Half-Duplex mode, the Transmit connections shall be used for both Receive and Transmit.

10.6.3.3 Modem

The FSK modem circuit shall have meet the requirements as listed in Section 10.1.4 for the corresponding match (6A, 6B and 6BE).

10.6.3.4 Enable/Disable Feature

The FSK modem shall provide circuitry to disable Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). C50 Enable shall disable Channel 2 via disabling the RS-485 signals to and from the motherboard. The Disable line shall be pulled up on these modules.

10.6.4 Circuits

Two independent circuits designated Circuits #1 and Circuits #2, shall be provided. Both circuit functions shall be identical, except for their Serial Communications Port and external connector (Circuits #1 to SP1 [or SP3] and C2S Connector and Circuits #2 to SP2 [or SP4] and C20S Connector). Circuits #1 & #2 shall optically isolate the FSK, C2 and C20 Serial Ports from the Motherboard SP EIA-495 signals. Each circuit shall provide full isolation from each other and the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-9x module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

10.6.5 Hot Swappable

The 2070-9x module shall be "Hot" swappable without damage to its circuitry or operations. A communication "glitch" occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

10.6.6 Power Requirements

The power requirements of the Model 2070-9x Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.6.7 Environmental

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The Model 2070-9x Modem shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.6.8 Form Factor
See A10-6 for Details

CHAPTER 10-SECTION 7

MODEL 2070-6E SERIAL 2 NETWORK COMM MODULE

10.7.1 Model 2070-6E Serial 2 Network Module

The Model 2070-6E Serial 2 Network (S2NET) Module shall provide two EIA-485/EIA-232 Asynchronous communications channels. The Model 2070-6E S2NET Module shall be a 2070 plug-in module with EIA-232 activity LEDs on the front edge. The Model 2070-6E S2NET Module shall communicate over standard IEEE 802.3 networks using both TCP (point-to-point) and UDP (point-to-multipoint) protocols.

10.7.2 Circuits

Two circuits, designated Circuits #1 and Circuits #2, shall be provided. Both circuits functions shall be identical, except for Circuit #1 which shall be routed to the terminal server and Circuit #2 shall routed directly to the front panel's DB-9 connector. Each circuit shall provide full isolation from the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The Model 2070-6E S2NET Module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less. The EIA-232 drivers to the external connectors must be capable of supporting a minimum of 115,200 bits per second.

Each circuit shall convert its EIA-485 signal lines (RX, TX, RTS, CTS and DCD) to/from board TTL Level Signals; isolate both signal and ground.

10.7.3 Mechanical/Electrical Requirements

The Model 2070-6E S2NET Module shall be designed to fit in a single slot of a Model 2070 Controller.

The Model 2070-6E S2NET Module shall be provided with LED indicators for 10/100 and Half/Full Duplex Network Communications.

The User Serial port shall be a DB9 Female connector accessible from the front.

The Network port shall be a RJ45 modular jack connector accessible from the front. DIP switches shall be externally accessible.

The Model 2070-6E S2NET Module shall be powered direct from the 2070 Controller's edge connector.

10.7.4 Functional Requirements.

The Card Edge (EIA-485) and the Serial Ports front panel connector (EIA-232) shall operate Asynchronous communications and shall encompass all ITS standard rates of 1200 bps, 2400 bps, 9600 bps, 19.2 Kbps, 38.4 Kbps, 56 Kbps and 115.2 Kbps.

The Model 2070-6E S2NET Module Network Interface shall meet IEEE 802.3 and ANSI 8802-3 Standards and support 10/100 Mbps.

10.7.5 Echo Mode

The Model 2070-6E S2NET Module shall provided with a switch allowing the user to switch module into Echo Mode. In Echo Mode communications from the external network shall be routed serially to the DB-9 on the front panel. An LED indicator shall be provided to indicate the Echo Mode communications.

10.7.6 Network Configuration

The Model 2070-6E S2NET Module shall support the following features:

Provide TCP and UDP over IP protocol communications.

Subnet masks for Class A, B, and C networks (see table below):

NETWORK CLASS	HOST BITS	Subnet Mask	Example IP Address
A	24	255.0.0.0	10.0.0.100
B	16	255.255.0.0	172.31.0.100
C	8	255.255.255.0	192.168.0.100

Allow Manual or Automatic TCP/IP socket connections configuration.

Provide Telnet access for both configuration and communications.

Provide Dumb Terminal access using a User Serial port for configuring network parameters.

Provide the Ability to adjust packet size and packing algorithm.

The Model 2070-6E S2NET Module shall be provided with a Web-Based-Interface (WBI). The WBI shall allow the user to set Network Configuration Parameters and Serial Settings using a Web Browser.

10.7.7 Data Interfaces

Channel 1 and 2 Model 2070 Card Edge Connector

User Serial Port EIA-232 (DB9 Female)

Ethernet Data Port RJ45 EIA 568B Pin Out

10.7.8 LED Indicators

RTS Green or Red: DTE Request to Send

CTS Green or Red: Network Clear to Send

TXD Green or Red: DTE Transmit EIA-232 Data

RXD Green or Red: DTE Receive EIA-232 Data

DCD Green or Red: Network Data

10.7.9 Power Requirements

The power requirements of the Model 2070-6E S2NET Module be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.7.10 Environmental

The Model 2070-6E S2NET Module shall operate within the specifications listed in Chapter 1 Section 1.8.4.

10.7.11 Form Factor

See A10-7 for Details

**CHAPTER 10-SECTION 8
MODEL 2070-9D DIAL-UP MODEM COMM MODULE**

10.8.1 2070-9D Modem

The Model 2070-9D Modem shall consist of a Dial-Up Modem and shall be a Plug-in Card style version for the 2070 Controller.

10.8.2 Dial-Up Modem

The Dial-Up Modem shall consist of a 33.6Kbps dial-up modem meeting the V.34 AT Command set standard. The Modem shall contain two RJ-11 connectors, one designated as the Line and the second as Phone. An internal speaker shall be provided as an indicator for phone call progress. The speaker shall be controlled through AT standard commands. Front Panel LED indicators shall also be provided as shown in the A10-8 of these specifications.

10.8.2.1 Modem default configuration

The Modem shall contain the following default configurations:

ACTIVE PROFILE:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0 &Y0

S00:001	S11:095
S01:000	S12:050
S02:043	S18:000
S03:013	S25:005
S04:010	S26:001
S05:008	S36:007
S06:002	S38:020
S07:050	S46:007
S08:002	S48:007
S09:006	S95:000
S10:014	

STORED PROFILE 0:

B1 E1 L1 M1 N0 Q0 T V1 W0 X4 Y0 &C1 &D0 &G0 &J0 &K0 &Q5 &R1 &S0 &T5 &X0

S00:001	S12:050
S02:043	S18:000

S06:002	S36:007
S07:050	S40:104
S08:002	S41:195
S09:006	S46:138
S10:014	S95:000
S11:095	

Profile 0 should be configured as shown above and default as the active profile on wake up. Factory default shall wake up at 2400 Baud, Parity 8, N, 1 and no handshaking.

The Modem shall have a switch (S1) and shall be factory configured as follows:

	S1 DESCRIPTION	OPEN	CLOSE
1	Modem Select	Smart Modem	Dumb
2	“SMART Modem DB-9 Aux” Sel	DTE	DCE
3	RTS Override	Normal	RTS High
4	“Modem /DB9 DTE Serial” Sel	Modem	DB9-DTE

All switches shall be OPEN as factory default except for position #2, which shall be closed as default. User shall be able to disable the SMART Modem Mode and set user baud rate, handshaking, and parity. In SMART Mode the user shall have the ability to set the baud rate, handshaking and parity.

10.8.2.2 Modulation

The Dial-Up Modem shall use Quadrature Amplitude Modulation and Operate within the following frequencies:

Data Carrier 1800 ± 0.5 Hz
 Calling Tone 1300 ± 10 Hz
 Answering Tone 2100 ± 15 Hz

The Modem shall have Receiver Frequency Tolerance of ± 14 Hz

10.8.2.3 Modem Standards

The Dial-Up Modem shall be ITU V.90, V.34 and Rockwell V.FC compatible. It shall meet the standards:

V.90, V.34, V.32 bis, V.32, V.22 bis, V.22A/B, V.23, V.21, Bell 212, Bell 103, V.33, V.17, V.29, V.27 ter, and V.21 Channel 2.

10.8.2.4 Data Rates

The Dial-Up Modem shall support the following data rates:

33.6Kbps, 31.3Kbps, 28.8Kpbs, 26.4Kbps, 24.0Kbps, 21.6Kbps, 19.2Kbps, 16.8Kbps, 14.4Kbps, 12.0Kbps, 9.6Kpbs, 7.2Kpbs, 4.8Kpbs, 2.4Kpbs, 1.2Kpbs, and 300 baud.

The Modem shall automatically select the best operating speed as indicated in Section 10.6.2.1 of these specifications.

10.8.2.5 Error Correction & Data Compression

The Modem shall use V.42 LAPM, MNP2-4 and MNP 10 for error correction and V.42 Bis, MNP 5 for Data Compression.

10.8.2.6 Tx/Rx Power Level

The transmit level shall be fixed at -11 ± 2 dB and the receiver shall have a S/N Ratio of -26 dB with a Dynamic Range of 12 dBm to -42 dBm.

The Ring detect Sensitivity shall be 38 VRMS.

10.8.2.7 Line Interface

The Dial-Up Modem shall have a Ring Equivalent of 1 Bel and a terminating Impedance of 600 Ohms. It shall have return loss of better than 14 dB.

10.8.3 Circuit

The Model 2070-9D shall be provided with full isolation from the Model 2070 Motherboard. Line drivers/receivers shall be socket or surface mounted.

The 2070-9D module's isolation circuitry shall be capable of reliably passing a minimum of 1.0 Mbps. The EIA-485 drivers to the external connectors must be capable of

supporting either two times the maximum applicable baud rate for the port or 1Mbps, which ever is less.

10.8.4 Hot Swappable

The 2070-9 D Module shall be “Hot” swappable without damage to its circuitry or operations. A communication “glitch” occurring during insertion/removal is acceptable since the application program should be able to recover/retry. Power-on and hot-swap current surges shall not exceed a 10 ms surge at three times (3x) the maximum rating of each voltage supply used by the module.

10.8.5 Power Requirements

The power requirements of the Model 2070-9D Modem shall be within the power limitations of the Model 2070 UNIT as describe elsewhere in this specifications.

10.8.6 Environmental

The Model 2070-9D Modem shall operate within the specifications listed in Chapter 1 [Section 1.8.4](#).

10.8.7 Form Factor

See A10-8 for Details

CHAPTER 10-SECTION 9 2070 COMM MODULE DETAILS

	Appendix
10.9.1 Model 2070-6, ASYNC-Modem Serial Comm	A10-1
10.9.2 Model 2070-7, ASYNC / SYNC Serial Comm	A10-2
10.9.3 Model 2070-6D, Fiber Optics Modem Comm Module	A10-3
10.9.4 Model 2070-Fx, Fiber Optics Network Comm Module	A10-4
10.9.5 Model 2070-6W, Wireless Modem Comm Module	A10-5
10.9.6 Model 2070-9, FSK/Dial-Up Modem Comm Module	A10-6
10.9.7 Model 2070-6E, Serial 2 Network Comm Module	A10-7
10.9.8 Model 2070-9D, Dial-Up Modem Comm Module	A10-8

CHAPTER 11
2070 / NEMA STANDARD
CONTROLLER UNITS

CHAPTER 11-SECTION 1 NEMA 2070

11.1.1 2070 / NEMA Standard Controller Units

This specification covers two versions of 2070 / NEMA Standard Controller Units. The versions associate with NEMA [TS1/TS2 Type 2](#) and NEMA TS2 Type 1 Standards. They are as follows:

Model 2070 (V or L) N1 Controller Unit ([TS1/TS2 Type 2](#))

Model 2070 (V or L) N2 Controller Unit ([TS2 Type-1](#))

11.1.2 N1 Unit Consisting

The Model 2070 (V or L) N1 Controller Unit consists of:

Unit Chassis

2070- 1A or 1B CPU Module

2070-2B Field I/O Module

2070-3B Front Panel Module

[2070-4NA Power Supply Module](#)

2070-5 VME Cage Assembly, if required)

2070-8 Field I/O Module

11.1.3 N2 Unit Consisting

The MODEL 2070 (V or L) N2 CONTROLLER UNIT consists of:

Unit Chassis

2070-1A or 1B CPU Module

2070-2N Field I/O Module

2070-3B Front Panel Module

2070-4N (A or B) Power Supply Module

2070-5 VME Cage Assembly, if required)

11.1.4 Address

The Serial Port 5 Frame Address for 2070-2N and 2070-8 shall be “20”.

CHAPTER 11-SECTION 2 2N FIELD IO MODULE

11.2.1 2070-2N Field I/O Module

The 2070-2N Field I/O Module provides a TS2 Type 1 compatible SDLC interface via 2070 Serial Port 3, AC Power to the 2070 Unit and Fault Monitor LOGIC Output via SP5 on output O78 (similar to the 2070-8) to the NEMA TS2 Malfunction Management Unit (MMU). The communications timeout operation shall function in a manner similar to the 2070-8 (see sections 11.4.11.6 and 11.4.11.7 for details)

11.2.2 Requirements Exceptions

The Module shall meet the 2070-2A Module Requirements with the following exceptions:

No C1, C11 and C12 Connectors on the front panel of the module

No 64 inputs / 64 outputs requirements

Serial Port 5 routed to the FCU MPU Device only

Serial Port 3 shall not have a disabling switch

No Watchdog output

No Muzzle Shunt

11.2.3 Types

The module shall be a 4X type board/front panel with three connectors. The connectors are 10 Pin Connector A, a NEMA 5-15 Receptacle and a Port 1 DA-15S connector labeled as either "C15S" or "Port 1". The Port 1 (C15S) connector shall be a 15 pin metal shell DA-15 connector with female contacts. The connector shall be equipped with latching blocks and shall intermate with a 15 pin D type connector, Amp Incorporated part number 205206-1, or equivalent, which is equipped with spring latches, Amp Incorporated part number 745012-1, or equivalent.

11.2.4 Power

Incoming 2070 AC Power is derived from Connector A Pin C (AC+), Pin A (AC-), and Pin H (Equipment Ground). The power is directly routed to the NEMA 5-15 Receptacle with equipment ground also connected to the face plate. Connector A shall intermate with a NEMA TS2 Type 1 (MS3106()-18-1S) cable.

11.2.5 Isolation

The module shall isolate 2070 Serial Port 3 from the A3 Connector and reconvert the lines to external EIA 485 drivers/receivers which shall be terminated at C15S Connector. The Port shall be clocked at 153.6 Kbps.

11.2.6 FCU Output

An FCU output shall drive an open collector transistor whose output shall be routed to Connector A Pin F for use as a FAULT MONITOR Output. The transistor shall be capable of sinking 200 mA at 30 VDC.

11.2.7 Connectors A, C15S pin out and functions

Connectors A and C15S pin_out and functions are as follows:

CONNECTOR A

Pin	Function	Pin	Function	Pin	Function
A.	AC Neutral	E.	NA	I.	NA
B.	NA	F.	Fault Monitor	J.	NA
C.	AC Line	G.	DCG #2		
D.	NA	H.	EG (Equip Ground)		

CONNECTOR C15S:

Pin	Function	Pin	Function	Pin	Function
1	SP3TXD+	6	DCG #2	11	SP3TXC-
2	DCG #2	7	SP3RXC+	12	EG (Equip Ground)
3	SP3TXC+	8	DCG #2	13	SP3RXD-
4	DCG #2	9	SP3TXD-	14	NA
5	SP3RXD+	10	Port 1 Disable	15	SP3RXC-

11.2.8 Serial Port 3

Serial Port 3 shall control the TS2 BIU Units using SDLC Protocol that meets the NEMA TS2 Type 1 Frame Command / Response Standards. SP3DCD shall be allocated to Port 1 Disable where 0 VDC input on C15S pin 10 equals DCD inactive (False). SP3DCD shall be opto-isolated from Port 1 Disable.

CHAPTER 11-SECTION 3 4N (A OR B) POWER SUPPLY MODULE

11.3.1 2070-4N Power Supply Module

The 2070-4N Power Supply Module supports the NEMA TS 1 and TS2 Standards. The module is identical to the [2070-4A](#) Power Supply Requirements except for the following:

The power cord shall have a 15 inch \pm 1 inch length as measured from the panel to the plug tips.

The AC Power Fail voltage shall be 85VAC \pm 2VAC.

The AC Power Restore voltage shall be 90VAC \pm 2VAC.

The [2070-4N \(A\)](#) power supply shall have proper marking Example “[2070 4N \(A \)](#)”. A permanent sticker shall be an acceptable marking method.

CHAPTER 11-SECTION 4 MODEL 2070- 8 FIELD I/O MODULE

11.4.1 Module Consisting

The Module shall consist of the Module Chassis, Module Power Supply, FCU Controller, Parallel Input/Output Ports, Serial Communications Circuits and Module Connectors. The Module CHASSIS shall be made of 0.06 in. minimum aluminum sheet and treated with clear chromate. All external screws, except where called out, shall be countersunk and shall be Phillips flat head stainless steel. The matching nuts shall be permanently captive on the mating surfaces.

11.4.2 Module Front Panel

The Module Front Panel shall be furnished with the following:

1. ON/OFF POWER Switch mounted vertically with ON in the UP position.
2. LED DC Power Indicator. The indicator shall indicate that the required + 5 VDC is within 3% and the +24 VDC is within 8%.
3. Incoming VAC fuse protection.
4. Two DB-25S COMM connectors labeled "EX1" & "EX2."
5. Four NEMA Connectors A, B, C, & D.

11.4.3 Label

A permanent Label shall be affixed to the Front Panel. The label shall display the unit's serial number. The number shall be permanent and easy to read.

11.4.4 Module Power Supply

A Module Power Supply shall be provided and located on the right side of the module as viewed from the front. The supply shall provide the necessary module internal circuitry DC power plus 2.0 Amperes minimum of +24 VDC for external logic, detector inputs, and output load control. The supply shall meet the following requirements:

11.4.4.1 Input Protection

Specification 9.5.3 Input Protection

11.4.4.2 Power Supply Requirements

The Power Supply shall meet the specification as listed in Section 9.5.6 Power Supply Requirements except Spec 9.5.3.

11.4.4.3 Tolerances

DC Voltage tolerances shall be $\pm 3\%$ for 5 VDC and $\pm 8\%$ for 24 VDC.

11.4.5 Incoming AC Power

The supplied Incoming AC Power shall be derived from Connector A Pins "p" (AC+) and "U" (AC Neutral). External +24 VDC shall be at Connector A, Pin "B" and Connector D Pin "NN." AC Power for the 2070 receptacle shall be tapped off from the secondary side of the ON Switch / Fuse configuration.

11.4.6 Module PC Boards

All Module PC Boards shall be mounted vertically.

11.4.7 POWERDOWN, NRESET, and LINESYNC

POWERDOWN, NRESET, and LINESYNC are incoming EIA-485 differential signals and shall be routed to the module via C12S Connector. The state of the module output ports at the time of POWERDOWN transition to LOW State and until NRESET goes HIGH shall be an open circuit.

11.4.8 Requirements

The Module shall meet all requirements under CHAPTER 9 SECTION 3 with the following exceptions:

11.4.8.1 Parallel Ports

118 Bits of Input and 102 bits of Output shall be provided. Specification for inputs applies except the voltage is +24 in lieu of +12, Ground False ("0") exceeds 16.0 VDC, and Ground True ("1") is less than 8.0 VDC.

11.4.8.2 Serial Communication Circuitry

The module shall interface with the 2070-2B Field I/O module via HAR 1 Harness meeting EIA-485 Requirements. HAR 1 Harness shall be 23 lines minimum with a C12P Connector on one end and soldered with strain relief on the other. In addition to SP5 being routed to the FCU Controller interface, the SP3 EIA-485 Signal lines shall be routed only to the EX1 Connector.

11.4.9 EIA-232 Serial Port

An EIA-232 Serial Port on the FCU shall be provided with baud rate selection by Shunt of 0.3, 1.2, 2.4, 4.8, 9.6, 19.2, & 38.4 Kbps asynchronous and shall be connected at EX1 Connector. This hardware is provided for future expansion capability and its use/protocol is currently undefined.

11.4.10 HAR 2 Harness

A 22-line minimum HAR 2 Harness shall be provided between EX2 Connector and Model 2070-6 Serial COMM Module in the 2070 UNIT. This provides two Modems or EIA-232 Interfaces between the 2070 UNIT and the outside world. The two EG (Equipment Ground) lines within HAR 2 shall be connected between EX2 and the 2070-8 module chassis.

11.4.11 Fault and Voltage Monitor Circuitry

NEMA TS1 Controller Fault and Voltage Monitor functions (outputs to cabinet monitor) shall be provided.

11.4.11.1 OR Gates

Conceptually, two 3-input OR gates shall be provided. The gate 1 output shall be connected to Connector A, Pin A (Fault Monitor) and gate 2 output shall be connected to Connector A, Pin C. Any False state input shall cause a gate output False (+24VDC) state.

11.4.11.2 FCU Output O78

The FCU output O78 shall normally change its state every 100 ms. A module Watchdog circuit shall monitor the output. No state change for 2 ± 0.1 seconds shall cause the circuit output to generate a FALSE (+24 VDC) output (input to gates 1 and 2). Should the FCU begin changing state, the Watchdog output shall return to TRUE (0 VDC) state.

11.4.11.3 Operation

The module shall have a +5 VDC monitoring circuit which monitors the module's +5 VDC (± 0.25). If the voltage exceeds the limits, the circuit output shall generate a False output (input to gates 1 and 2). Normal operation shall return the output state to TRUE state.

11.4.11.4 Microprocessor Output

The FCU microprocessor output shall be assigned to FAULT Monitor (input to gate 1) and another output shall be assigned to VOLTAGE Monitor (input to gate 2).

11.4.11.5 Message Outputs

CPU Port 5 Set Output Command Message Outputs O78 and O79 shall be assigned to FAULT (O78) and VOLTAGE (O79). The bit logic state "1" shall be FCU output FALSE.

11.4.11.6 CPU / FCU Operations

CPU / FCU operation at POWER UP shall be as follows:

1. FCU Comm Loss Flag set. FAULT and VOLTAGE MONITOR outputs set to FALSE state.
2. CPU REQUEST MODULE STATUS COMMAND Message with "E" bit set is sent to FCU to clear Comm Loss Flag and FCU responds to CPU with "E" bit reset.
3. Before the Comm Loss timer expires, the SET OUTPUT COMMAND data must be sent. In that data, the 078 and 079 logically set to "0" will cause the FCU microprocessor port pins assigned for FM and VM outputs to go to their TRUE state. At this point, the signal outputs defined in the message will be permitted at the output connectors. Any number of other messages may be sent between the MODULE STATUS COMMAND and SET OUTPUTS COMMAND.
4. * If the above message sequence is not followed, Comm Loss Flag shall be set (or remain) and VM & FM shall retain the FALSE output state.
5. Performs items 2 & 3 above User Software.

11.4.11.7 CPU / FCU Communications

A CPU / FCU Communications Loss during normal operation shall cause all outputs to go blank (FALSE state) and shall set the Comm. Loss Flag. FM and VM outputs shall be in FALSE state.

**CHAPTER 11-SECTION 5
2070N1 DETAILS**

11.5.1 Front View	Appendix
11.5.2 Side View	A11-1
11.5.3 ISO View	A11-2
11.5.4 2070-8 Field I/O Module, Connector A & B	A11-3
11.5.5 2070-8 Field I/O Module, Connector C & D	A11-4
11.5.6 2070-8 Field I/O Module, EX1 & EX2 Connectors	A11-5
11.5.7 2070-2N Field I/O Module	A11-6
	A11-7

***Notes: Module sheet metal tolerance shall be 0.015 inch or less.**

APPENDIX A
CHAPTER DETAILS

**APPENDIX A1
CHAPTER 1 DETAILS**

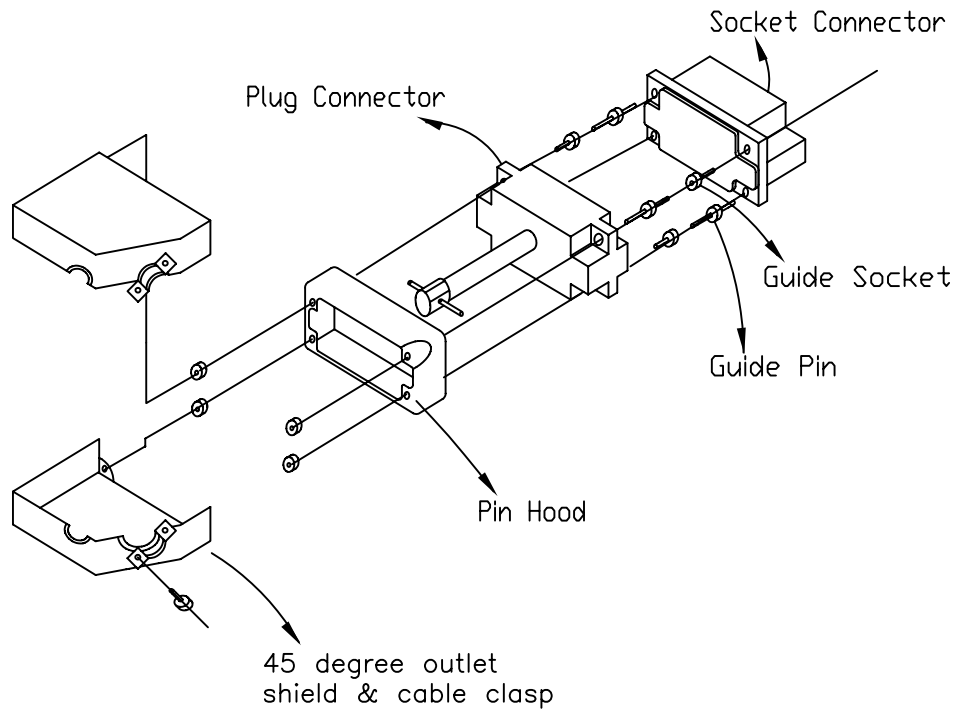
M104 – Connector	A1-1
M14 – Connector	A1-2
M50 & Circular Plastic Connectors	A1-3
M14S- Serial Connector	A1-4

Section Notes:

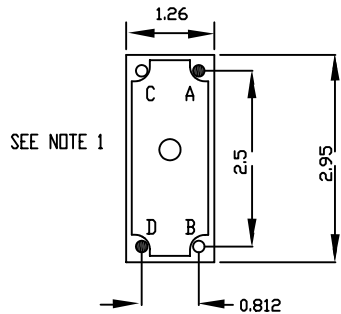
M Type connector blocks shall be constructed of phenolic or equal and shall have an insulation resistance of 5000 MegaOhms. The contacts shall be secured in the blocks with stainless steel springs.

M Type connector corner guides shall be stainless steel. The guide pins shall be 27.86 in length and the guide sockets shall be 15.66 in length.

Circular plastic connectors shall have quick connect / disconnect capability and thread assist positive detent coupling. The connectors shall be UL listed glass-filled nylon, 94 V-I rated, heat stabilized and fire resistant.

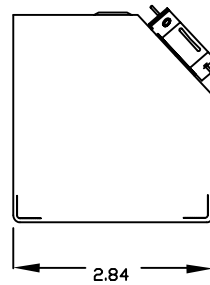
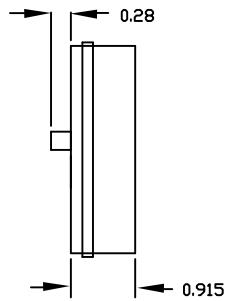


M104 CONNECTOR C1 DETAIL

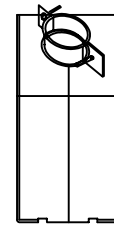


SEE NOTE 1

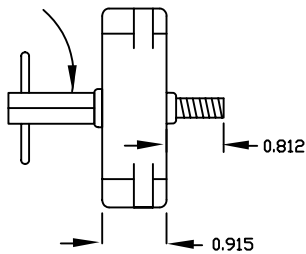
M104 SOCKET CONNECTOR



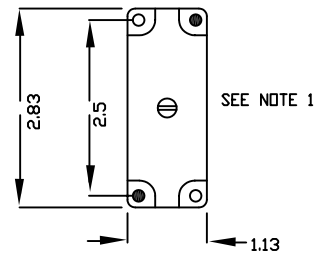
M104 SHIELD



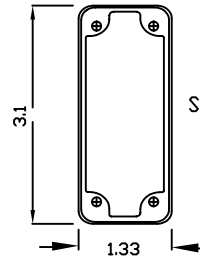
T-Handle Screw Fastener



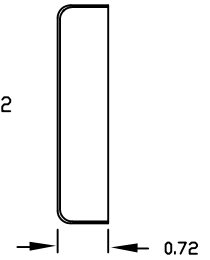
CONNECTOR C1P



SEE NOTE 1



SEE NOTE 2

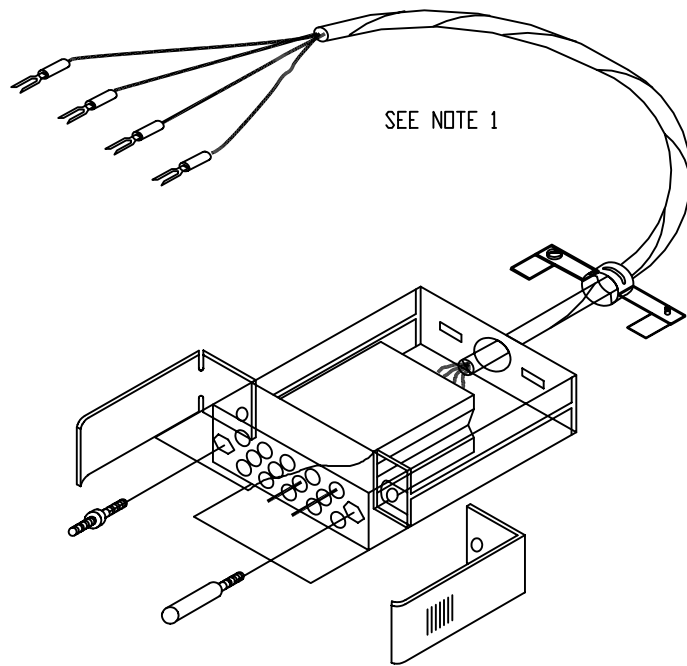


M104 HOOD

NOTES:

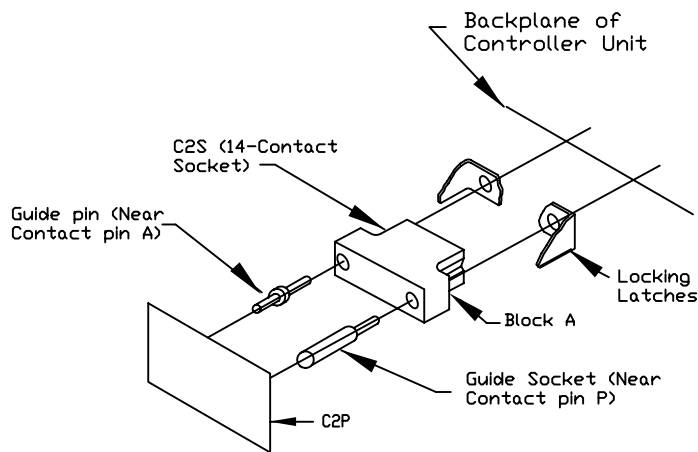
1. The darker circles denote guide pin location and the open circles are guide sockets.
2. Provide clearance for M104 plug with hood when mounting to its socket.
3. All dimensions shown are in inches.

TITLE:		CONNECTOR DETAIL-M104
NO SCALE		A1-1
TEES 2009		

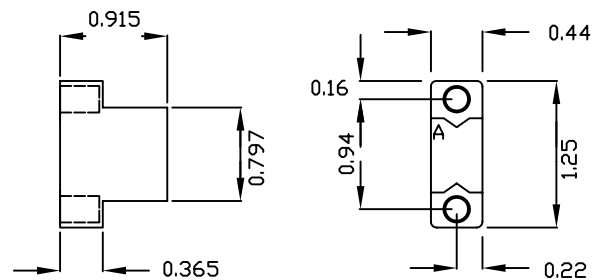


C2P MODEM INTERCONNECT HARNESS

C2P CONNECTOR ASSIGNMENT		
PIN	FUNCTION	WIRE COLOR
A	AUDIO IN	WHITE
B	AUDIO IN	BLACK
C	AUDIO OUT	RED
E	AUDIO OUT	GREEN



CONNECTOR C2 DETAIL

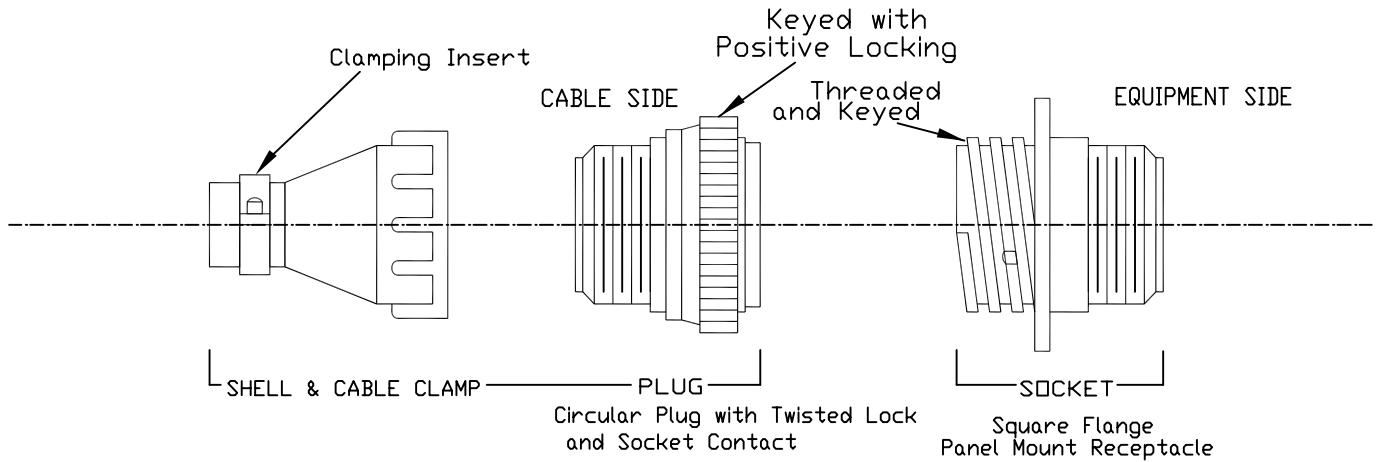


CONNECTOR C2S

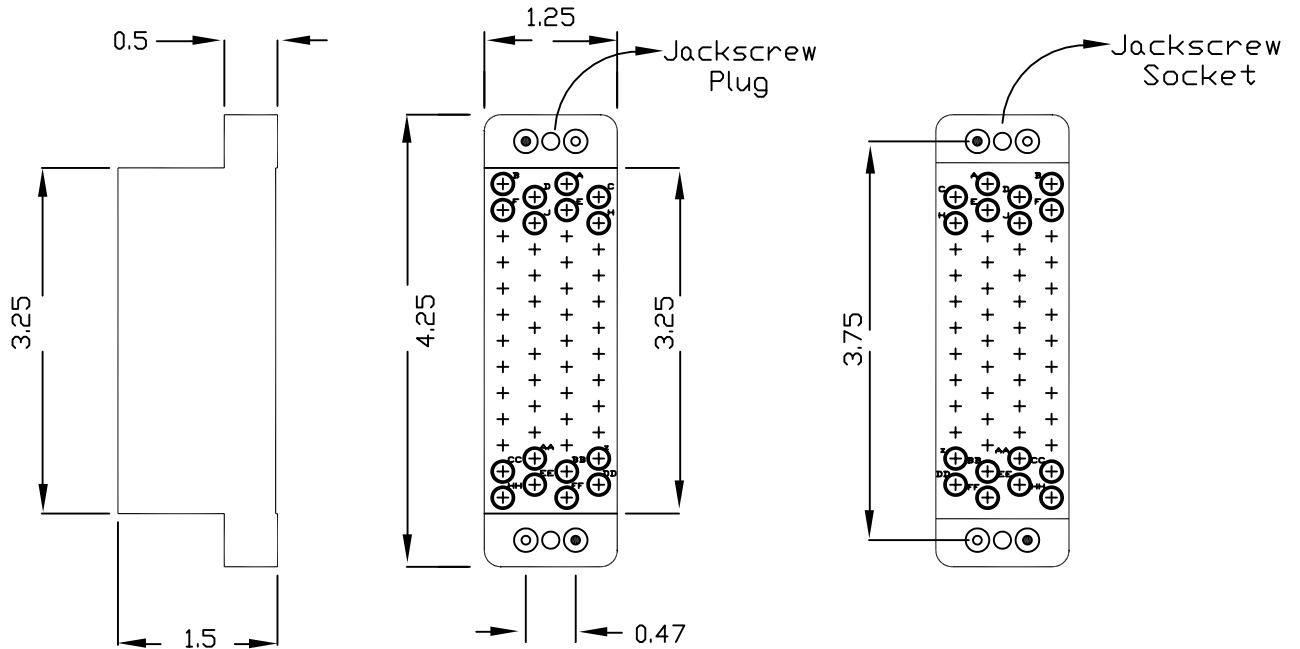
NOTES:

1. Cable length shall be 35.98in minimum. The cable shall be 2-pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.
2. All dimensions shown are in inches.

TITLE:		CONNECTOR DETAIL - M14
NO SCALE		A1-2
TEES 2009		



PLASTIC CIRCULAR PLUG AND SOCKET CONNECTOR

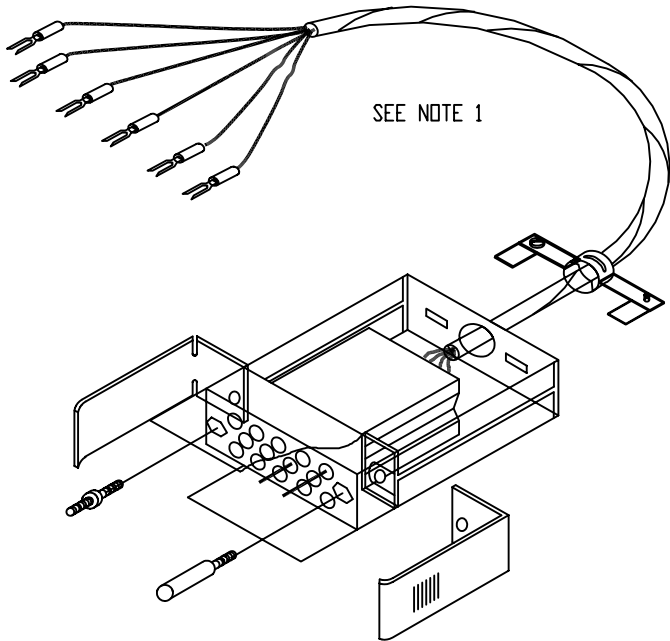


CONNECTOR PIN ARRANGEMENT

NOTES:

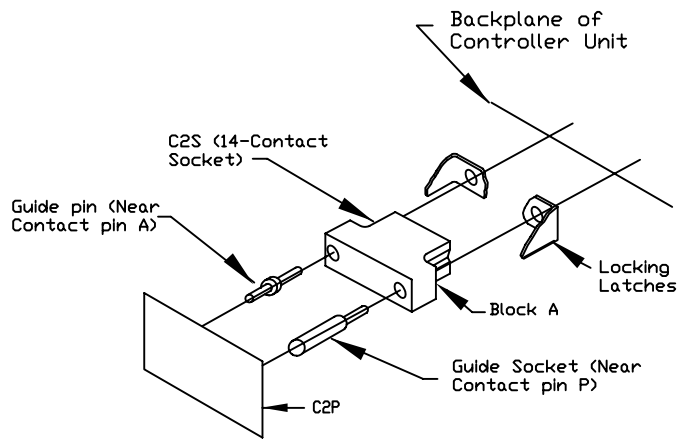
1. Guide Pins & Sockets, and Jackscrews are centered symmetrical to connector.
2. Key: - socket
- plug
3. All dimensions shown are in inches.

TITLE: CONNECTOR DETAIL M50 & CIRCULAR PLASTIC CONNECTOR	
NO SCALE	A1-3
TEES 2009	

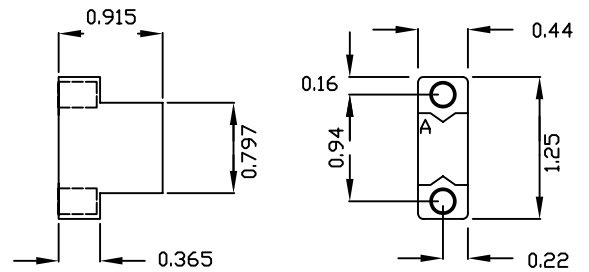


C2P MODEM INTERCONNECT HARNESS

C2P CONNECTOR ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
A	NA	J	RTS
B	NA	K	RXD
C	NA	L	TXD
D	NA	M	CTS
E	NA	N	GND
F	NA	P	NA
H	DCD	R	NA



CONNECTOR C2 DETAIL



CONNECTOR C2S

NOTES:

1. Cable length shall be 35.98in minimum. The cable shall be 2-pair #20 cable conductors, Belden 9402 or equal. The field end connections shall be #8 stud spring spade type.
2. All dimensions shall be inches.

TITLE:		SERIAL CONNECTOR DETAIL - M14S
NO SCALE		A1-4
TEES 2009		

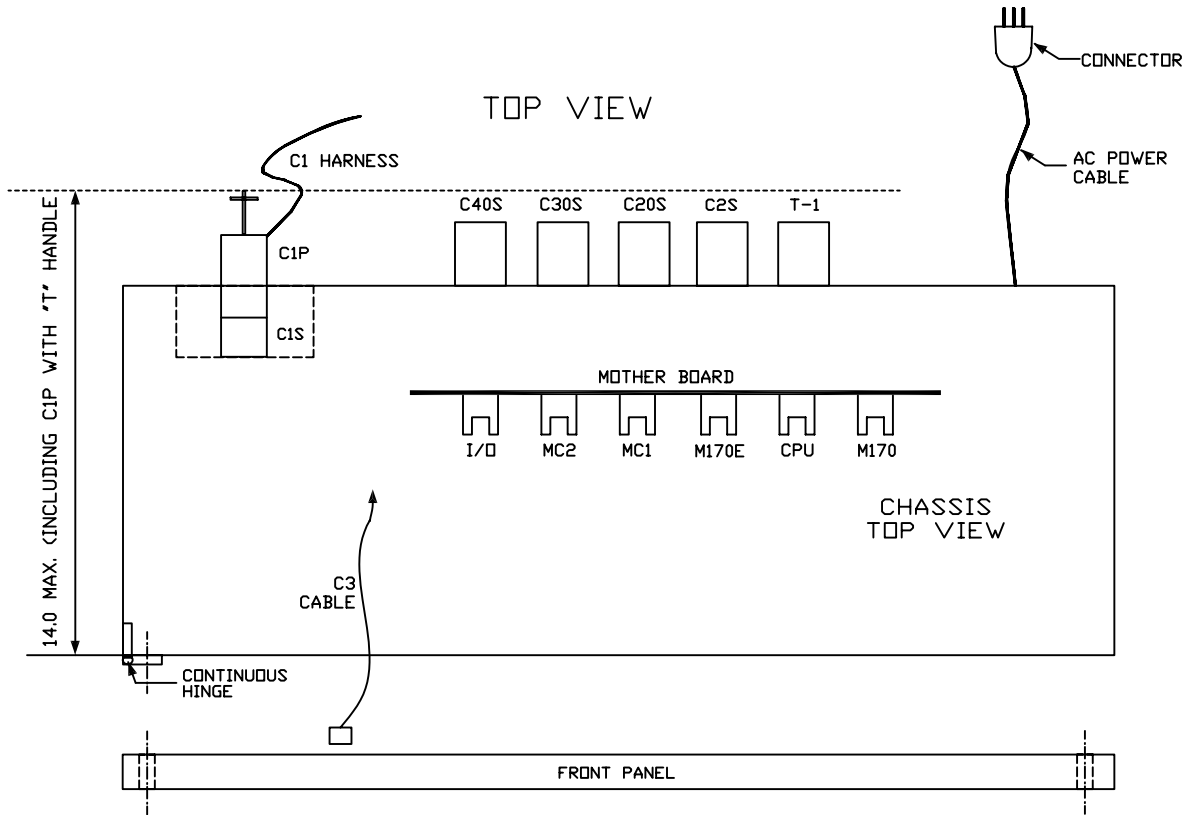
**APPENDIX A2
CHAPTER 2 DETAILS**

Model 170E Controller Unit Diagram	A2-1
Model 170E Controller Unit Block Diagrams	A2-2
Model 170E Input Port Address	A2-3
Model 170E Output Port Address	A2-4
Model 400, 400B and 400BE Modem	A2-5
Model 412C Program Module & Connectors M170 & M170E	A2-6
Model 400D Dial-Up and 400N Ethernet Module	A2-7
Model 400F Fiber Module	A2-8

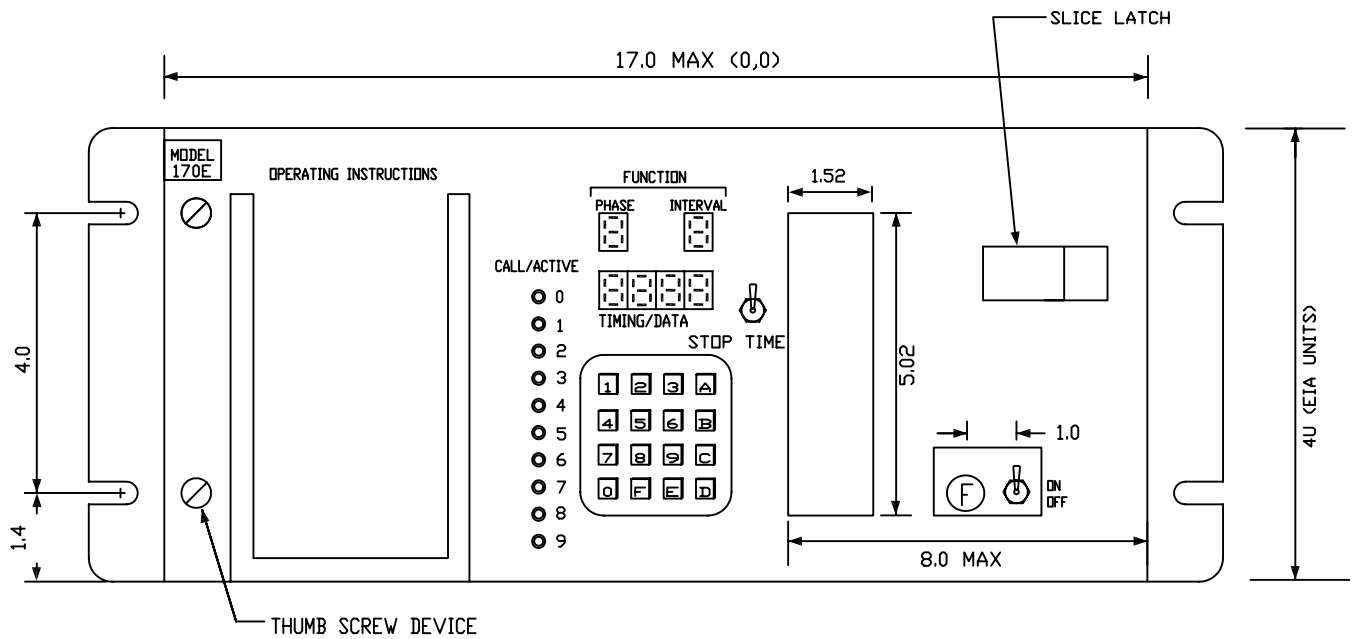
NOTES:

5. Program module' height and width dimensions are maximum.
6. C1 connector Pins 1, 14, 92 & 104 shall be connected to the controller unit DC logic ground.
7. All function under connector C2 & the terminal block T-1 are in reference to the MODEM
8. Detail Definitions:
 - BL** = BLANKING
 - CC** = CHARACTER CONTROL OR STROBE
 - CD** = CARRIER DETECT
 - CH** = CHARACTER
 - CTS** = CLEAR TO SEND
 - DP** = DECIMAL POINT
 - LS** = LEAST SIGNIFICANT
 - MS** = MOST SIGNIFICANT
 - NA** = PRESENTLY NOT ASSIGNED. CANNOT BE USED BY THE CONTRACTORS FOR OTHER PURPOSES.
 - NLS** = NEXT LEAST SIGNIFICANT
 - NMS** = NEST MOST SIGNIFICANT
 - P&I** = PHASE AND INTERVAL
 - RTS** = REQUEST TO SEND

MODEL 170E CONTROLLER UNIT DIAGRAM



FRONT VIEW



FRONT PANEL DISPLAY AND UNIT DETAIL

NOTE:

All dimensions shown are in inches.

TITLE: MODEL 170E CONTROLLER UNIT DIAGRAM

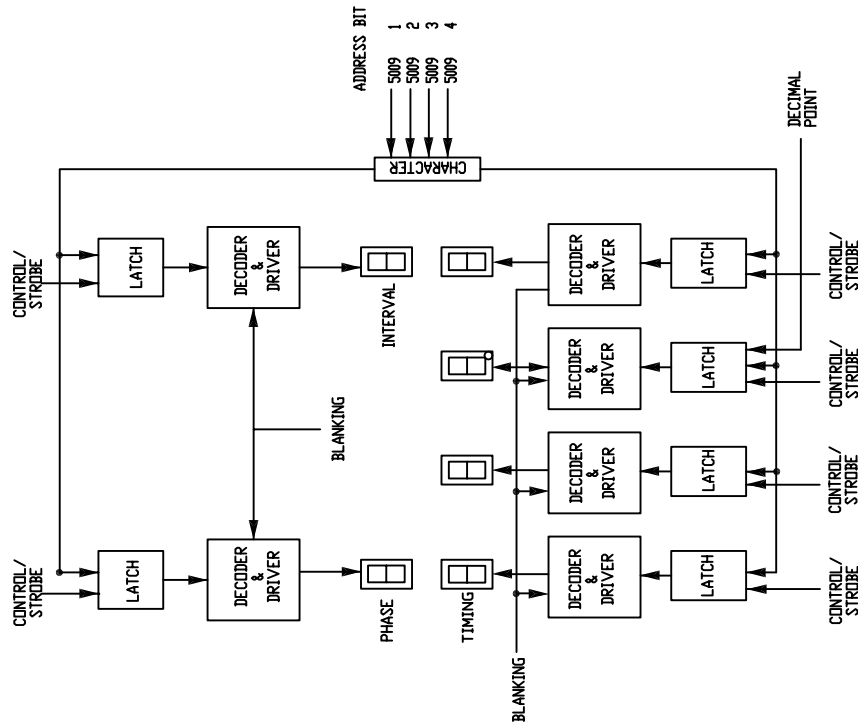
NO SCALE

TEES 2009

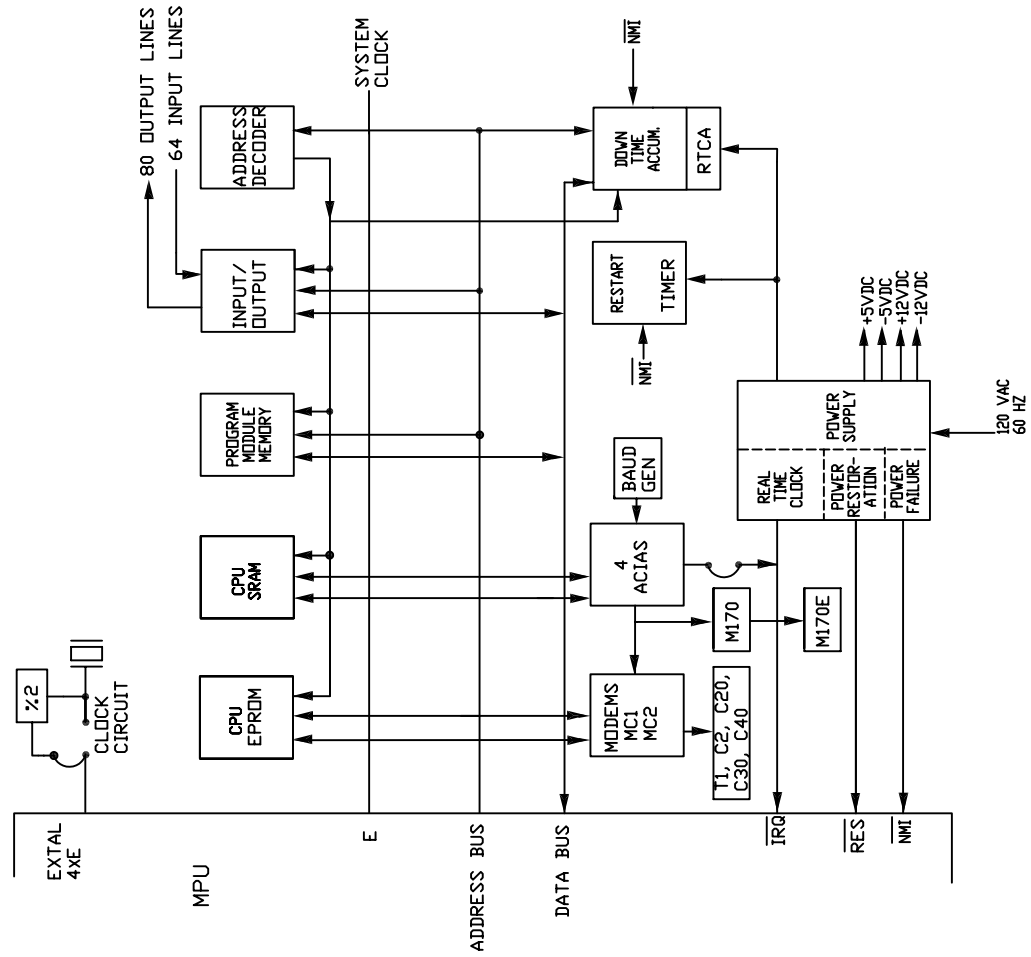
A2-1

MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS

FRONT PANEL DISPLAY BLOCK DIAGRAM



ORGANIZATION OF MODEL 170E CONTROLLER UNIT BLOCK DIAGRAM



TITLE: MODEL 170E CONTROLLER UNIT BLOCK DIAGRAMS	
NO SCALE	A2-2
TEES 2009	

INPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 AND C3

<u>INPUT PORT</u> <u>ADDRESS</u>	<u>BIT</u>	<u>CONNECTOR</u>		<u>INPUT PORT</u> <u>ADDRESS</u>	<u>BIT</u>	<u>CONNECTOR</u>	
		<u>C1</u>	<u>C3</u>			<u>C1</u>	<u>C3</u>
		<u>SOCKET</u> <u>CONTACTS</u>				<u>SOCKET</u> <u>CONTACTS</u>	
5001	1	39		5005	1	67	
5001	2	40		5005	2	68	
5001	3	41		5005	3	69	
5001	4	42		5005	4	70	
5001	5	43		5005	5	71	
5001	6	44		5005	6	72	
5001	7	45		5005	7	73	
5001	8	46		5005	8	74	
5002	1	47		5006	1	75	
5002	2	48		5006	2	76	
5002	3	49		5006	3	77	
5002	4	50		5006	4	78	
5002	5	51		5006	5	79	
5002	6	52		5006	6	80	
5002	7	53		5006	7	81	
5002	8	54		5006	8	82	
5003	1	55		5007	1		KEYBOARD CONTROL
5003	2	56		5007	2		KEYBOARD CH LS
5003	3	57		5007	3		KEYBOARD CH NLS
5003	4	58		5007	4		KEYBOARD CH NMS
5003	5	59		5007	5		KEYBOARD CH MS
5003	6	60		5007	6		STOP TIMING
5003	7	61		5007	7		NA
5003	8	62		5007	8		NA
5004	1	NA		5008	1		NA
5004	2	NA		5008	2		NA
5004	3	NA		5008	3		NA
5004	4	NA		5008	4		NA
5004	5	63		5008	5		NA
5004	6	64		5008	6		NA
5004	7	65		5008	7		NA
5004	8	66		5008	8		NA

CONNECTOR C2 SOCKET ASSIGNMENT (C20, C30 & C40)

<u>C2</u>		<u>C2</u>	
<u>SOCKET</u> <u>CONTACTS</u>	<u>FUNCTION</u>	<u>SOCKET</u> <u>CONTACTS</u>	<u>FUNCTION</u>
A	Audio IN	J	RTS
B	Audio IN	K	Data IN
C	Audio OUT	L	Data OUT
D	+5VDC	M	CTS
E	Audio OUT	N	DC GND
F	-5VDC	P	NA
H	CD	R	NA

TERMINAL BLOCK T-1 ASSIGNMENTS

- | | |
|-------------|--------------|
| 1. Audio IN | 6. CTS |
| 2. Audio IN | 7. Data Out |
| 3. CD | 8. Audio Out |
| 4. RTS | 9. Audio Out |
| 5. Data IN | 10. DC GND |

TITLE:

MODEL 170E INPUT ADDRESS

NO SCALE

TEES 2009

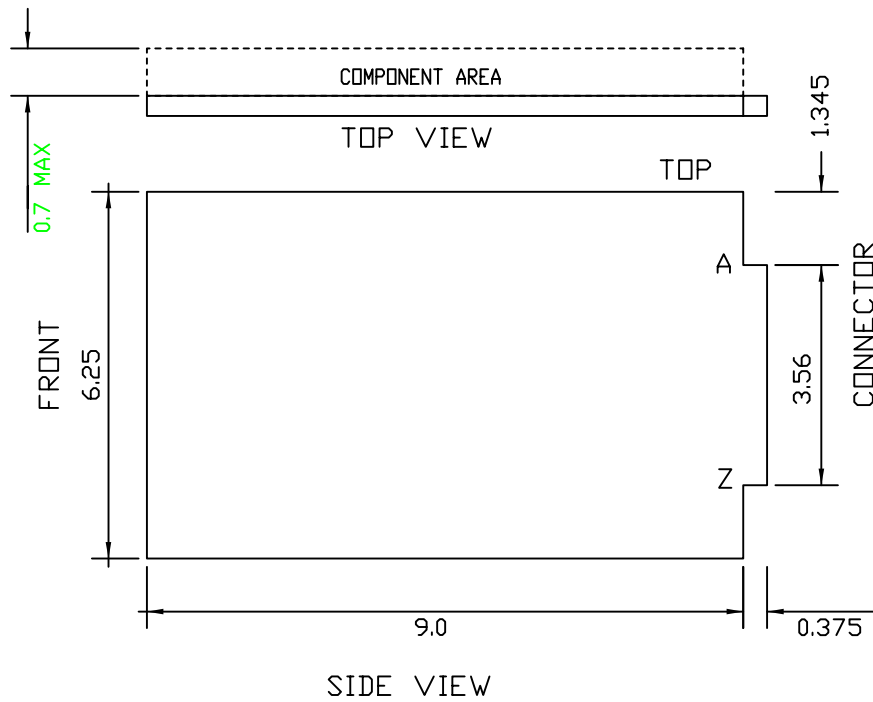
A2-3

OUTPUT PORT ADDRESS ASSIGNMENTS
FOR CONNECTORS C1 AND C3

<u>OUTPUT PORT ADDRESS</u>	<u>BIT</u>	<u>CONNECTOR C1 SOCKET CONTACTS</u>	<u>OUTPUT PORT ADDRESS</u>	<u>BIT</u>	<u>CONNECTOR C1 SOCKET CONTACTS</u>	<u>C3</u>
5001	1	2	5006	1	83	
5001	2	3	5006	2	84	
5001	3	4	5006	3	85	
5001	4	5	5006	4	86	
5001	5	6	5006	5	87	
5001	6	7	5006	6	88	
5001	7	8	5006	7	89	
5001	8	9	5006	8	90	
5002	1	10	5007	1	91	
5002	2	11	5007	2	93	
5002	3	12	5007	3	94	
5002	4	13	5007	4	95	
5002	5	15	5007	5	96	
5002	6	16	5007	6	97	
5002	7	17	5007	7	98	
5002	8	18	5007	8	99	
5003	1	19	5008	1		CC-PHASE
5003	2	20	5008	2		CC-INTERVAL
5003	3	21	5008	3		CC-TIMING LS
5003	4	22	5008	4		CC-TIMING NLS
5003	5	23	5008	5		CC-TIMING MLS
5003	6	24	5008	6		CC-TIMING MS
5003	7	25	5008	7		CALL LT 8
5003	8	26	5008	8		CALL LT 9
5004	1	27	5009	1		CH-LS
5004	2	28	5009	2		CH-NLS
5004	3	29	5009	3		CH-NMS
5004	4	30	5009	4		CH-MS
5004	5	31	5009	5		DP
5004	6	32	5009	6		BL-P&I
5004	7	33	5009	7		BL-TIMING
5004	8	34	5009	8		NA
5005	1	35	500A	1		CALL LT 0
5005	2	36	500A	2		CALL LT 1
5005	3	37	500A	3		CALL LT 2
5005	4	38	500A	4		CALL LT 3
5005	5	100	500A	5		CALL LT 4
5005	6	101	500A	6		CALL LT 5
5005	7	102	500A	7		CALL LT 6
5005	8	103	500A	8		CALL LT 7

TITLE: OUTPUT PORT ADDRESS ASSIGNMENTS FOR CONNECTORS C1 & C3	
NO SCALE	A2-4
TEES 2009	

MODEL 400, 400B & 400BE MODEM MODULE



MODEL 400, 400B & 400BE MODULE CONNECTOR ASSIGNMENT

COMPONENT SIDE	
CONTACT	MODEL 400 FUNCTION
1	NA
2	AUDIO INPUT
3	AUDIO INPUT
4	NA
5	NA
6	NA
7	NA
8	NA
9	NA
10	NA
11	NA
12	NA
13	NA
14	NA
15	NA
16	NA
17	NA
18	NA
19	NA
20	NA
21	NA
22	NA

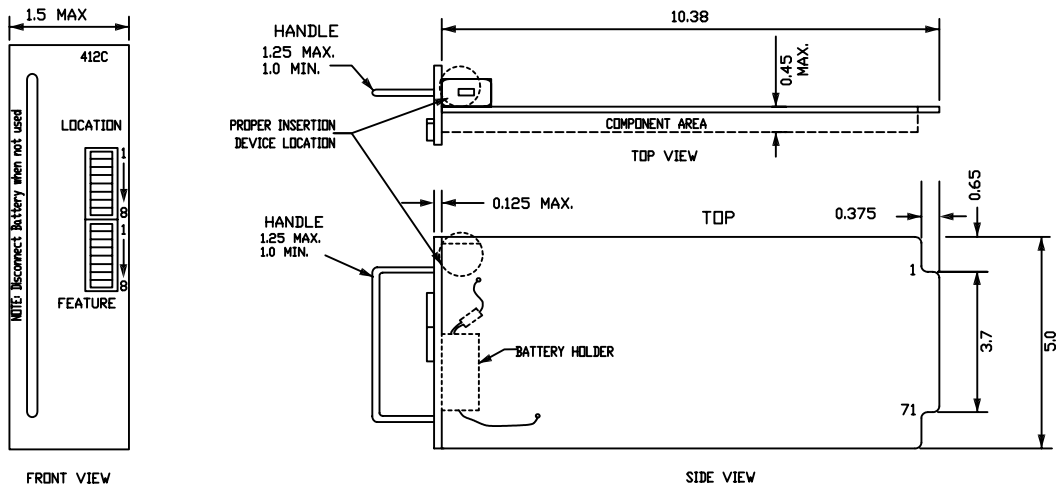
CIRCUIT SIDE	
CONTACT	MODEL 400 FUNCTION
A	DC GROUND
B	DC GROUND
C	12 VDC
D	12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	CARRIER DETECT
L	REQUEST TO SEND
M	DATA INPUT
N	CLEAR TO SEND
P	DATA OUTPUT
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	AUDIO OUTPUT
Y	AUDIO OUTPUT
Z	NA

NOTE:

All dimensions shown are in inches.

TITLE: MODEL 400, 400B & 400BE MODEM MODULE	
NO SCALE	A2-5
TEES 2009	

MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E



M170, M170E, AND 412C
PROGRAM MODULE CONNECTOR ASSIGNMENTS

CIRCUIT SIDE		COMPONENT SIDE		M170 ONLY NOT REQUIRED BY 412C
FUNCTION	PCB CONNECTOR	FUNCTION		
A0	1	2	A1	
A2	3	4	A3	
A4	5	6	A5	
A6	7	8	A7	
A8	9	10	A9	
A10	11	12	A11	
A12	13	14	A13	
A14	15	16	A15	
D0	17	18	D1	
D2	19	20	D3	
D4	21	22	D5	
D6	23	24	D7	
VMA / Q2(E)	25	26	NA	RES
READ/WRITE	27	28	NA	NMI
NA	29	30	NA	ROT
NA	31	32	NA	
NA	33	34	EQUIP. GND	
NA	35	36	NA	RTS ACIA 4
NA	37	38	NA	CTS ACIA 4
NA	39	40	NA	DCD ACIA 4
NA	41	42	NA	TXD ACIA 4** (SEE NOTE)
NA	43	44	NA	RXD ACIA 4** (SEE NOTE)
NA	45	46	NA	
NA	47	48	NA	
NA	49	50	NA	
NA	51	52	NA	
NA	53	54	NA	
NA	55	56	NA	
NA	57	58	NA	
12 VDC	59	60	12 VDC	
-12 VDC	61	62	-12 VDC	
KEY				
-5 VDC	63	64	-5 VDC	
5 VDC	65	66	5 VDC	
5 VDC	67	68	5 VDC	
GND	69	70	GND	
GND	*71	*72	GND	

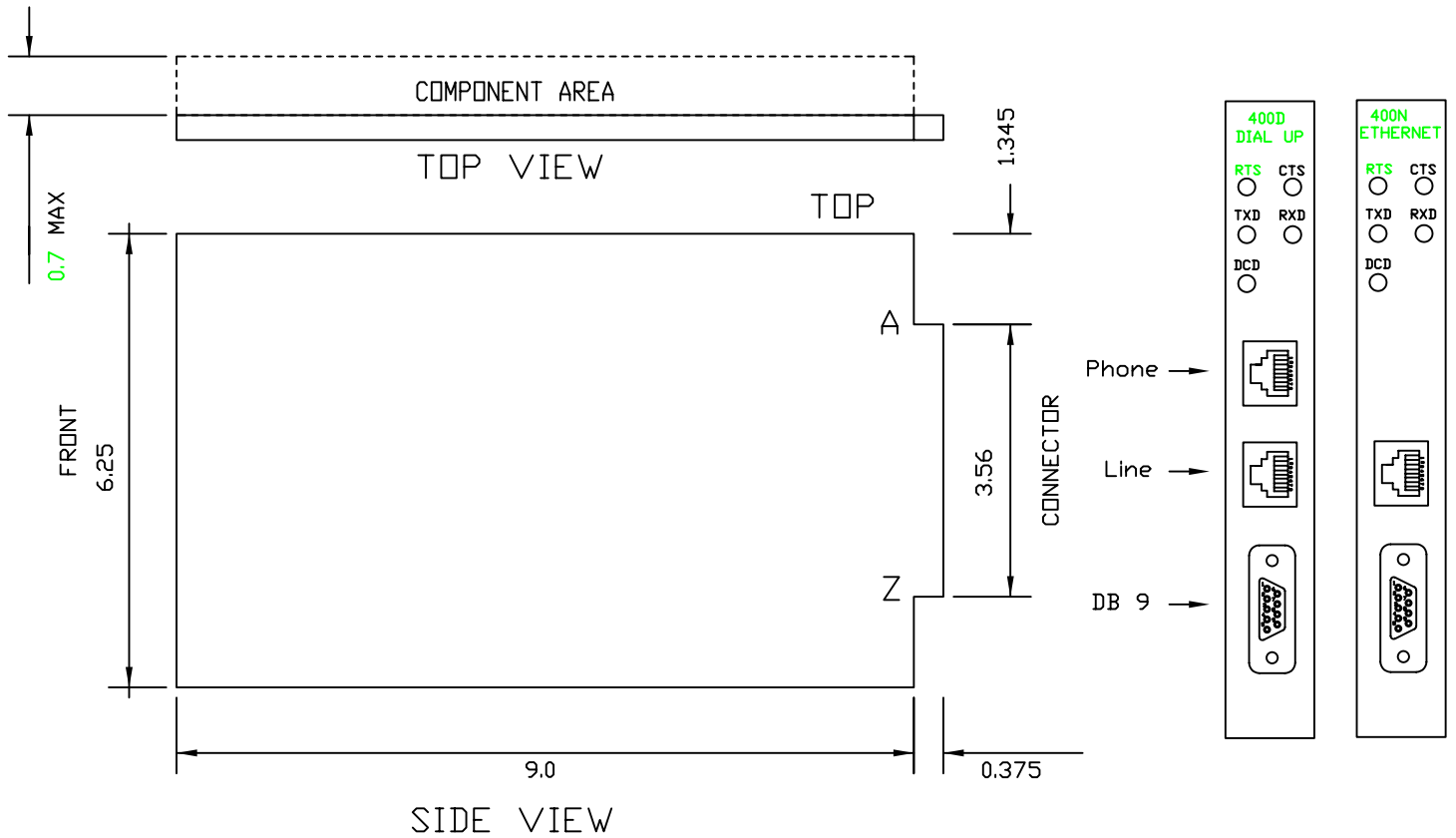
NOTES:

* Pins 71 & 72 on M170 & 170E connectors shall be commoned. Pins 71 & 72 on the Model 412C shall be tied to pins 69 & 70.

** Relative to the ACIA.

All dimensions shown are in inches.

TITLE: MODEL 412C PROGRAM MODULE AND CONNECTORS M170 & M170E	
NO SCALE	A2-6
TEES 2009	



CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA

DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

RJ45 ETHERNET PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	NA
3	RX +	7	NA
4	RX-	8	NA

NOTE:

All dimensions shown are in inches.

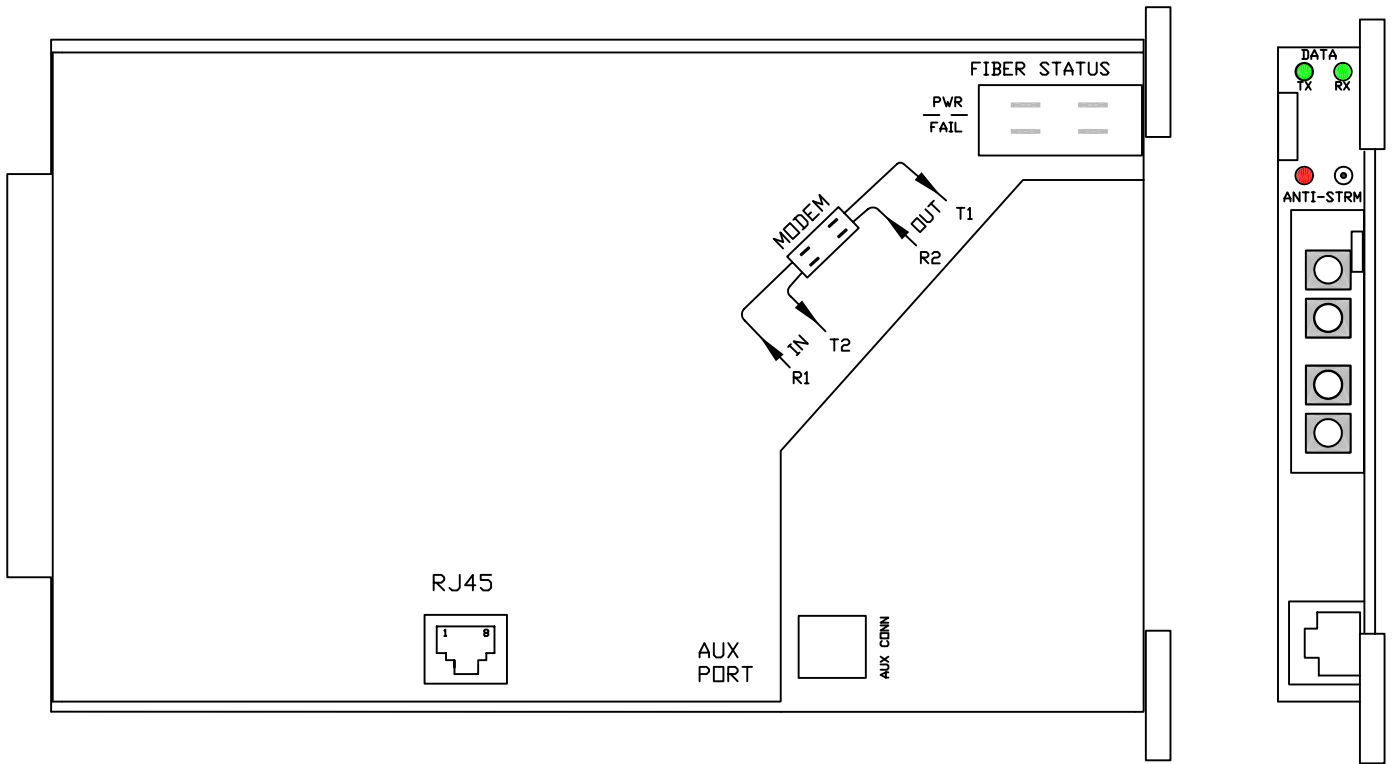
TITLE:

MODEL 400D & 400N

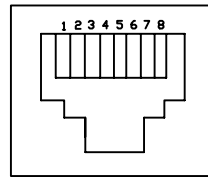
NO SCALE

TEES 2009

A2-7



CARD EDGE	
PIN	FUNCTION
A	DC GROUND
B	DC GROUND
C	+12 VDC
D	+12 VDC
E	-12 VDC
F	-12 VDC
H	NA
J	NA
K	DCD
L	RTS
M	TXD
N	CTS
P	RXD
R	NA
S	NA
T	NA
U	NA
V	NA
W	NA
X	NA
Y	NA
Z	NA



RJ45 (detail)

RJ45 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	NA	5	RXD
2	CD	6	TXD
3	NA	7	CTS
4	GND	8	RTS

TITLE:

MODEL 400F FIBER MODULE

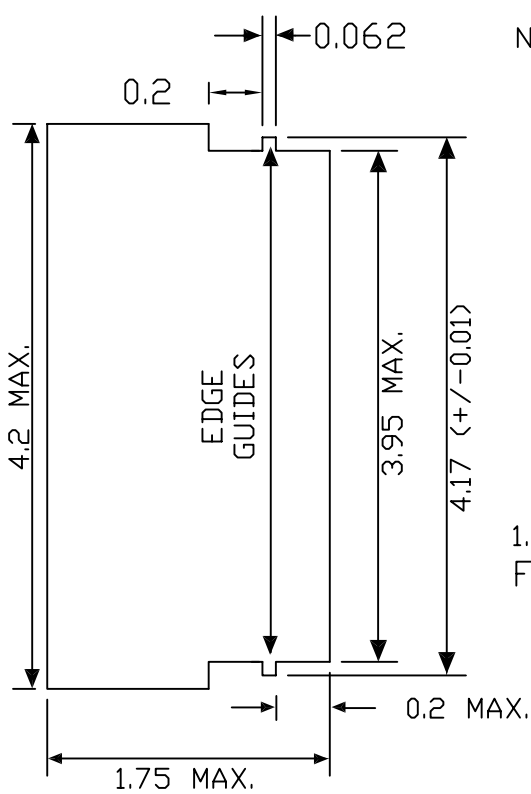
NO SCALE

TEES 2009

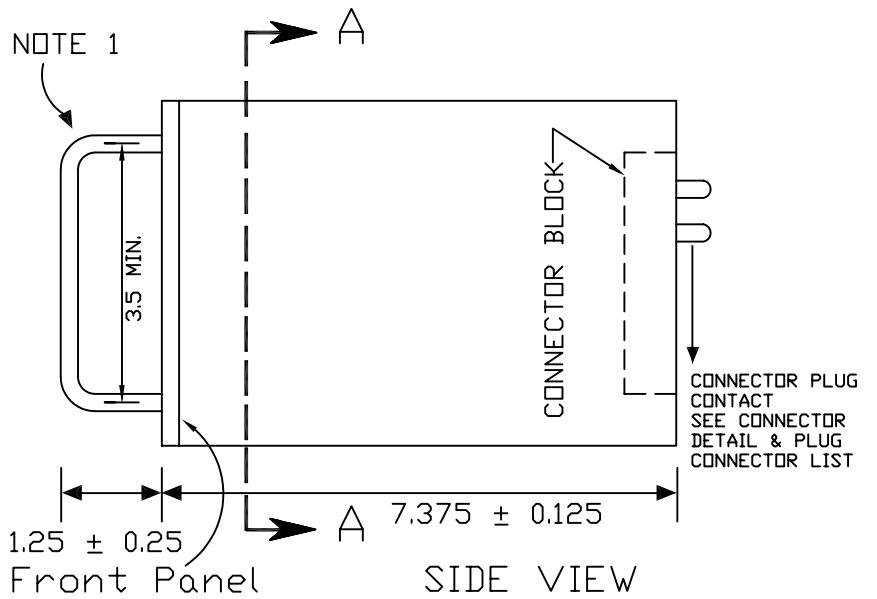
A2-8

**APPENDIX A3
CHAPTER 3 DETAILS**

Model 200 Switch Pack, 204 & 205 CONNECTOR DETAILS	A3-1
Model 208 T170 Monitor Units	A3-2
Model 210 T170 Monitor Unit	A3-3
Model 210 T170 Monitor Unit	A3-4
Programming Card Connector & Wiring Assignments	
Models 222, 224, 232, 242 and 252	A3-5
Model 206L Power Supply	A3-6



CROSS SECTION A-A



MODEL PLUG CONNECTORS LIST
(OR EQUAL)

- MODEL 200 - BEAU P-5412-LAB
- MODEL 204 - BEAU P-5406-LAB
- MODEL 205 - BEAU P-5408-LAB

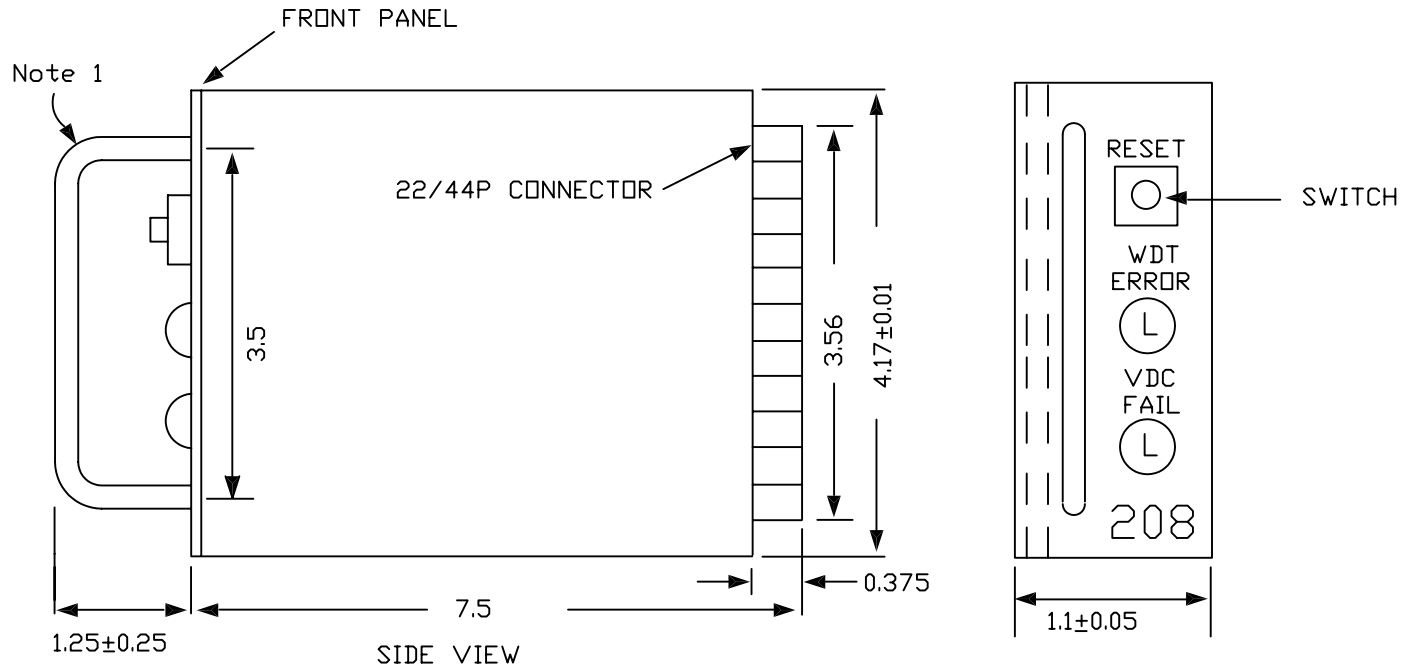
MODEL 200, 204 & 205 CONNECTOR DETAIL

PIN	FUNCTION	PIN	FUNCTION	PIN	Function
1	AC+	7	Load Circuit #1	1	Coil
2	Equip. Ground	8	Load Circuit #2	2	Coil
3	Red Output	9	Equip. Ground	3	NC CKT1
4	Not Assigned	10	AC-	4	NC CKT2
5	Yellow Output	11	AC+	5	Common CKT1
6	Red Input	12	Not Assigned	6	Common CKT2
7	Green Output			7	NO CKT1
8	Yellow Input			8	NO CKT2
9	+24 VDC				
10	Green Input				
11	AC-				
12	Not Assigned				

NOTES:

1. "U" shape rod handle shall be fabricated of 0.18in to 0.26in diameter stock to form a handle.
2. All dimensions shown are in inches.

TITLE:	
MODEL 200 SWITCH PACK, 204 & 205 CONNECTOR DETAILS	
NO SCALE	A3-1
TEES 2009	



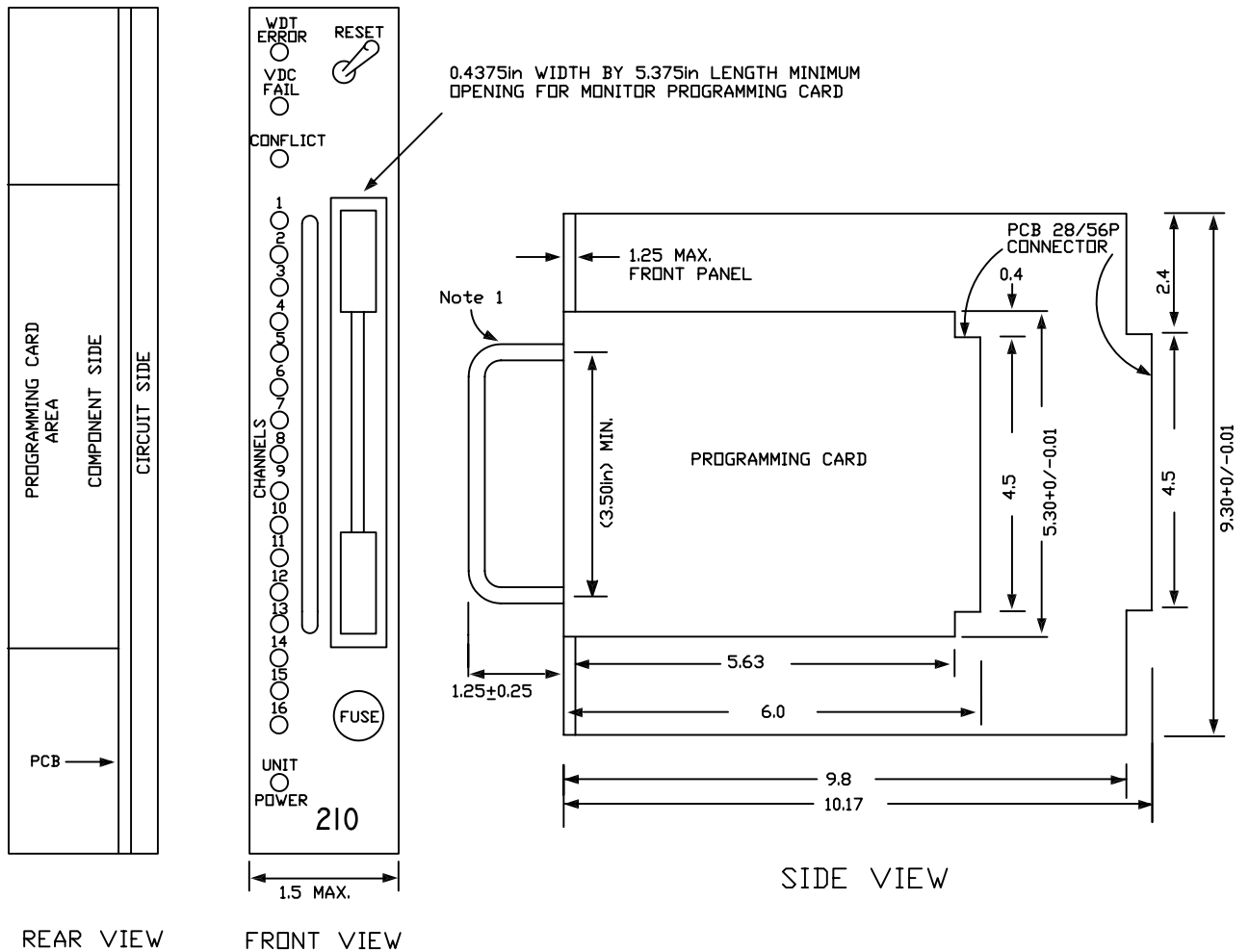
MODEL 208 MONITOR UNIT PIN ASSIGNMENT

<u>PIN</u>	<u>FUNCTION</u>
1/A	DC Ground
2/B	WDT Ext. Reset
5/E	WDT IN
10/L	+24 VDC
15/S	AC-
17/U	Normally Open, Circ. #2
19/W	AC+
20/X	WDT Lamp (External)
21/Y	Circ. Common #1 & #2
22/Z	Normally Closed, Circ. #1

NOTE:

- "U" shape rod handle shall be fabricated of 0.18in to 0.26in diameter stock to form a handle.
- All dimensions shown are in inches.

TITLE:		MODEL 208 T170 MONITOR UNITS
NO SCALE	A3-2	
TEES 2009		



NOTES: (FOR DETAILS A3-3 & A3-4):

- "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter stock to form a handle.
- Model 210 tolerance dimensions are +/- 0.02 in except as noted.
- Sheet definitions:
 - = Slotted for keying.
 - (C) = Collector
 - (E) = Emitter
 - * = NA for these connections on models 232 & 242.
- All dimensions shown are in inches.

TITLE:	
MODEL 210 T170 MONITOR UNIT	
NO SCALE	A3-3
TEES 2009	

MODEL 210 MONITOR UNIT
CONNECTOR WIRING ASSIGNMENTS

MODEL 210
PROGRAMMING CARD
CONNECTOR WIRING ASSIGNMENTS

Pin	FUNCTION	Pin	FUNCTION
1	Channel #2 Green	A	Channel #2 Yellow
2	Channel #13 Green	B	Channel #6 Green
3	Channel #6 Yellow	C	Channel #15 Green
4	Channel #4 Green	D	Channel #4 Yellow
5	Channel #14 Green	E	Channel #8 Green
6	Channel #8 Yellow	F	Channel #16 Green
7	Channel #5 Green	H	Channel #5 Green
8	Channel #13 Yellow	J	Channel #1 Green
9	Channel #1 Yellow	K	Channel #15 Yellow
10	Channel #7 Green	L	Channel #7 Yellow
11	Channel #14 Yellow	M	Channel #3 Green
12	Channel #3 Yellow	N	Channel #16 Yellow
13	Channel #9 Green	P	NA
14	NA	R	Channel #10 Green
15	Channel #11 Yellow	S	Channel #11 Green
16	Channel #9 Yellow	T	NA
17	NA	U	Channel #10 Yellow
18	Channel #12 Yellow	V	Channel #12 Green
19	NA	W	NA
20	Equipment Ground	X	NA
21	AC- *	Y	DC Ground
22	Watchdog Timer	Z	External Reset
23	+24 VDC	AA	+24 VDC
24	(Pins 24 & 25 Tied Together)	BB	Stop Time
25		CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

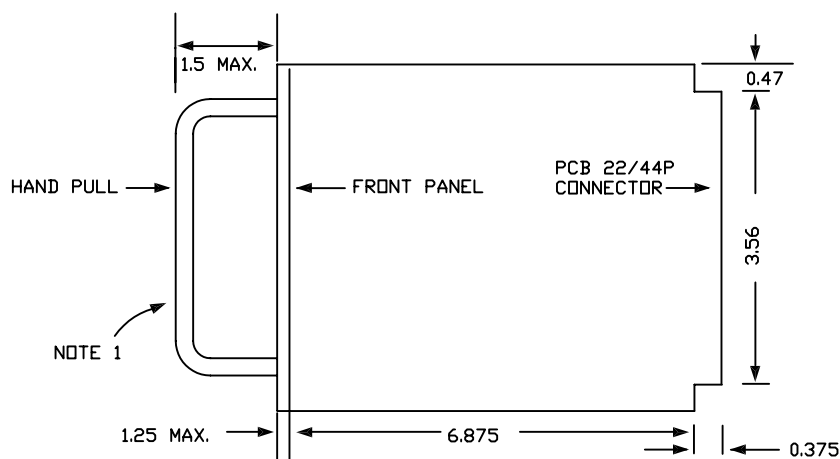
Pin	FUNCTION (Circuit Side)	Pin	FUNCTION (Component Side)
1	Channel #2 Green	A	Channel #1 Green
2	Channel #3 Green	B	Channel #2 Green
3	Channel #4 Green	C	Channel #3 Green
4	Channel #5 Green	D	Channel #4 Green
5	Channel #6 Green	E	Channel #5 Green
6	Channel #7 Green	F	Channel #6 Green
7	Channel #8 Green	H	Channel #7 Green
8	Channel #9 Green	J	Channel #8 Green
9	Channel #10 Green	K	Channel #9 Green
10	Channel #11 Green	L	Channel #10 Green
11	Channel #12 Green	M	Channel #11 Green
12	Channel #13 Green	N	Channel #12 Green
13	Channel #14 Green	P	Channel #13 Green
14	Channel #15 Green	R	Channel #14 Green
15	Channel #15 Green	S	Channel #15 Green
16	DC Ground	T	CONFLICT
17	Channel #1 Yellow	U	Channel #9 Yellow
18	Channel #2 Yellow	V	Channel #10 Yellow
19	Channel #3 Yellow	W	Channel #11 Yellow
20	Channel #4 Yellow	X	Channel #12 Yellow
21	Channel #5 Yellow	Y	Channel #13 Yellow
22	Channel #6 Yellow	Z	Channel #14 Yellow
23	Channel #7 Yellow	AA	Channel #15 Yellow
24	Channel #8 Yellow	BB	Channel #16 Yellow
25	NA	CC	NA
26	NA	DD	NA
27	NA	EE	Output SW, Side #2
28	Output SW, Side #1	FF	AC+

TITLE: MODEL 210 T170 MONITOR UNIT
PROGRAMMING CARD CONNECTOR
& WIRING ASSIGNMENTS

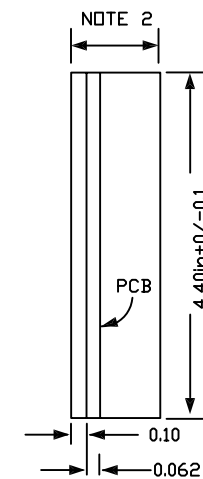
NO SCALE

TEES 2009

A3-4



SIDE VIEW



END VIEW

MODEL 222, 224, & 232
CONNECTOR ASSIGNMENTS

PIN	FUNCTION
A	DC Ground
B	+24 VDC
---	---
*C	Detector Reset
D	# 1 Input
E	# 1 Input
F	# 1 Output (C)
H	# 1 Output (E)
J	# 2 Input
K	# 2 Input
L	Equipment Ground
M	AC-
---	---
N	AC+
P	# 3 Input
R	# 3 Input
S	# 3 Output (C)
T	# 3 Output (E)
U	# 4 Input
V	# 4 Input
W	# 2 Output (C)
X	# 2 Output (E)
Y	# 4 Output (C)
Z	# 4 Output (E)

MODEL 242 & 252
CONNECTOR ASSIGNMENTS

PIN	FUNCTION
*A	DC Ground
*B	+24 VDC
---	---
C	NA
D	# 1 Input
E	# 1 Input Common
F	# 1 Output (C)
H	# 1 Output (E)
J	# 2 Input
K	# 2 Input Common
L	Equipment Ground
M	AC-
---	---
N	AC+
P	NA
R	NA
S	NA
T	NA
U	NA
V	NA
W	# 2 Output (C)
X	# 2 Output (E)
Y	NA
Z	NA

NOTES:

- "U" shape rod handle shall be fabricated of 0.18in to 0.26 diameter stock to form a handle.
- Models 222, 232, 242 and 252 shall have a width of 1.12in. Model 224 shall have a width of 2.0+/-0.25.
- Sheet definitions:
 ---- = Slotted for keying.
 (C) = Collector
 (E) = Emitter
 * = NA for these connections on models 232 & 242.
- All dimensions shown are in inches.

TITLE:

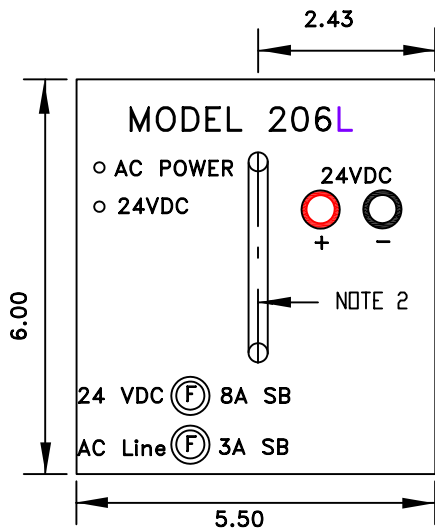
MODELS 222, 224, 232,
242 AND 252

NO SCALE

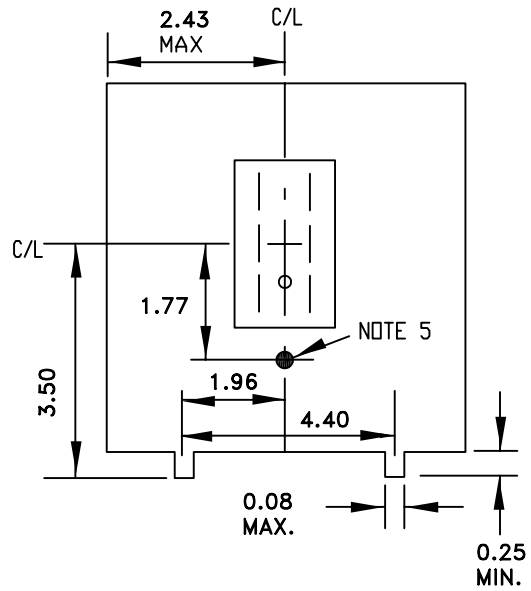
TEES 2009

A3-5

MODEL 206L POWER SUPPLY MODULE

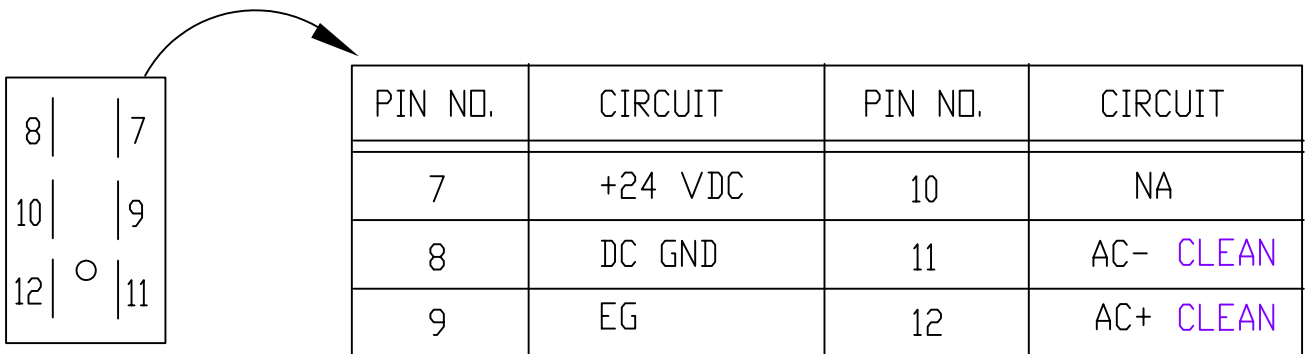


FRONT VIEW



REAR VIEW

POWER SUPPLY MODULE WIRING DETAIL

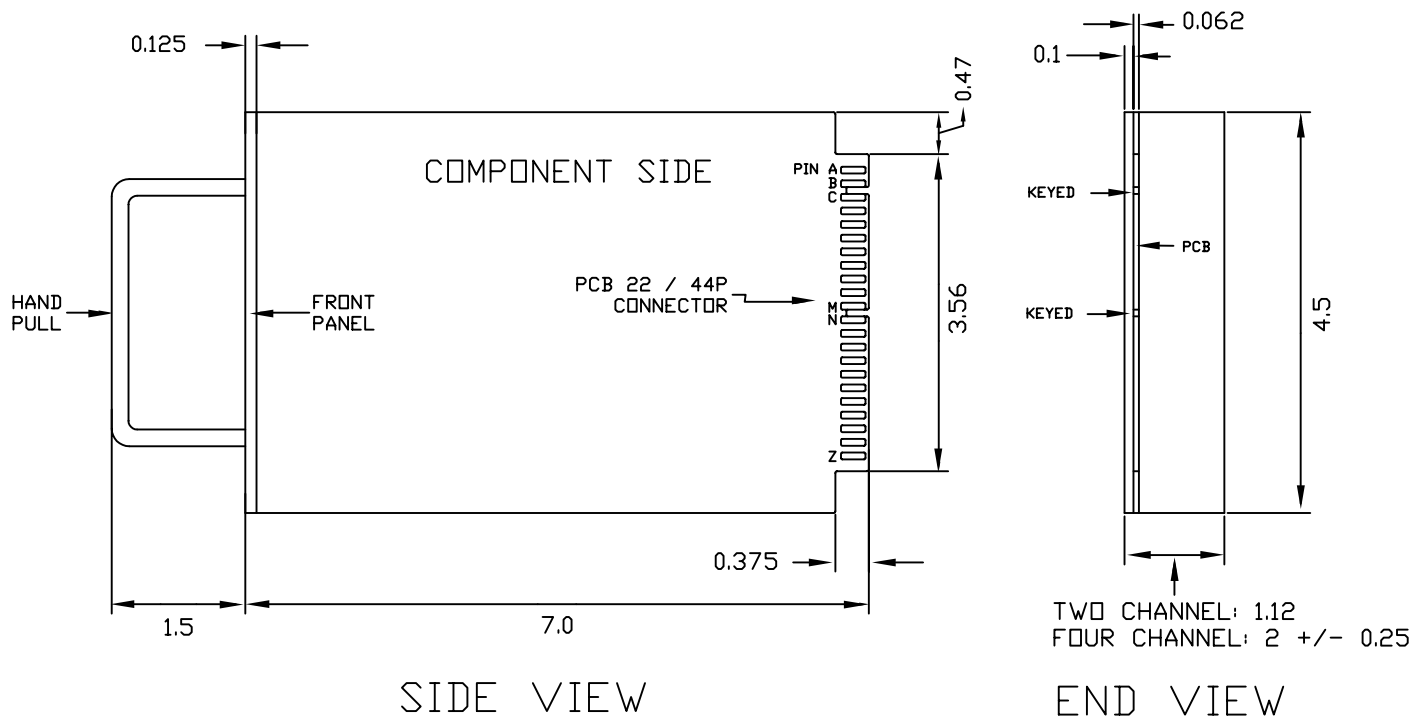


REAR VIEW

NOTE:
All dimensions shown are in inches.

TITLE:		MODEL 206L POWER SUPPLY
NO SCALE	A3-6	
TEES 2009		

**APPENDIX A5
CHAPTER 5 DETAILS**



CONNECTOR ASSIGNMENTS

PIN	ISOLATORS	SENSORS
A	DC GROUND	
B	+24 VDC	
C	N/A	EXT RESET
D	INPUT #1	
E	INPUT #1	
F	OUTPUT #1 (C)	
H	OUTPUT #1 (E)	
J	INPUT #2	
K	INPUT #2	
L	EQUIPMENT GROUND	
M	AC-	
N	AC+	
P	N/A	INPUT #3
R	N/A	INPUT #3
S	N/A	OUTPUT #3 (C)
T	N/A	OUTPUT #3 (E)
U	N/A	INPUT #4
V	N/A	INPUT #4
W	OUTPUT #2 (C)	
X	OUTPUT #2 (E)	
Y	N/A	OUTPUT #4 (C)
Z	N/A	OUTPUT #4 (E)

NOTES:

1. Tolerance dimensions are +/-0.02 in except as noted.
2. "U" shape rod handle shall be fabricate of 0.18 in to 0.26 in diameter stock.
3. All dimensions shall be in inches.

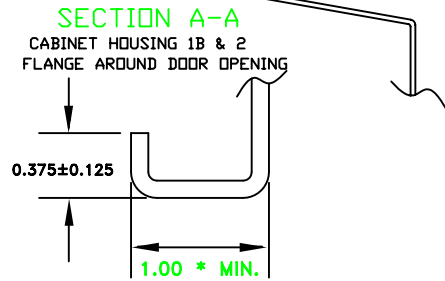
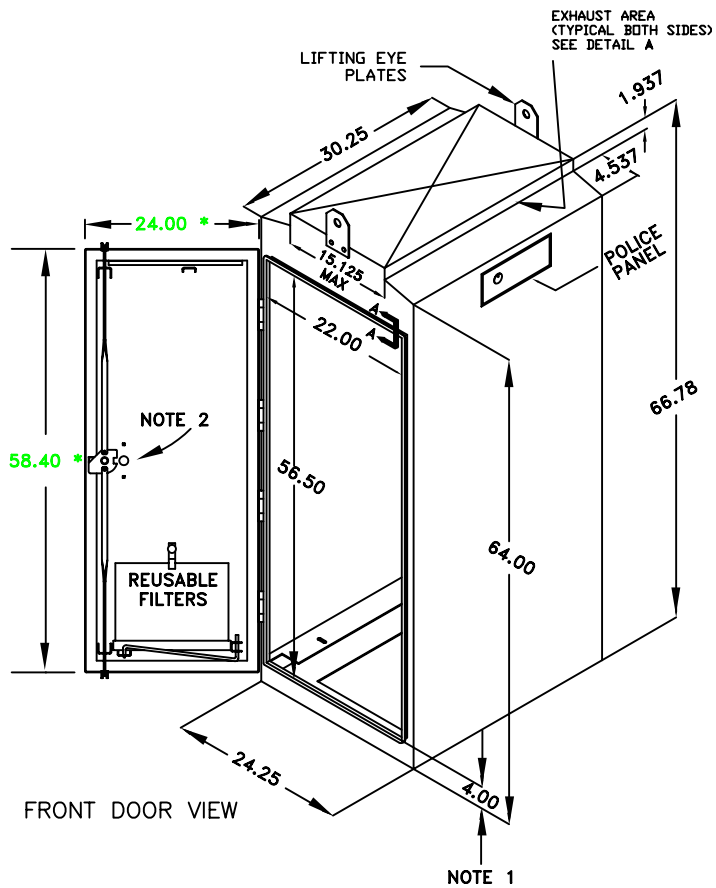
TITLE: SENSOR UNIT AND ISOLATOR DETAILS	
NO SCALE	A5-1
TEES 2009	

**APPENDIX A6
CHAPTER 6 DETAILS**

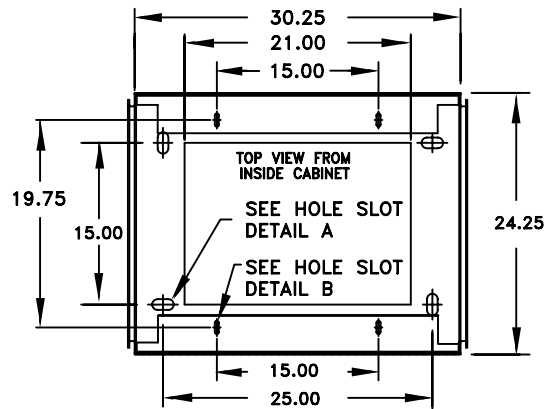
Cabinet Housing Details - sheet 1 of 4	A6-1
Cabinet Housing Details - sheet 2 of 4	A6-2
Cabinet Housing Details - sheet 3 of 4	A6-3
Cabinet Housing Details - sheet 4 of 4	A6-4
Cabinet Equipment Mounting Details	A6-5
Drawer Shelf Details	A6-6
Model 332L and 336L One Line Diagram	A6-7
SSR Installation Details	A6-8
Model 334L One Line Diagram	A6-9
Service Panel Assembly Details – sheet 1 of 3	A6-10
Service Panel Assembly Details – sheet 2 of 3	A6-11
Service Panel Assembly Details - sheet 3 of 3	A6-12
PDA #2L & #3L Details – sheet 1 of 3	A6-13
PDA #2L & #3L Details – sheet 2 of 3	A6-14
PDA #2L & #3L Details – sheet 3 of 3	A6-15
Input/Output Files Details - sheet 1 of 5	A6-16
Input/Output Files Details - sheet 2 of 5	A6-17
Input/Output Files Details - sheet 3 of 5	A6-18
Input/Output Files Details - sheet 4 of 5	A6-19
Input/Output Files Details - sheet 5 of 5	A6-20
Side Panel Details - sheet 1 of 4	A6-21
Side Panel Details - sheet 2 of 4	A6-22
Side Panel Details - sheet 3 of 4	A6-23
Side Panel Details - sheet 4 of 4	A6-24
Hardness Wiring Details - sheet 1 of 5	A6-25
Hardness Wiring Details - sheet 2 of 5	A6-26
Hardness Wiring Details - sheet 3 of 5	A6-27
Hardness Wiring Details - sheet 4 of 5	A6-28
Hardness Wiring Details - sheet 5 of 5	A6-29
Fan and Thermostat Details	A6-30

CABINET HOUSING 1B

DETAIL A CABINET HOUSING 1B & 2 VENTILATION EXHAUST DETAIL

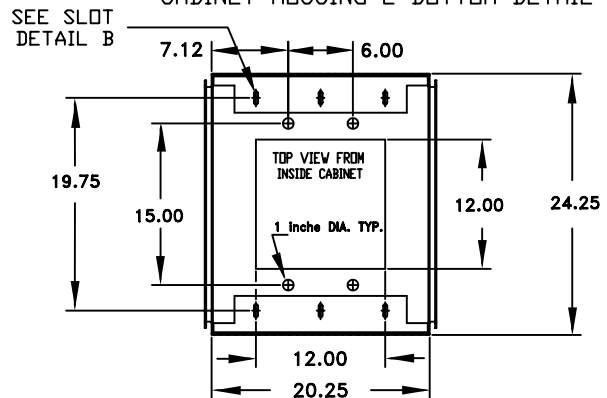
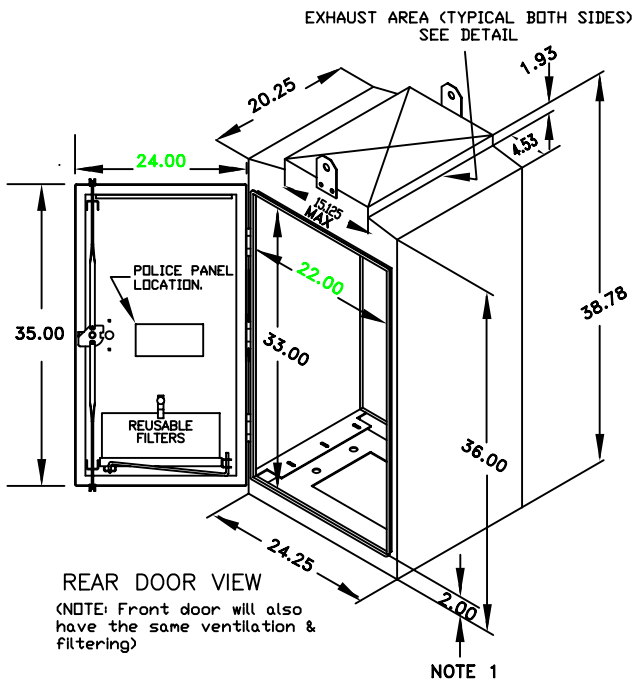


* TOLERANCE +0.0625, -0
CABINET HOUSING 1B BOTTOM DETAIL

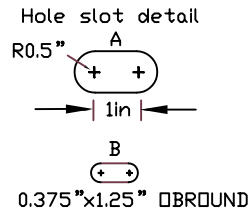


CABINET HOUSING 2

CABINET HOUSING 2 BOTTOM DETAIL



NOTE: ALL HOLE PATTERNS CENTERED ON CABINET BOTTOMS.

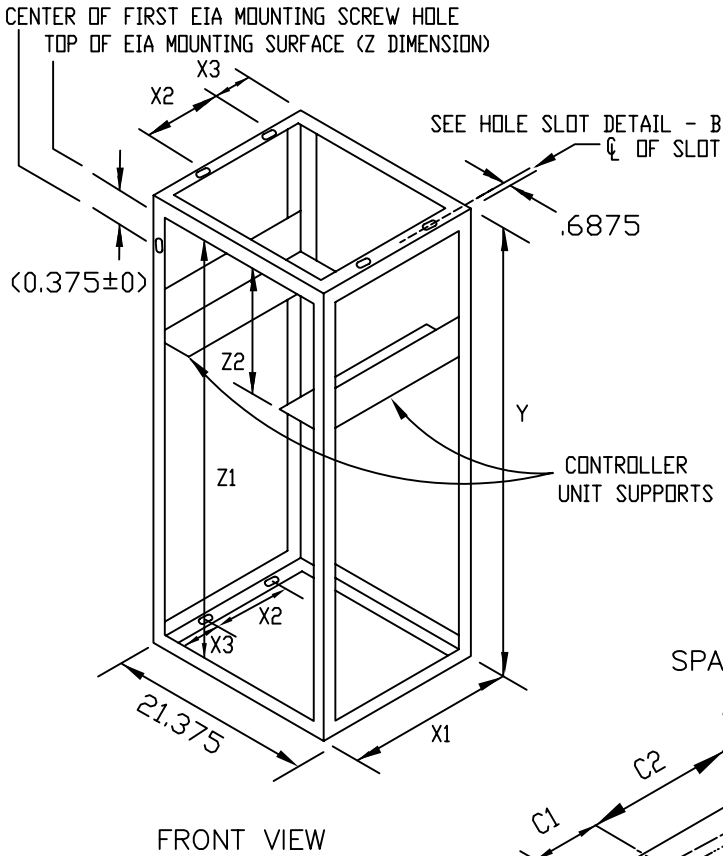


NOTE:

1. Cabinet base to door opening.
2. The locks & handles shall be on right side of the front door & the left side of the rear door (viewed externally)
3. All dimensions shown are in inches.

TITLE:	
CABINET HOUSING DETAILS SHEET 1 OF 4	
NO SCALE	A6-1
TEES 2009	

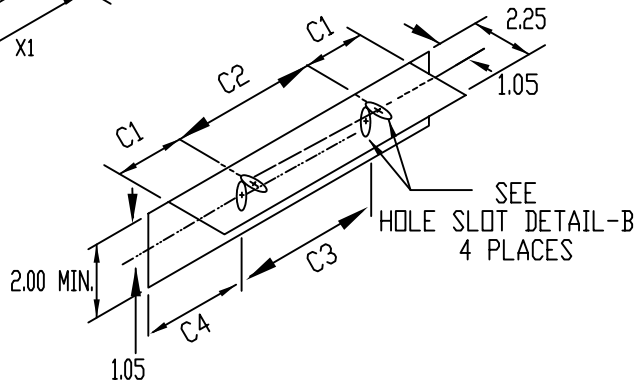
CAGE SUPPORT DETAIL



CABINET CAGE DIMENSIONS

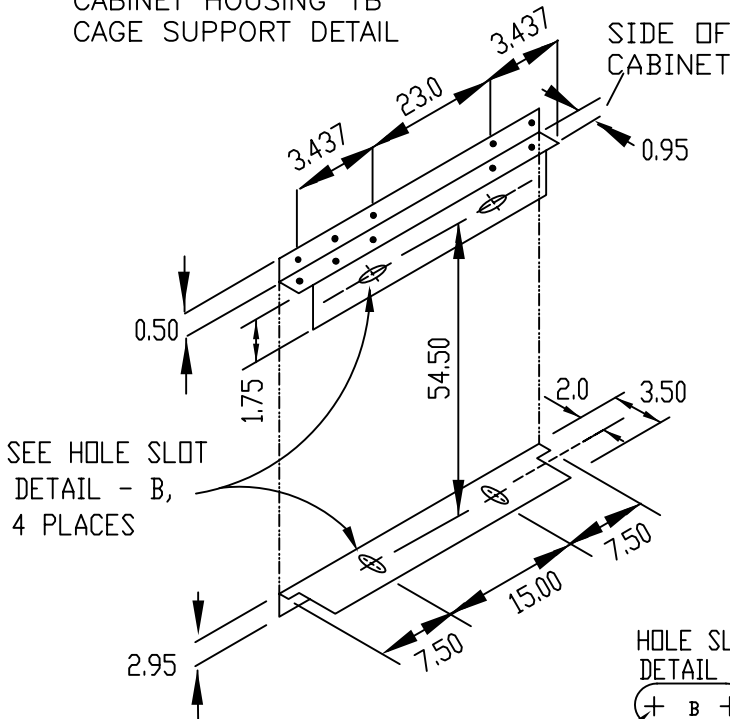
	CAGE #1	CAGE #2
X1	21.375	16.00
X2	15.00	12.00
X3	3.188	2.00
Y	55.50	32.50
Z1	53.00 MIN.	31.00 MIN.
Z2	15.75	7.25

SPACER BRACKET DETAIL

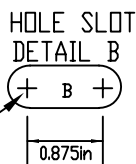
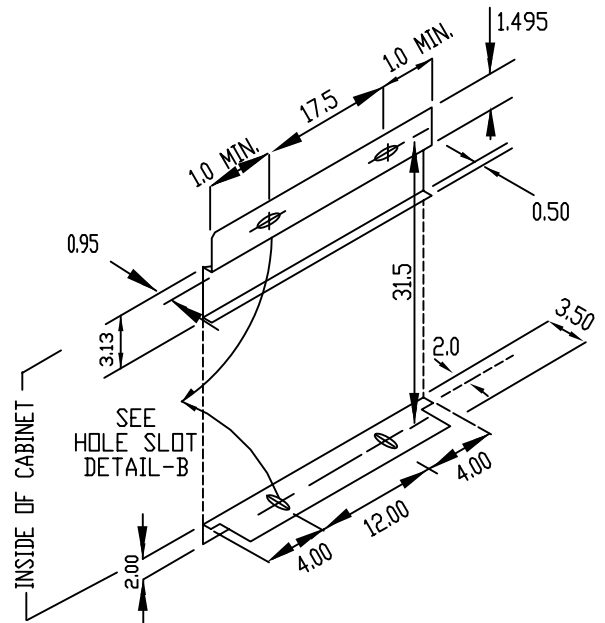


	CAGE #1	CAGE #2
C1	3.0 MIN.	3.0 MIN.
C2	15.0	12.0
C3	23.0	17.5
C4	1.0 MIN.	1.0 MIN.

CABINET HOUSING 1B CAGE SUPPORT DETAIL



CABINET HOUSING 2 CAGE SUPPORT DETAIL

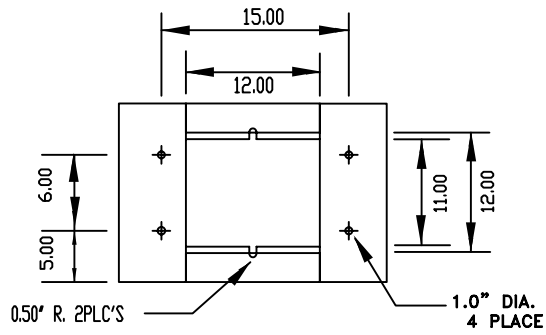


NOTE:
All dimensions shown are in inches

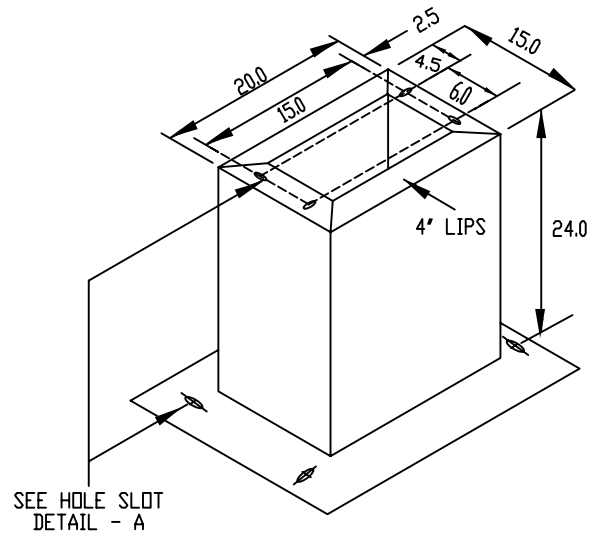
TITLE: CABINET HOUSING DETAILS SHEET 2 OF 4	
NO SCALE	A6-2
TEES 2009	

TYPE 332/336 ADAPTOR

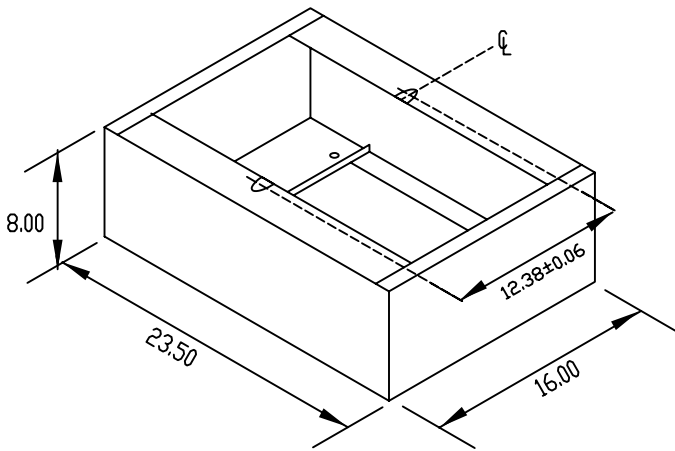
CABINET HOUSING 2
"M" BASE ADAPTOR DETAIL



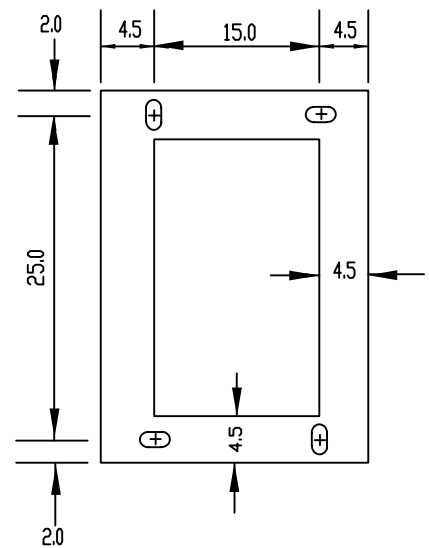
TOP VIEW



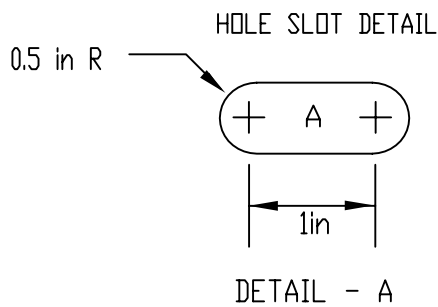
SEE HOLE SLOT
DETAIL - A



BOTTOM VIEW



332 BASE VIEW

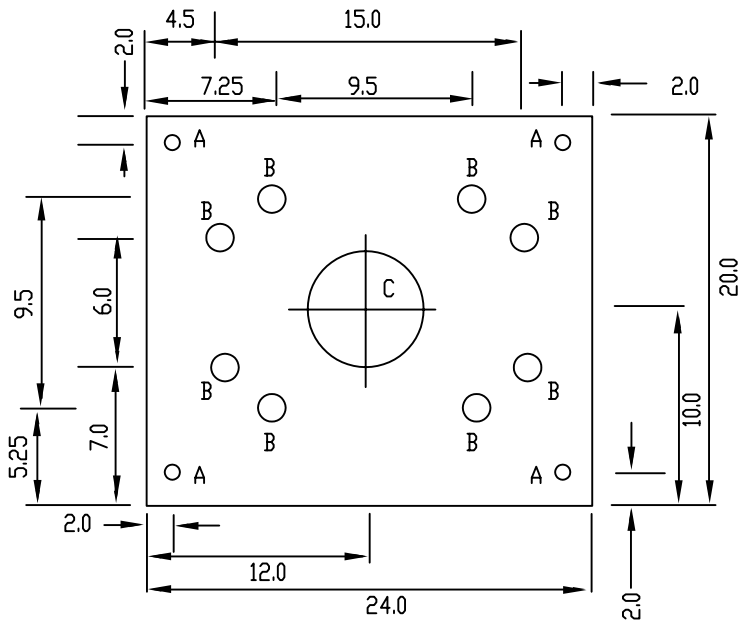


NOTE:

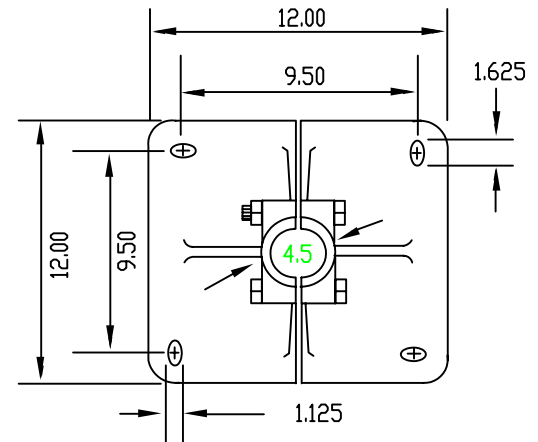
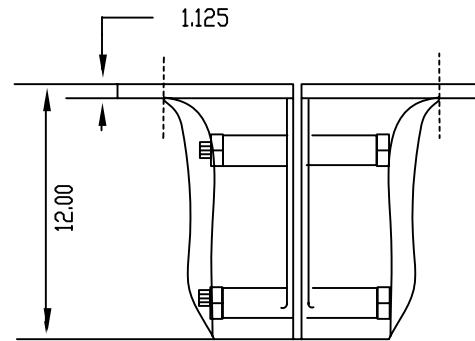
All dimensions shown are in inches.

TITLE:		<p>CABINET HOUSING DETAILS SHEET 3 OF 4</p>
NO SCALE		
TEES 2009		
		<p>A6-3</p>

CABINET HOUSING 2 PEDESTAL ADAPTOR

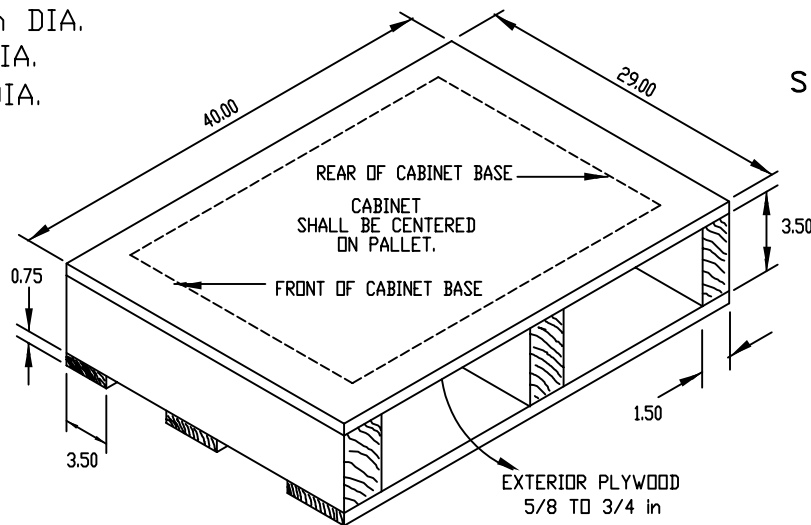


**SLIPFITTER BASE PLATE DETAIL
(0.375 inches ALUMINUM)**



**SLIPFITTER (CAST ALUMINUM)
DETAIL**

- A = 0.50 in DIA.
- B = 1 in DIA.
- C = 5 in DIA.

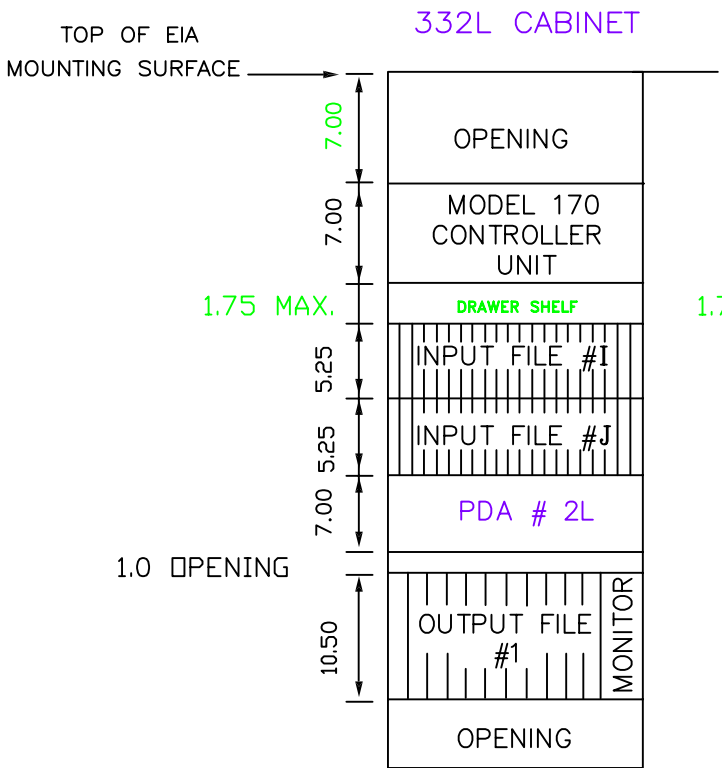


CABINET PALLET

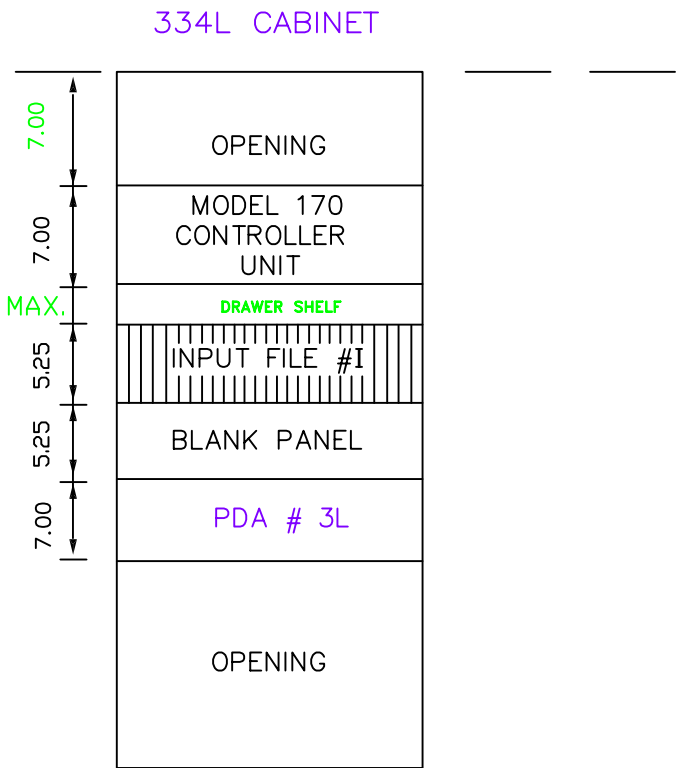
NOTE: (FOR DETAILS A6-1 to A6-4)

1. Housing 1B used in cabinets 332L & 334L and Housing 2 in cabinet 336L.
2. Adaptors delivered separately shall be delivered centered and bolted on a plywood shipping pallet.
3. Dashed lines on cabinet cage support detail delineates the cabinet side wall.
4. The bottom cabinet cage supports shall be continuously welded along the sides of the cabinet & extended to the inside corner of door openings. The top cabinet cage supports shall be continuously welded along the sides of the cabinet.
5. Cage support hole slots dimension shall be common for top & bottom.
6. All dimensions shown are in inches.

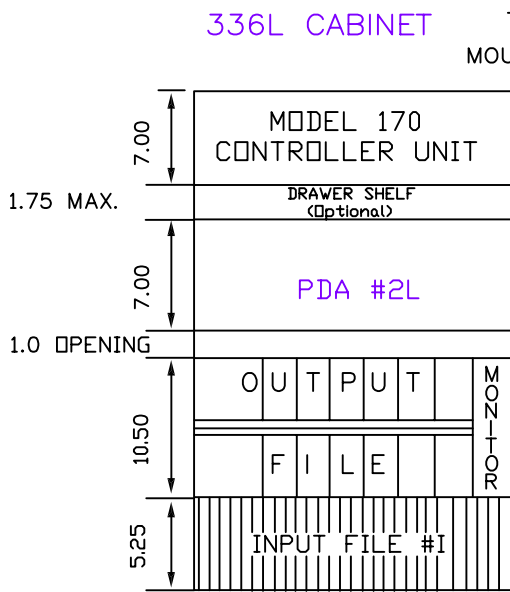
TITLE:	CABINET HOUSING DETAILS SHEET 4 OF 4	
NO SCALE	A6-4	
TEES 2009		



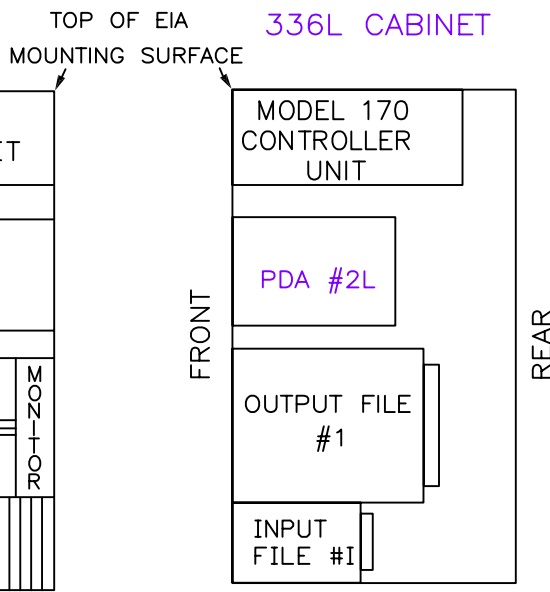
FRONT VIEW



FRONT VIEW



FRONT VIEW



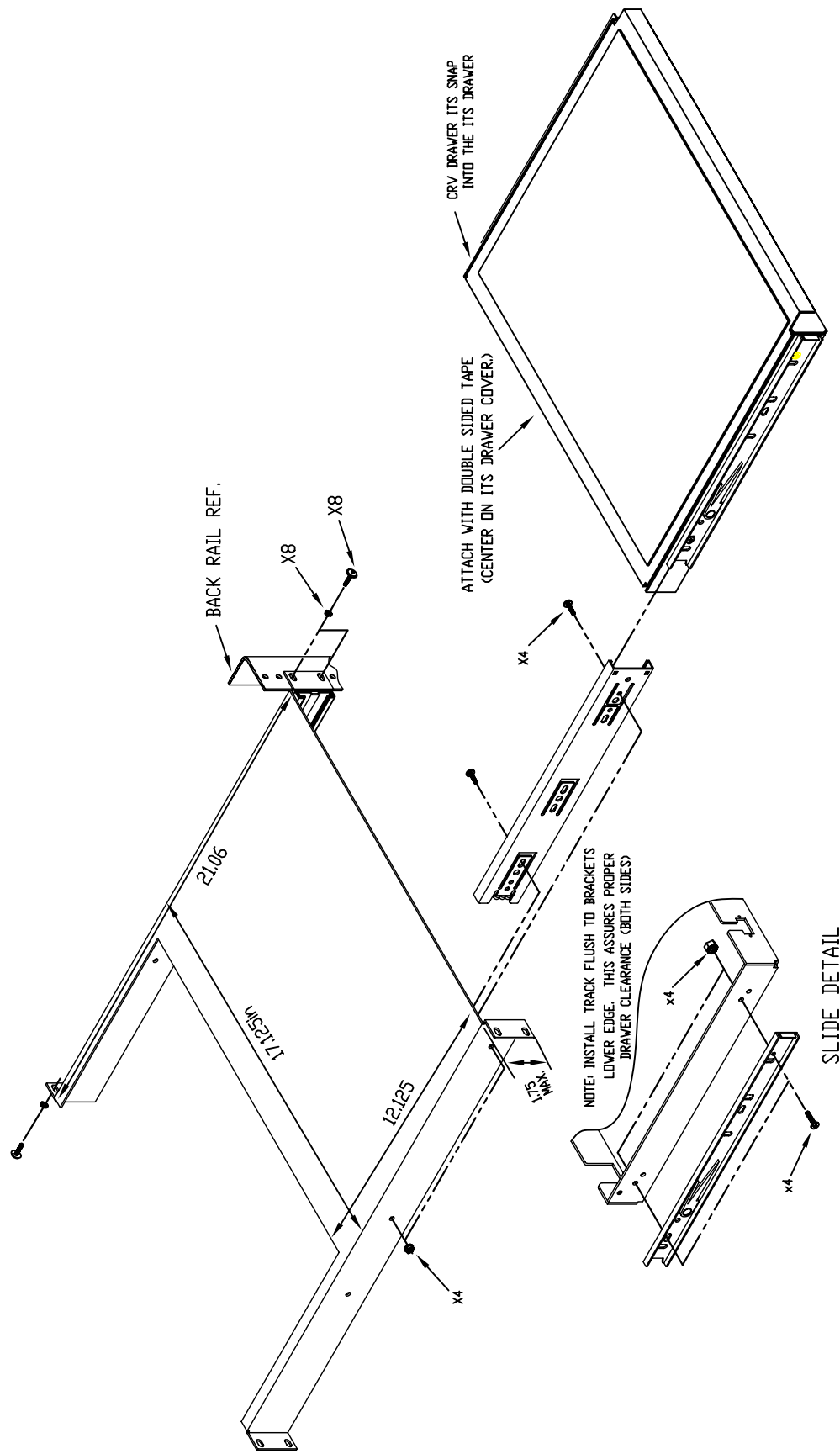
SIDE VIEW

NOTE:

All dimensions shown are in inches.

TITLE:		A6-5
CABINET EQUIPMENT MOUNTING DETAILS		
NO SCALE		
TEES 2009		

DRAWER SHELF UNIT



NOTE:
All dimensions shown are in inches

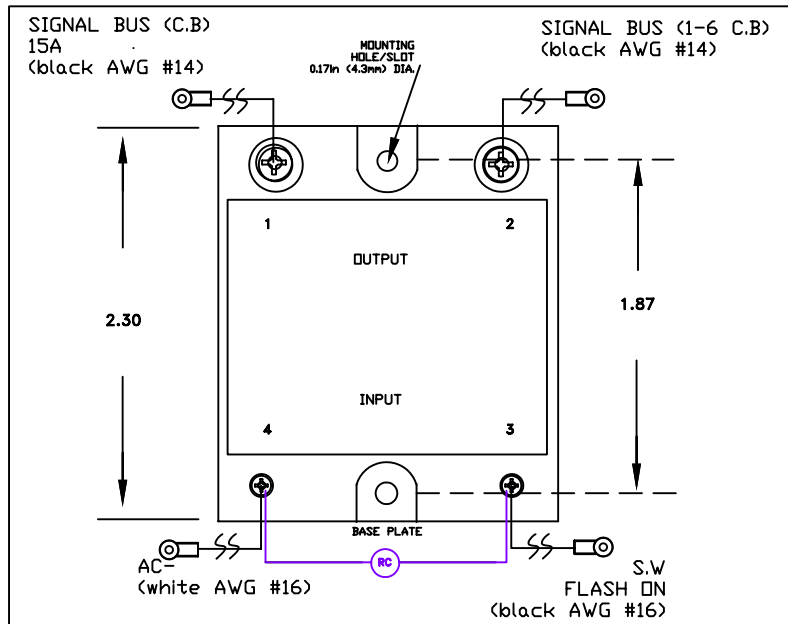
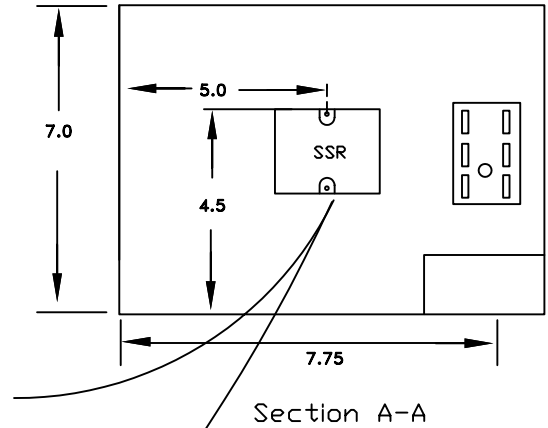
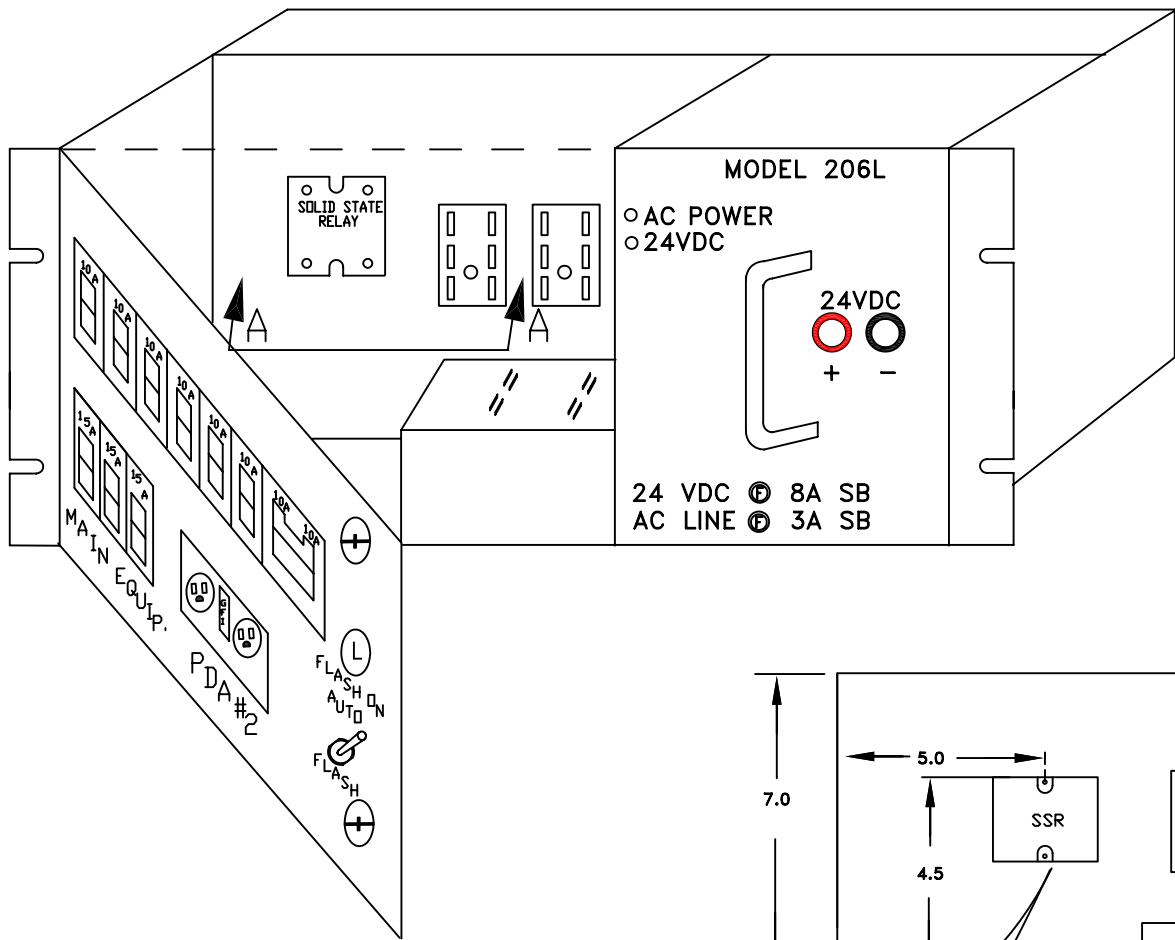
TITLE:

DRAWER SHELF DETAILS

NO SCALE

TEES 2009

A6-6



NOTE:

All dimensions shown are in inches.

TITLE:

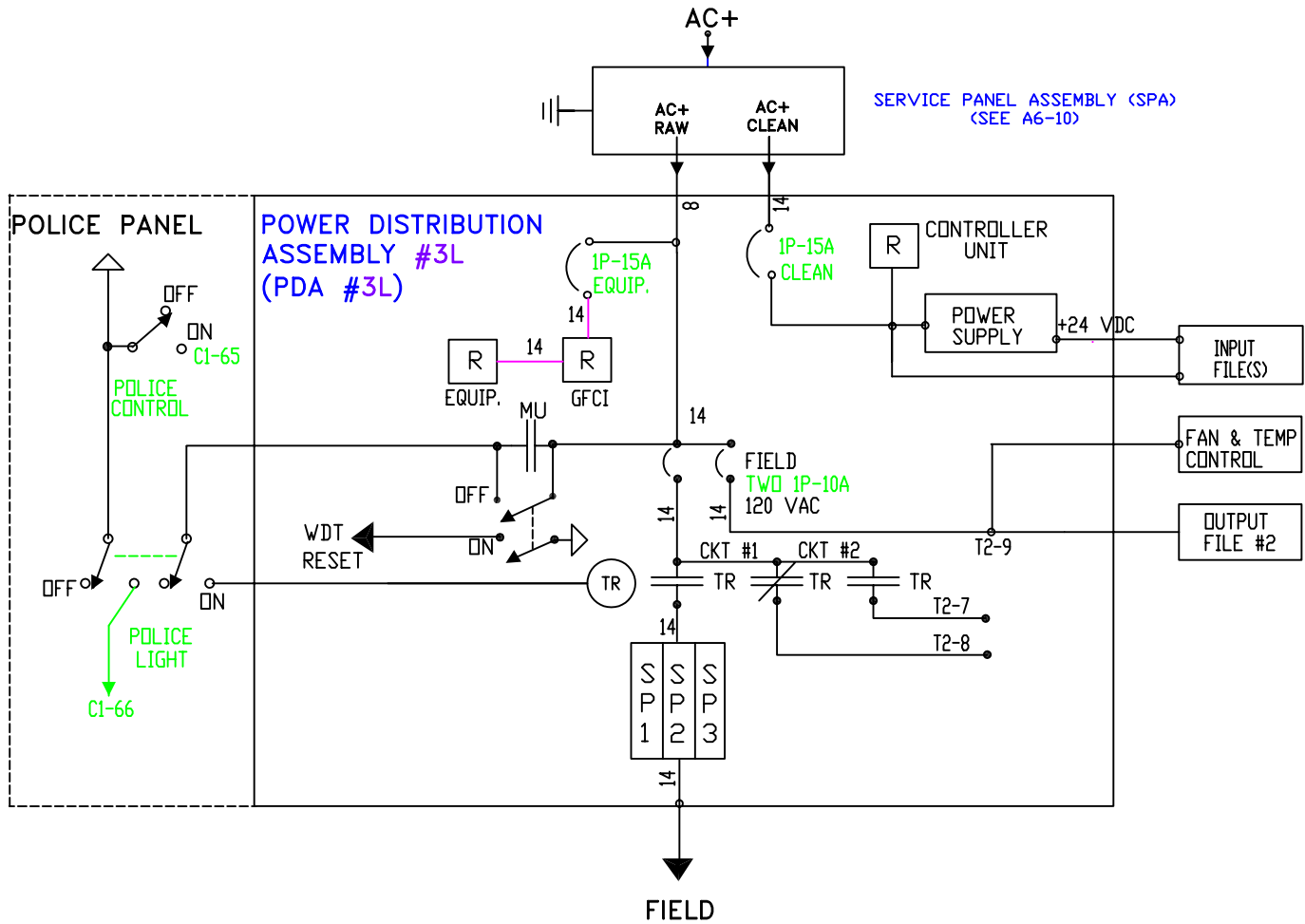
SSR INSTALLATION DETAILS

NO SCALE

TEES 2009

A6-8

334L CABINET ONE LINE DIAGRAM



SHEET DEFINITIONS

TBS	TERMINAL BLOCK - SERVICE	WDT	WATCHDOG TIMER
	EQUIPMENT GROUND	MU	MONITOR UNIT
8	WIRE SIZE, IF NOT INDICATED SHALL BE #16 AWG OR LARGER	CB-1	SIGNAL CIRCUIT BREAKER 1 (SECONDARY)
	CIRCUIT BREAKER	TR	TRANSFER RELAY
	DUPLEX RECEPTACLE	T2-6	TERMINAL BLOCK 2, POSITION 6
WGFI	WITH GROUND FAULT INTERRUPTER	C1-65	C1 CONNECTOR, PIN 65
	RELAY CONTACT, NORMALLY CLOSED	IFI-14J	INPUT FILE 1, TERM. BLOCK 14, TERM. DESTINATION J (CHANNEL 2 INPUT)
	RELAY CONTACT, NORMALLY OPEN		DC GROUND
SPA	SERVICE PANEL ASSEMBLY		SWITCH CONTACT
	FLASHER UNIT ONE		

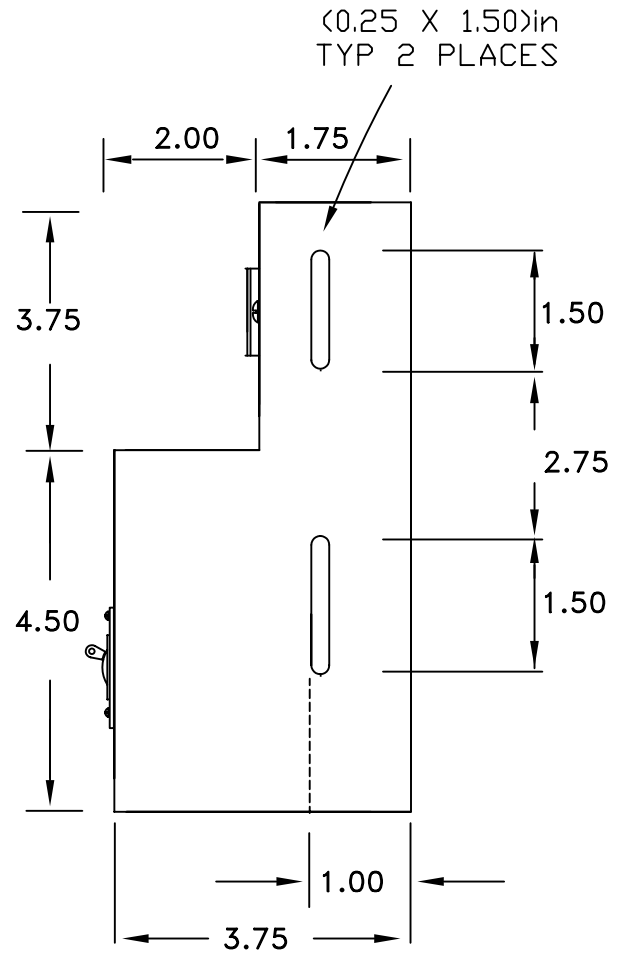
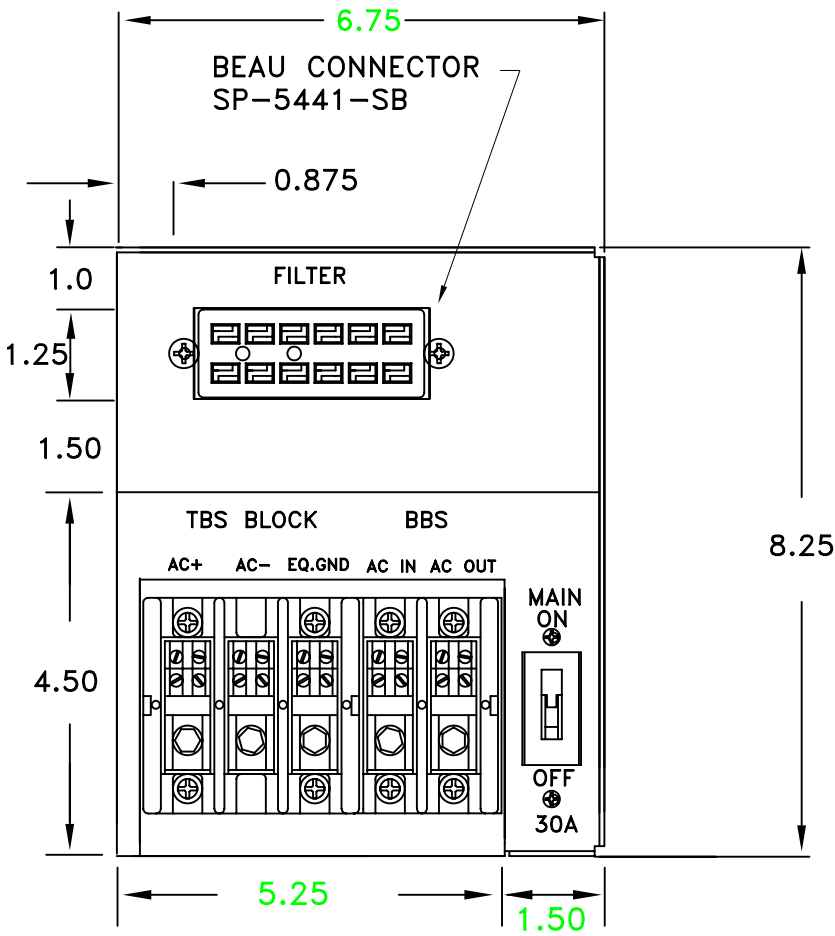
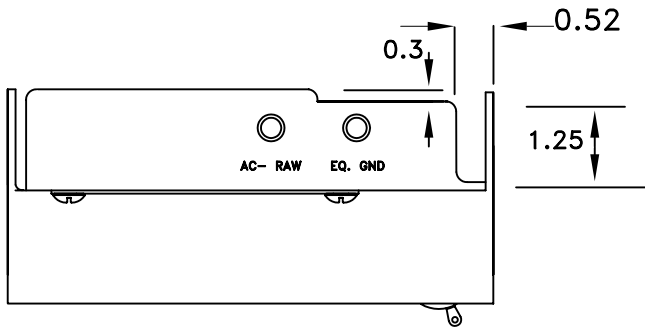
TITLE:

MODEL 334L ONE LINE DIAGRAM

NO SCALE

TEES 2009

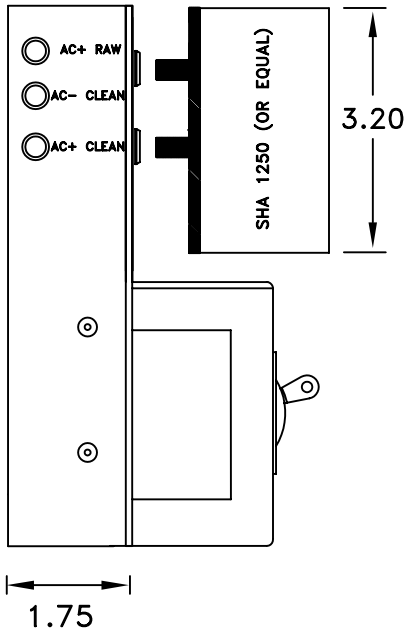
A6-9



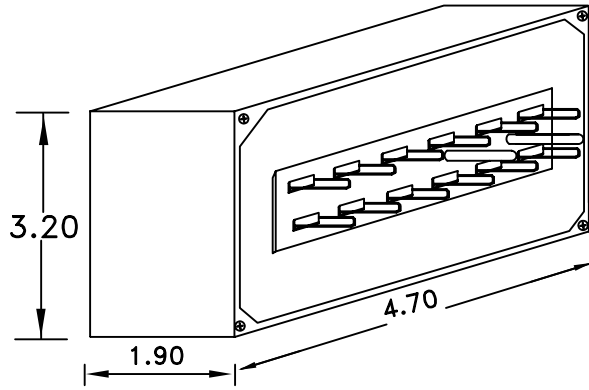
NOTE:

All dimensions shown are in inches.

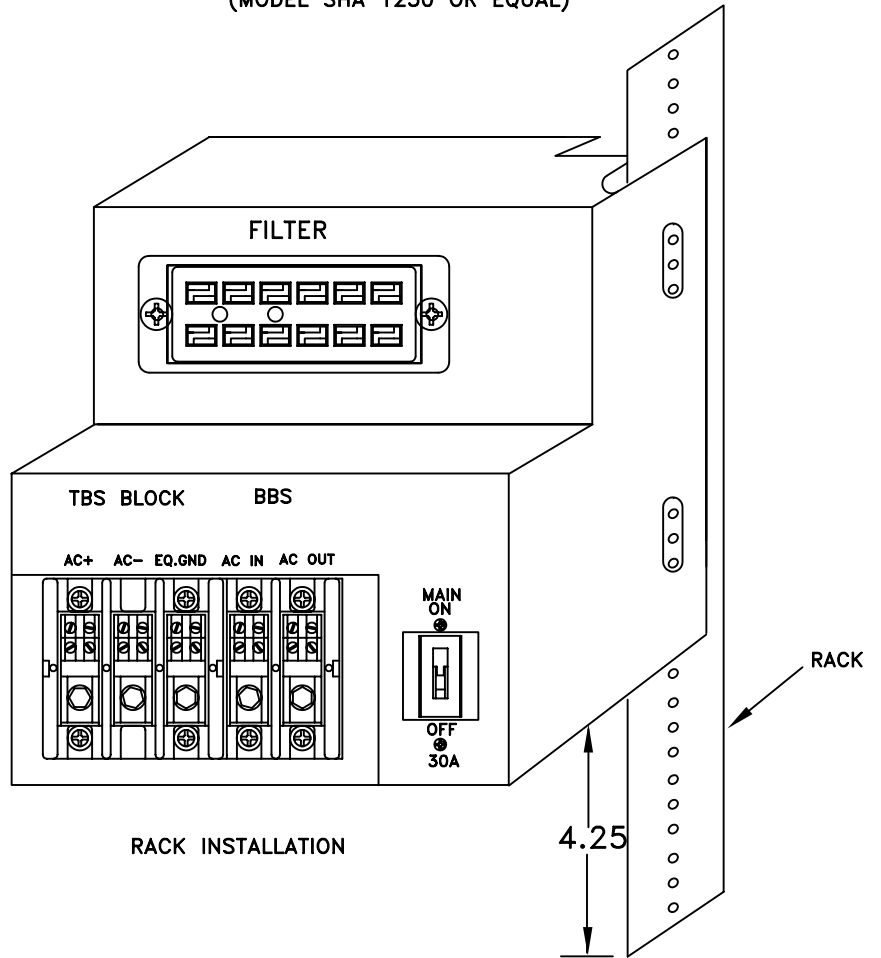
TITLE:	
SERVICE PANEL ASSEMBLY (SPA) DETAILS SHEET 1 OF 3	
NO SCALE	A6-10
TEES 2009	



SIDE VIEW



FILTER
(MODEL SHA 1250 OR EQUAL)

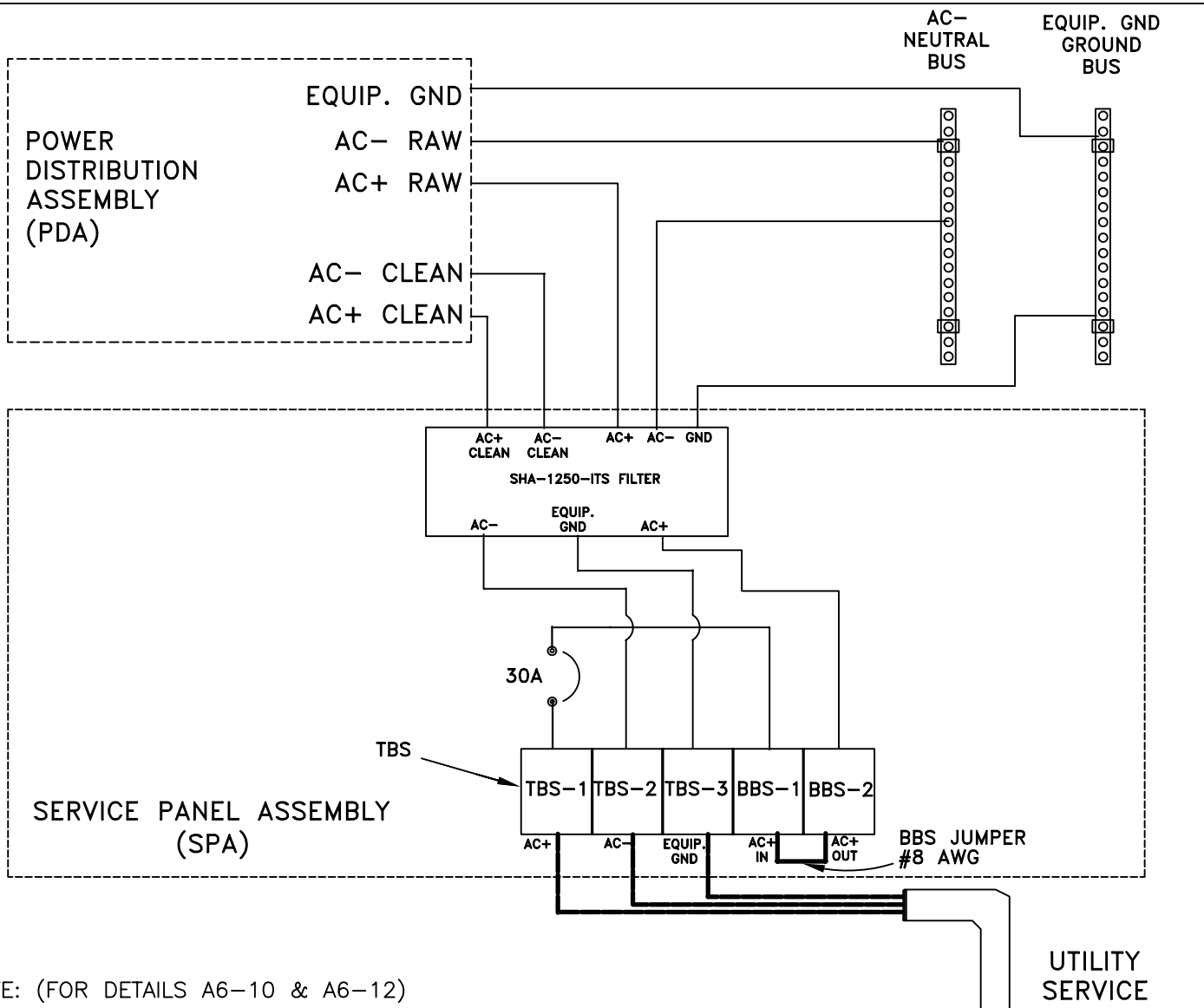


RACK INSTALLATION

NOTES: (FOR THIS DETAIL)

1. The SPA shall be mounted at least 4.25in above the bottom of the cabinet shelf.
2. All dimensions shown are in inches.

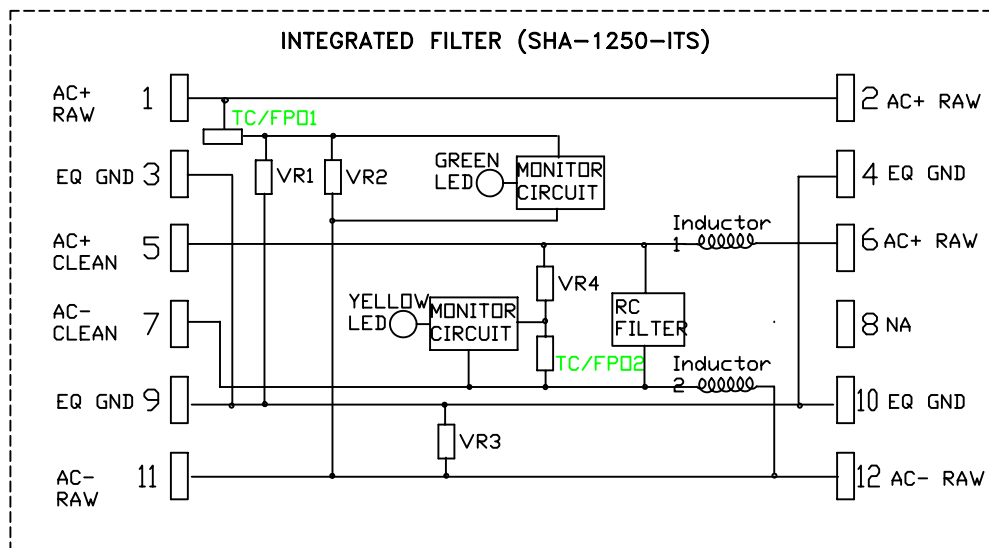
TITLE:	
SERVICE PANEL ASSEMBLY (SPA) DETAILS SHEET 2 OF 3	
NO SCALE	A6-11
TEES 2009	



NOTE: (FOR DETAILS A6-10 & A6-12)

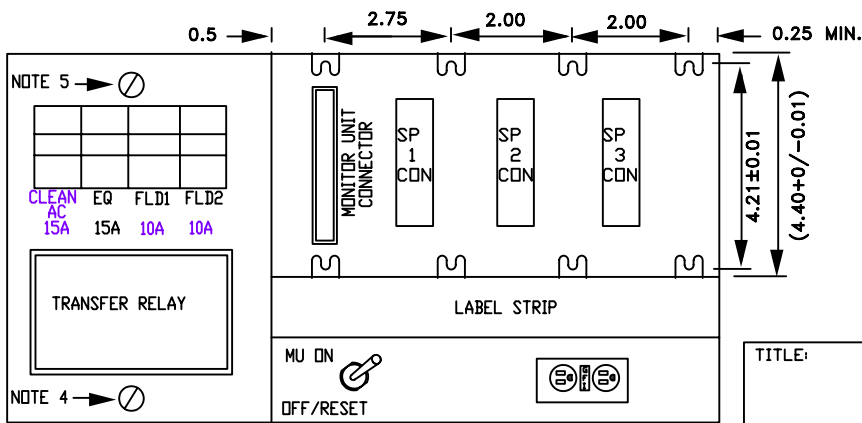
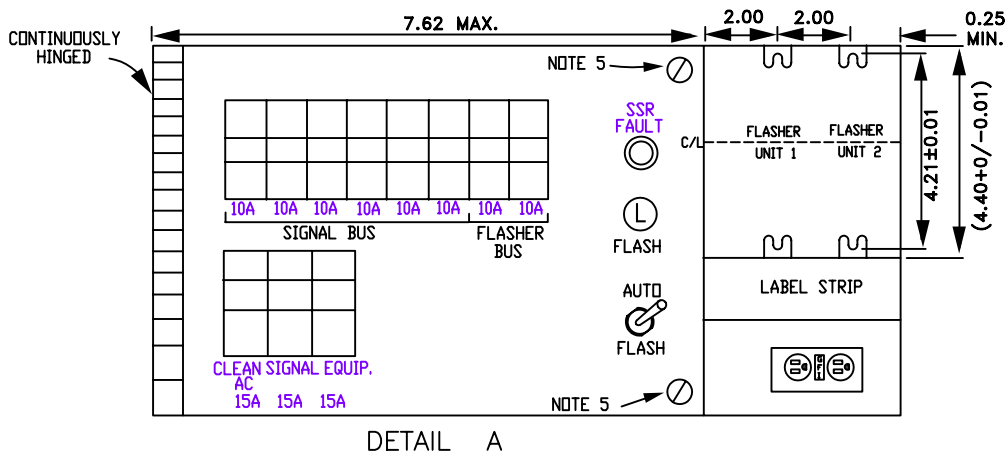
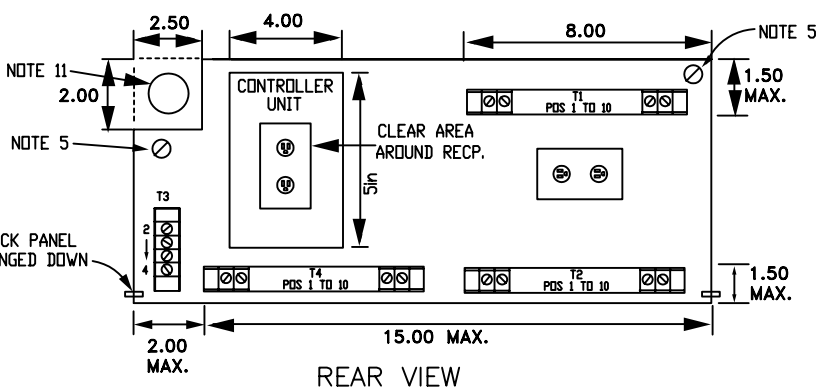
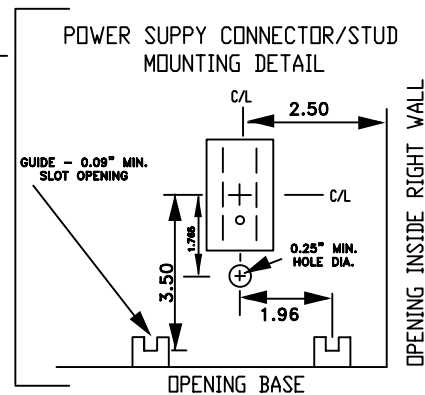
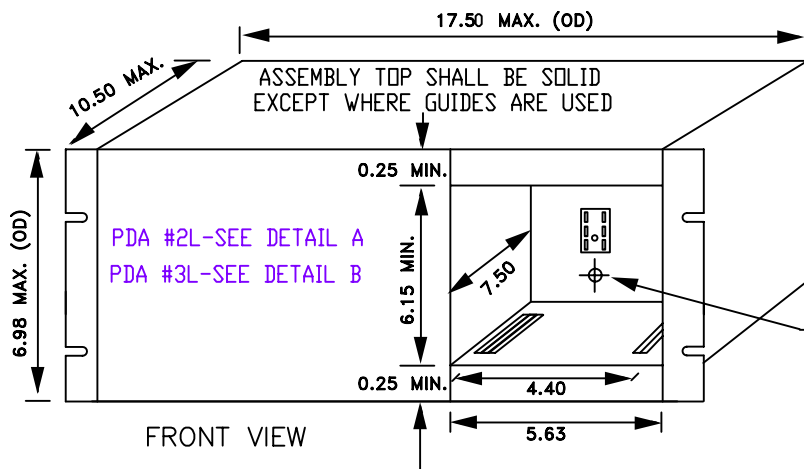
BBS Battery Back-up System
TBS Terminal Block Service

1. VR1,2 and 4 are 100 joule Movistors rated with 200V clamping.
2. VR3 is 135 joule rated Movistors with 250V clamping.
3. TC/FP01 and 2 Thermal Cut Off/Fuse Protection for the Movistors.
4. Inductor 1 and 2 rated 30 MicroHenries at 20A.
5. RC filter system 10 DB at 10 KHZ, 50 DB at 100 KHZ and 90 DB at 1 Mhz.



6. GREEN LED Indicator ON= ok, OFF= error.
7. YELLOW LED ON= error, Off= ok.
8. Remove jumper when connecting BBS.

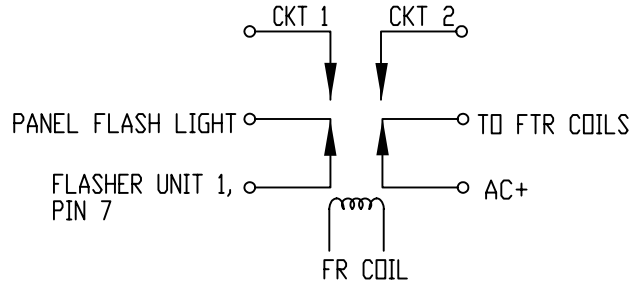
TITLE: SERVICE PANEL ASSEMBLY (SPA) DETAILS SHEET 3 OF 3	
NO SCALE	A6-12
TEES 2009	



NOTE:
All dimensions shown are in inches.

TITLE: PDA #2L & #3L DETAILS SHEET 1 OF 3	
NO SCALE	A6-13
TEES 2009	

FLASH RELAY CONNECTOR SOCKET WIRING DETAIL



FLASHER UNIT CONNECTOR SOCKET WIRING DETAIL

PIN NO.	CIRCUIT	PIN NO.	CIRCUIT
7	LD Ckt #1	10	AC- CLEAN
8	LD Ckt #2	11	AC+ CLEAN
9	EG	12	NA

TITLE:

PDA #2L & #3L DETAILS
SHEET 2 OF 3

NO SCALE

TEES 2008

A6-14

POWER DISTRIBUTION ASSEMBLY TERMINAL BLOCK ASSIGNMENT DETAIL

BLOCK	T1	T2		T3	T4	
PDA's POS	2A/B (3A/B - NA)	2A/B	3A/B	2 & 3A/B	2A/B	3A/B
1.	EG BUS / EG	* / ER AC-	EG BUS / EQ GND	+24VDC BUS / PS-7	NA / NA	FL1 / SP 3-3
2.	AC- BUS / AC-	01-5 / FU1-7	AC- BUS / AC-	NA / PS-7	NA / NA	FL2 / SP 3-5
3.	CR AC- / AC- CLEAN	01-6 / FU1-8	* / MCB(SEC)	DC GND BUS / PS 8	NA / NA	FL3 / SP 3-7
4.	03-5 / SCB CKT 5	01-7 / FU2-7	* / MCB(SEC)	NA / PS-8	NA / NA	FL4 / SP 2-3
5.	* / MCB (SEC)	01-8 / FU2-8	* / MU		NA / NA	FL5 / SP 2-5
6.	CR AC+ / AC+ CLEAN	* / TR NC CKT	* / TR COIL		NA / NA	FL6 / SP 2-7
7.	* / SSR	01-1 / SCB CKT 1	NA / TRC2ND		NA / NA	FL7 / SP 1-3
8.	03-6 / SCB CKT 6	01-2 / SCB CKT 2	NA / TRC2NC		NA / NA	FL8 / SP 1-5
9.	* / FCBI (SEC)	01-3 / SCB CKT 3	03-5 / FLD2		NA / NA	FL9 / SP 1-7
10.	* / ER AC+	01-4 / SCB CKT 4	NA / NA		NA / NA	NA / NA

A = EXTERNAL SIDE B = INTERNAL SIDE * = WIRE PER ONE LINE DIAGRAM

NOTES: (FOR DETAILS A6-13 TO A6-15)

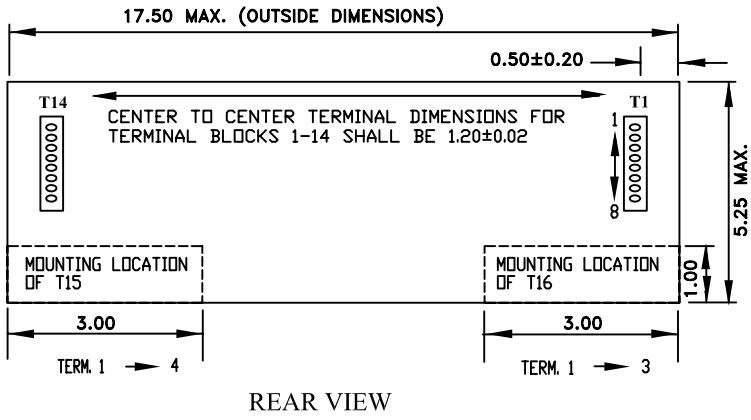
- All dimensions shown are in inches.
- SHEET DEFINITIONS:

CKT = CIRCUIT	EG = EQUIPMENT GROUND
FLD1 = FIELD 1 CIRCUIT BREAKER	FL1 = FIELD LOAD 1
FU1-7 = FLASHER UNIT #1, PIN 7	ER = EQUIPMENT RECEPTACLE
L = LAMP	LD CKT#1 = LOAD CIRCUIT 1
SSR = SOLID STATE RELAY	MCB = MAIN CIRCUIT BREAKER
MN = MAIN	MU-22 = MONITOR UNIT - PIN 22
OD = OUTSIDE DIMENSION	POS = POSITION
PS-7 = POWER SUPPLY PIN 7	SCB = SIGNAL CIRCUIT BREAKER
SP 3-3 = SWITCH PACK 3, PIN 3	TR = TRANSFER RELAY
01-8 = OUTPUT FILE TB 01, POSITION 8	FCBI = FIELD CIRCUIT BREAKER 1
	CR = CONTROL RECEPTACLE

- "U" sharpened rod handle fabricated of 0.25±0.05 diameter, aluminum stock, with 4.00±0.125 length, & rod center to center, shall be provided. The handle shall be vertically centered. The depth from the vertical centerline of the handle rod to the module from panel shall be 1.25±0.125.
- The power supply module dimension, from panel to connector plug, shall be 7.375 +0.000, -0.125.
- Thumb screw device.
- A standard 8-32 metal stud retaining screw shall provide proper securing of the power supply when installed in the PDA using washers and a wingnut. When torqued in the locking position no stress shall be applied on the mating socket/plug connector surface. No mounting of chassis support screws shall protrude beyond the mating surface of the power supply connector.
- Top of the transfer relay shall be flush with the front of the PDA #1 Assembly. Relay in PDA #2L & #3L shall extend no more than 1.0 inch out from the assembly front face.
- Slack shall be provided in the wiring for the circuit breakers and GFI receptacle to allow for the removal and repair. Excess bends and stress on the wiring shall be minimized.
- See output file plan sheet for heavy duty relay and switch pack wiring assignments and connector mounting location.
- Wiring shall be routed (with extra length) to minimize movement when front panel door is opened. The wiring going to the front panel shall be routed such that it does not cause undue twisting or bending of the wires.
- No ventilation hole shall be large enough to place a 0.375 inch diameter object through.
- The C5P support connector and support bracket shall be installed (wiring NA) in the PDA #2L. If PDA #2L is used, the input panel C5P connector is not required and harness #2L - C5S connector shall be connected to PDA #2L C5P. The C6P connector and support bracket shall be installed in PDA #3L.

TITLE:		PDA #2L & #3L DETAILS SHEET 3 OF 3
NO SCALE	A6-15	
TEES 2009		

INPUT FILE DETAIL



INPUT FILE TERMINAL ASSIGNMENT DETAIL

T1 - 14

TERM	PIN - FUNCTION
1	SP - SPARE
2	F - CHANNEL 1 OUTPUT
3	W - CHANNEL 2 OUTPUT
4	D - CHANNEL 1 INPUT
5	E - CHANNEL 1 INPUT
6	J - CHANNEL 2 INPUT
7	K - CHANNEL 2 INPUT
8	L - EQUIP. GROUND

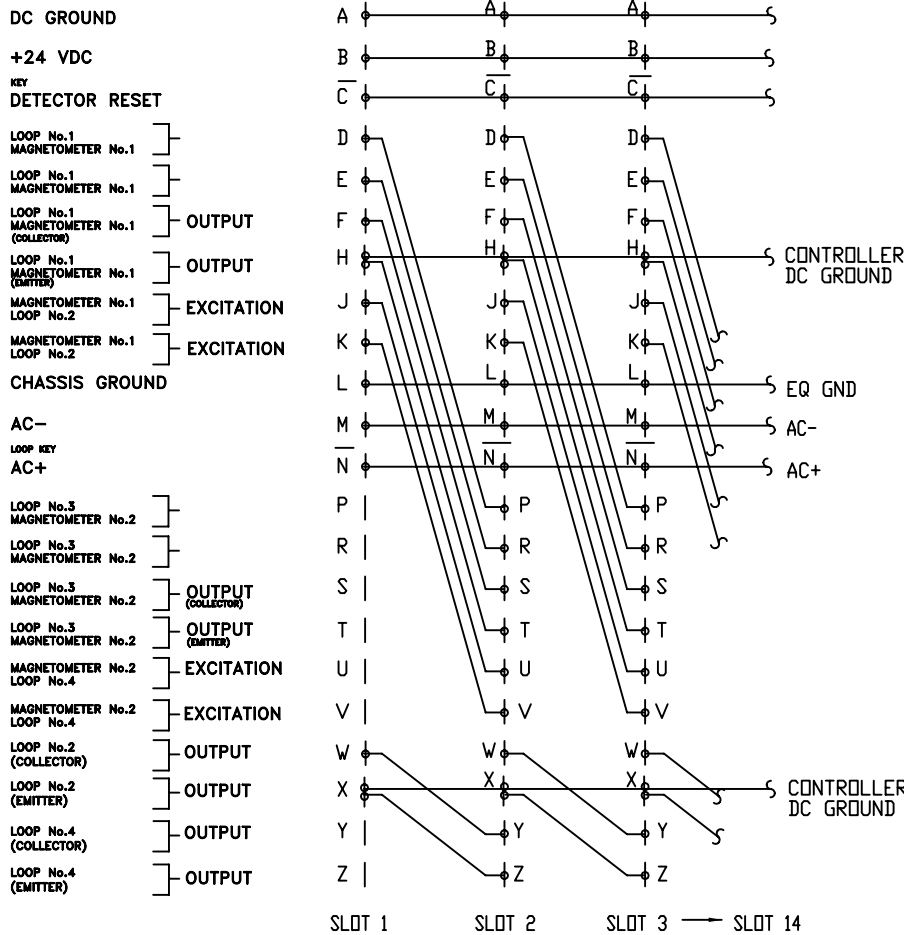
T15

TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	DETECTOR RESET
4	C1 HARNESS DC GROUND

T16

TERM	FUNCTION
1	AC+ CLEAN
2	AC- CLEAN
3	EQUIP. GROUND

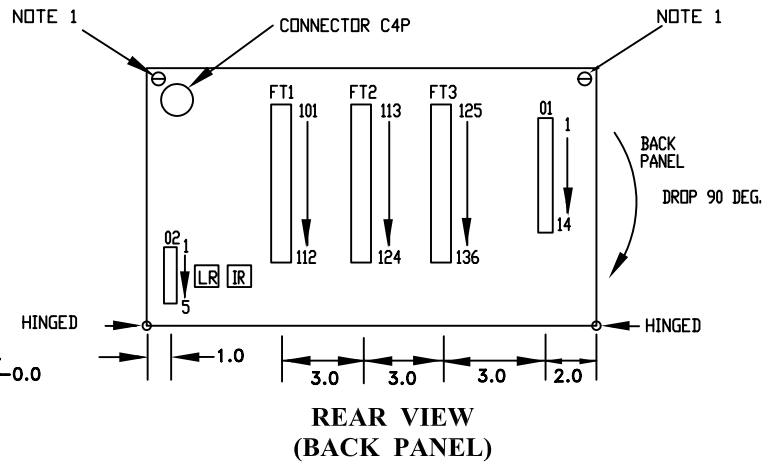
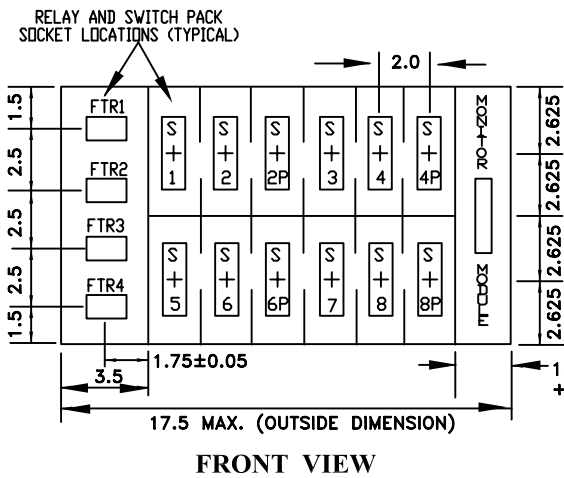
INPUT FILE WIRING DIAGRAM



NOTE:
All dimensions shown are in inches.

TITLE:		INPUT/OUTPUT FILE DETAILS SHEET 1 OF 5
NO SCALE		
TEES 2009		
		A6-16

OUTPUT FILE #1 DETAIL



OUTPUT FILE #1 TERMINAL ASSIGNMENT DETAIL

01 TERM	FUNCTION
1	PDA CKT1/SWPKS 1,2,2P-1
2	PDA CKT2/SWPKS 3,4,4P-1
3	PDA CKT3/SWPKS 5,6,6P-1
4	PDA CKT4/SWPKS 7,8,8P-1
5	PDA FU1 CKT1/FTR1
6	PDA FU1 CKT2/FTR2
7	PDA FU2 CKT1/FTR3
8	PDA FU2 CKT2/FTR4
9	EQUIP. GROUND
10	AC-
11	AC+ (FROM PDA)
12	SSR (TO PDA)
13	DOOR SW. (FROM POL PAN)
14	FTR COILS (TO)

02 TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	IFI - 14J, STOPTIME (FROM MU)
4	IFI - 14D, FLASH SENSE (FROM IR)
5	EXTERNAL RESET (TO MU)

FT1 TERM	FUNCTION	FT2 TERM	FUNCTION	FT3 TERM	FUNCTION
101	SWPK 4-RED	113	SWPK 2P-RED	125	SWPK 1-RED
102	SWPK 4-YEL	114	SWPK 2P-YEL	126	SWPK 1-YEL
103	SWPK 4-GRN	115	SWPK 2P-GRN	127	SWPK 1-GRN
104	SWPK 4P-RED	116	SWPK 3-RED	128	SWPK 2-RED
105	SWPK 4P-YEL	117	SWPK 3-YEL	129	SWPK 2-YEL
106	SWPK 4P-GRN	118	SWPK 3-GRN	130	SWPK 2-GRN
107	SWPK 8-RED	119	SWPK 6P-RED	131	SWPK 5-RED
108	SWPK 8-YEL	120	SWPK 6P-YEL	132	SWPK 5-YEL
109	SWPK 8-GRN	121	SWPK 6P-GRN	133	SWPK 5-GRN
110	SWPK 8P-RED	122	SWPK 7-RED	134	SWPK 6-RED
111	SWPK 8P-YEL	123	SWPK 7-YEL	135	SWPK 6-YEL
112	SWPK 8P-GRN	124	SWPK 7-GRN	136	SWPK 6-GRN

NOTE:

1. Thumb screws device
2. All dimensions shown are in inches

TITLE:

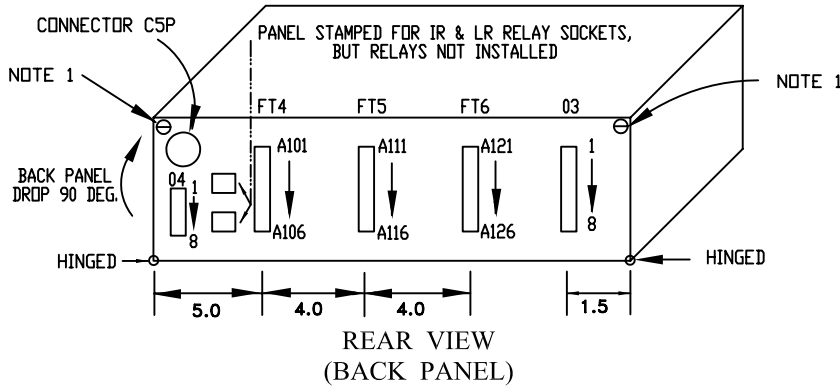
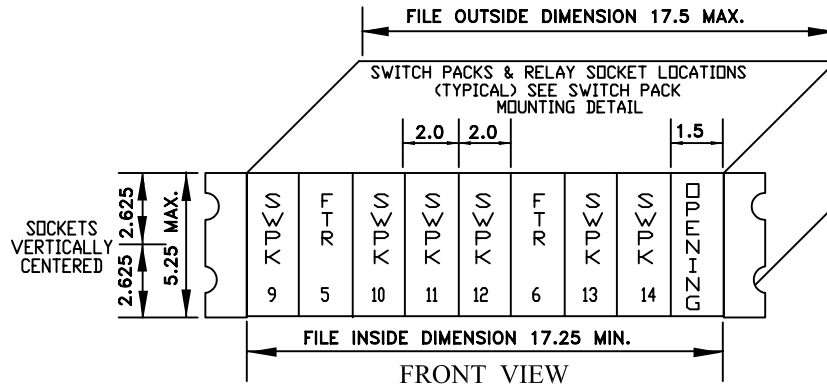
INPUT/OUTPUT FILE DETAILS
SHEET 2 OF 5

NO SCALE

TEES 2009

A6-17

OUTPUT FILE #2 DETAIL



OUTPUT FILE #2 TERMINAL ASSIGNMENT DETAIL

O3 TERM	FUNCTION
1	PDA FU1 CKT1/FTR5
2	PDA FU2 CKT2/FTR6
3	FTR COILS (TO)
4	AC-
5	PDA CKT5/SWPKS 9,10,11-1
6	PDA CKT6/SWPKS 12,13,14-1
7	EQUIP. GROUND
8	AC+ (FROM PDA)

O4 TERM	FUNCTION
1	+24 VDC
2	DC GROUND
3	STOPTIME
4	FLASH SENSE
5	EXTERNAL RESET
6	WDT INPUT
7	LR COIL (UNIT IN)
8	MC COIL (PDA)

FT4 TERM	FUNCTION	FT5 TERM	FUNCTION	FT6 TERM	FUNCTION
A101	SWPK 13-RED	A111	SWPK 11-RED	A121	SWPK 9-RED
A102	SWPK 13-YEL	A112	SWPK 11-YEL	A122	SWPK 9-YEL
A103	SWPK 13-GRN	A113	SWPK 11-GRN	A123	SWPK 9-GRN
A104	SWPK 14-RED	A114	SWPK 12-RED	A124	SWPK 10-RED
A105	SWPK 14-YEL	A115	SWPK 12-YEL	A125	SWPK 10-YEL
A106	SWPK 14-GRN	A116	SWPK 12-GRN	A126	SWPK 10-GRN

NOTE:

1. Thumb screws device.
2. All dimensions shown are in inches.

TITLE:

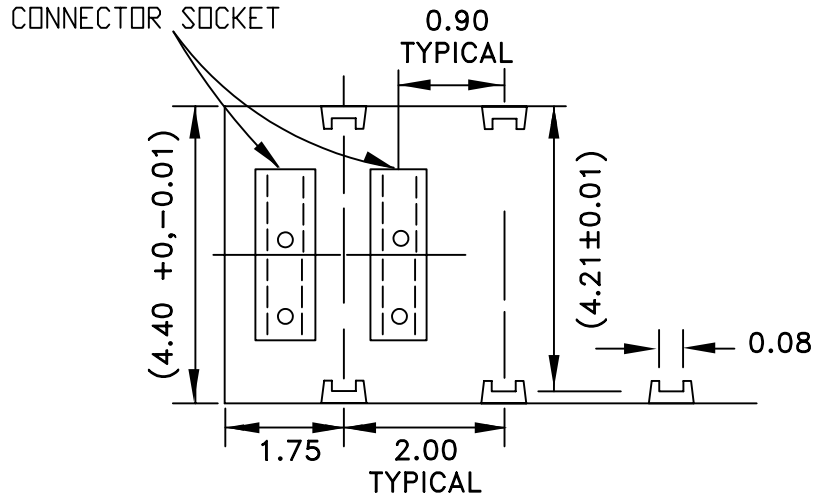
INPUT/OUTPUT FILE DETAILS
SHEET 3 OF 5

NO SCALE

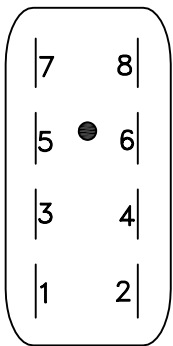
TEES 2009

A6-18

SWITCH PACK MOUNTING DETAIL



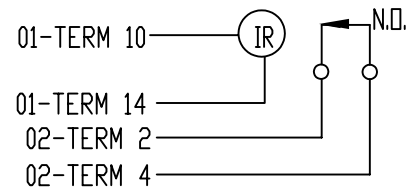
HEAVY DUTY RELAY SOCKET DETAIL



REAR VIEW

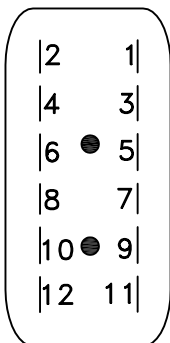
PIN	FUNCTION
1	COIL
2	COIL
3	N.C. CIRCUIT #1
4	N.C. CIRCUIT #2
5	COMMON CIRCUIT #1
6	COMMON CIRCUIT #2
7	N.O. CIRCUIT #1
8	N.O. CIRCUIT #2

ISOLATION RELAY (IR) DETAIL



(Refer to detail A6-16)

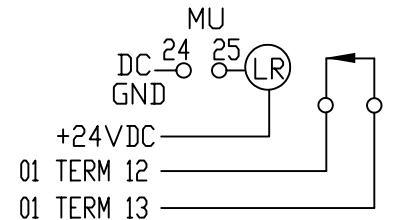
SWITCH PACK SOCKET DETAIL



REAR VIEW

PIN	FUNCTION
1	AC+
2	EQUIP. GROUND
3	RED OUTPUT
4	NA
5	YELLOW OUTPUT
6	RED INPUT
7	GREEN OUTPUT
8	YELLOW INPUT
9	+24 VDC
10	GREEN INPUT
11	NA
12	NA

LOGIC RELAY (LR) DETAIL



(Refer to detail A6-16)

NOTE:

All dimensions shown are in inches

TITLE:

INPUT/OUTPUT FILE MU DETAILS
SHEET 4 OF 5

NO SCALE

TEES 2009

A6-19

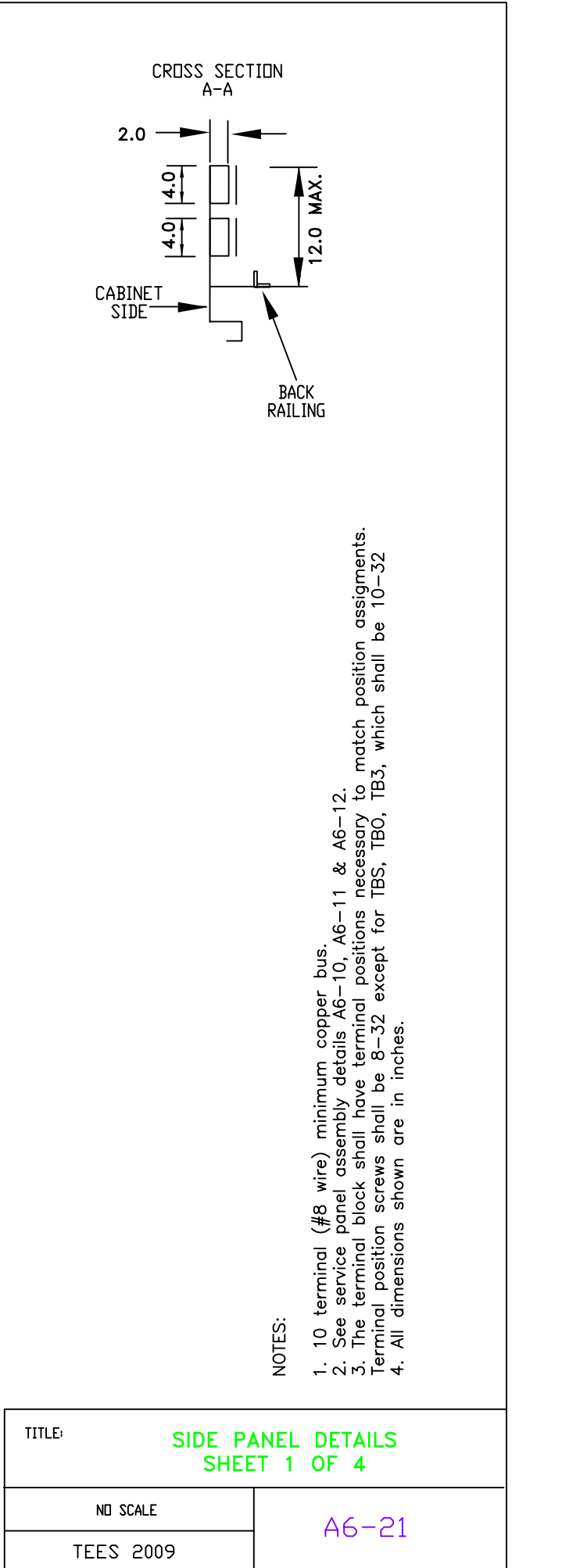
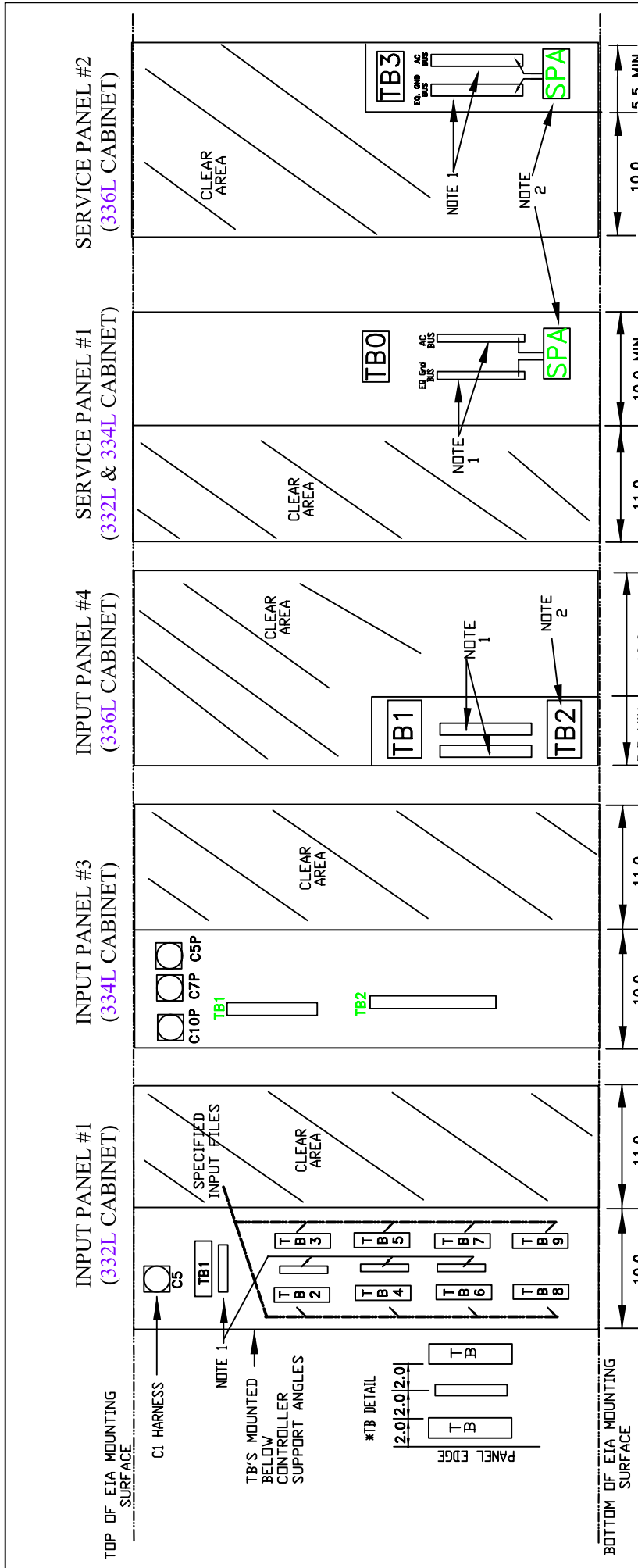
MODEL 210 MONITOR UNIT PIN ASSIGNMENT

CONNECTOR PIN No.	MONITOR FUNCTION	TERMINATION	CONNECTOR PIN No.	MONITOR FUNCTION	TERMINATION
1	SWPKS 2 GRN		A	SWPKS 2 YEL	
2	SWPKS 2P GRN		B	SWPKS 6 GRN	
3	SWPKS 6 YEL		C	SWPKS 6P GRN	
4	SWPKS 4 GRN		D	SWPKS 4 YEL	
5	SWPKS 4P GRN		E	SWPKS 8 GRN	
6	SWPKS 8 YEL		F	SWPKS 8P GRN	
7	SWPKS 5 GRN		H	SWPKS 5 YEL	
8	T & B		J	SWPKS 1 GRN	
9	SWPKS 1 YEL		K	T & B	
10	SWPKS 7 GRN		L	SWPKS 7 YEL	
11	T & B		M	SWPKS 3 GRN	
12	SWPKS 3 YEL		N	T & B	
13	T & B		P	NA	
14	NA		R	T & B	
15	T & B		S	T & B	
16	T & B		T	NA	
17	NA		U	T & B	
18	T & B		V	T & B	
19	NA		W	NA	
20	EQUIP. GROUND	01-TERM 9	X	NA	
21	AC-	01-TERM 10	Y	DC GROUND	02-TERM 2
22	WATCHDOG TIMER	C4-37	Z	EXTERNAL RESET	02-TERM 5
23	+24 VDC	02-TERM 1	AA	T & B	
24	B.D. OUT CKT	LOGIC RELAY COIL	BB	STOPTIME	02-TERM 3
25	B.D. OUT CKT	DC GROUND	CC	NA	
26	NA		DD	NA	
27	NA		EE	OUTPUT SW-SIDE 2	01-TERM 12
28	OUTPUT-SW SIDE 1	AC+	FF	AC+	01-TERM 11

NOTES: (FOR DETAILS A16-20)

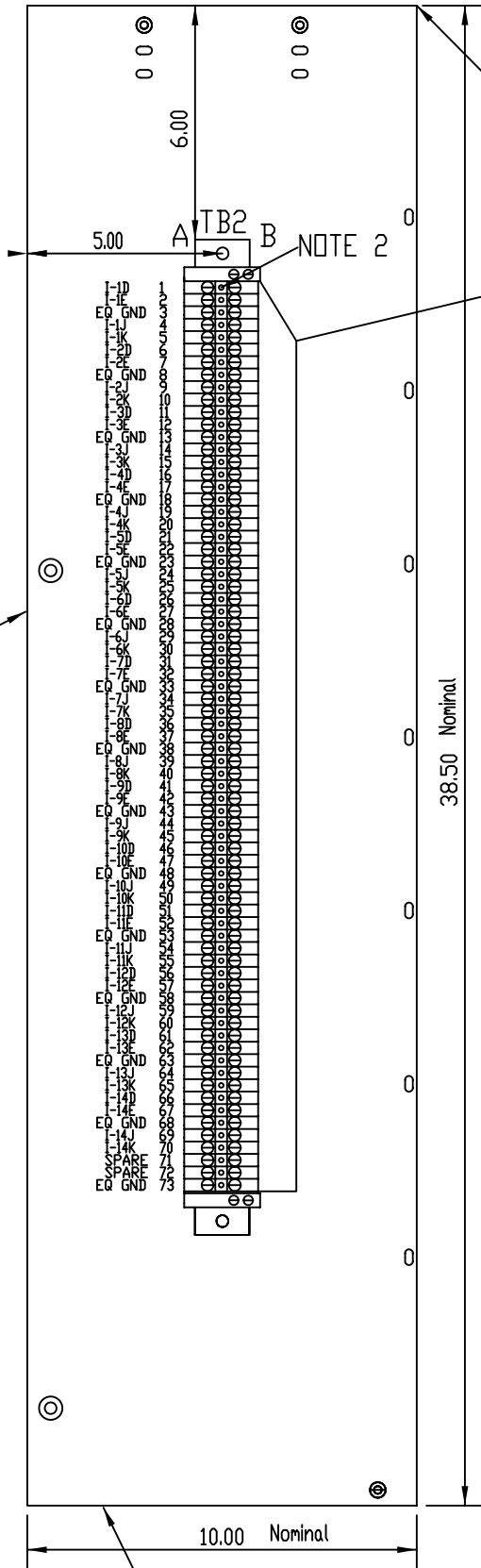
- Top of relays shall be flush with face of file.
- The isolation relay shall be potter & brumfield R10-E1-X2-115 (or equal). The logic relay (LR) shall be potter & brumfield KUP11(D11 or 15) or equal.
- See connectors C4 & C5 wiring lists for connector/file interface.
- Sheet definitions:
 CKT = CIRCUIT
 FU = FLASHER UNIT
 FTR = FLASH TRANSFER RELAY
 IFI-14D = INPUT FILE "I", TB 14, TERMINAL D
 SSR = SOLID STATE RELAY
 MU = MONITOR UNIT
 N.C. = NORMALLY CLOSED RELAY CIRCUIT
 N.O = NORMALLY OPEN RELAY CIRCUIT
 PDA FU1 CKT1 = PDA FLASHER UNIT 1, OUTPUT CIRCUIT 1
 POL PAN = POLICE PANEL
 SW = SWITCH
 SWPK(S) = SWITCH PACK(S)
 T&B = CONDUCTORS CONNECTED TO PIN,
 Two feet in length with ring lug on unconnected end, tied & bundled separately.
 2P-1 = PHASE 2 PED. PIN
- All dimensions shown are in inches.

TITLE:		INPUT/OUTPUT FILE DETAILS SHEET 5 OF 5
NO SCALE	A6-20	
TEES 2009		



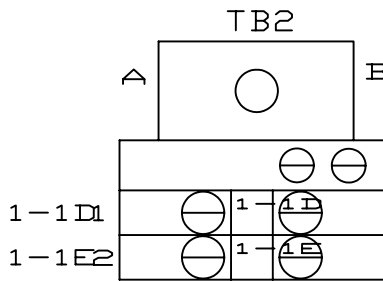
- NOTES:
1. 10 terminal (#8 wire) minimum copper bus.
 2. See service panel assembly details A6-10, A6-11 & A6-12.
 3. The terminal block shall have terminal positions necessary to match position assignments. Terminal position screws shall be 8-32 except for TBS, TBO, TB3, which shall be 10-32
 4. All dimensions shown are in inches.

TITLE: SIDE PANEL DETAILS SHEET 1 OF 4	
NO SCALE	A6-21
TEES 2009	



Panel Continuous or Two Sections (upper and lower)

Specified Input File I Terminals.



LABELING ON PANEL AND TERMINAL BLOCK.

NOTES:

1. Provide and install a 73 position TB2 Terminal Block. TB2 shall be a USK 10 Open Construction Phoenix Contact Terminal Blocks (or equal) mounted on DIN Railing (supported every 6 inches) with position function label tabs and positions commoned and end locks.
2. All terminals to be labeled using manufacturer recommended plastic labels as shown above.
3. All dimensions shown are in inches.

TITLE:

SIDE PANEL DETAILS
SHEET 3 OF 4

No Scale

TEES 2009

A6-23

INPUT PANEL #1
TERMINAL BLOCK ASSIGNMENT DETAIL

POS	A	B	POS	A	B	POS	A	B
TB1 - * SEE INPUT PANEL #4 TB1 ASSIGNMENTS			TB4-1		I-4D	TB7-1	DET 33	J-7D
			TB4-2	DET 7	I-4E	TB7-2		J-7E
			TB4-3		I-4J	TB7-3		J-7J
			TB4-4	DET 8	I-4K	TB7-4	DET 34	J-7K
			TB4-5		I-5D	TB7-5	DET 35	J-8D
			TB4-6		I-5E	TB7-6		J-8E
			TB4-7	DET 10	I-5J	TB7-7	DET 36	J-8J
			TB4-8		I-5K	TB7-8		J-8K
			TB4-9	DET 11	I-6D	TB7-9	DET 37	J-9D
			TB4-10		I-6E	TB7-10		J-9E
			TB4-11	DET 12	I-6J	TB7-11	DET 38	J-9J
			TB4-12		I-6K	TB7-12		J-9K
TB2-1		I-1D	TB5-1	DET 25	J-4D	TB8-1	MANUAL	I-11D
TB2-2	DET 1	I-1E	TB5-2		J-4E	TB8-2	SPARE	I-11J
TB2-3		I-1J	TB5-3	DET 26	J-4J	TB8-3	11 COM	I-11K
TB2-4	DET 2	I-1K	TB5-4		J-4K	TB8-4	PED Ø2	I-12D
TB2-5		I-2D	TB5-5		J-5D	TB8-5	PED Ø4	I-12J
TB2-6	DET 3	I-2E	TB5-6	DET 29	J-5E	TB8-6	12 COM	I-12K
TB2-7		I-2J	TB5-7		J-5J	TB8-7	PED Ø6	I-13D
TB2-8	DET 4	I-2K	TB5-8	DET 30	J-5K	TB8-8	PED Ø8	I-13J
TB2-9		I-3D	TB5-9		J-6D	TB8-9	13 COM	I-13K
TB2-10	DET 5	I-3E	TB5-10	DET 31	J-6E	TB8-10	FLH SENSE	I-14D
TB2-11		I-3J	TB5-11		J-6J	TB8-11	STOP TIME	I-14J
TB2-12	DET 6	I-3K	TB5-12	DET 32	J-6K	TB8-12	14 COM	I-14K
TB3-1		J-1D	TB6-1	DET 13	I-7D	TB9-1	SPARE 2	J-11D
TB3-2	DET 19	J-1E	TB6-2		I-7E	TB9-2	SPARE 3	J-11J
TB3-3		J-1J	TB6-3	DET 14	I-7J	TB9-3	11 COM	J-11K
TB3-4	DET 20	J-1K	TB6-4		I-7K	TB9-4	EVA	J-12D
TB3-5		J-2D	TB6-5	DET 15	I-8D	TB9-5	EVC	J-12J
TB3-6	DET 21	J-2E	TB6-6		I-8E	TB9-6	12 COM	J-12K
TB3-7		J-2J	TB6-7	DET 16	I-8J	TB9-7	EVB	J-13D
TB3-8	DET 22	J-2K	TB6-8		I-8K	TB9-8	EVD	J-13J
TB3-9		J-3D	TB6-9		I-9D	TB9-9	13 COM	J-13K
TB3-10	DET 23	J-3E	TB6-10	DET 17	I-9E	TB9-10	RR1	J-14D
TB3-11		J-3J	TB6-11	DET 18	I-9J	TB9-11	RR2	J-14J
TB3-12	DET 24	J-3K	TB6-12		I-9K	TB9-12	14 COM	J-14K

INPUT PANEL #4
TERMINAL BLOCK ASSIGNMENT DETAIL

TERM	A	B
TB1-1	+24 VDC	OF IF M
TB1-2	M RESET	NA
TB1-3	RESERVED	RESERVED (COMM IN)
TB1-4	RESERVED	RESERVED (COMM IN)
TB1-5	RESERVED	RESERVED (COMM OUT)
TB1-6	RESERVED	RESERVED (COMM OUT)
TB2-1 TO 6	NA	NA

SERVICE PANELS 1 & 2
TERMINAL BLOCK ASSIGNMENT DETAIL

TERM	A	B
TBS-1	AC+	TO PDA (without BBS) TO BBS-1 (with BBS)
TBS-2	AC-	AC- BUS
TBS-3	NA	TO EQ.GND BUS
BBS-1	AC+ IN	MBPS AC+ IN
BBS-2	MBPS AC+ OUT	TO PDA
TB0-1 TO 12	NA	NA
TB3-1 TO 6	NA	NA

(See Service Panel Assembly (SPA) details A6-10 & A6-11)

NOTES:

- Sheet definitions:
 - 11 COM = DC COMMON
 - COMM = COMMUNICATION
 - DET1 = DETECTOR #1
 - EVA = EMERGENCY VEHICLE PREEMPTION A
 - IFI-1D = INPUT FILE 1, SLOT 1, CONNECTOR PIN D
 - OF = OUTPUT FILE
 - M = MONITOR MODULE
 - NA = NOT ASSIGNED
 - RR1 = RAILROAD PREEMPTION 1
 - MBPS = MANUAL BYPASS SWITCH
 - BBS = BATTERY BACK-UP SYSTEM
 - PDA = POWER DISTRIBUTION ASSEMBLY
- All dimensions shown are in inches.

INPUT PANEL #3
TERMINAL BLOCK (TB #1) ASSIGNMENT DETAIL

POS	A	B
TB1-1	+24 VDC	I/O FILES
TB1-2	+24 VDC	CAB. HARNESS #5
TB1-3	DC GND	C1 PINS 1 & 104
TB1-4	DC GND	I/O FILES & CAB. HARNESS #5
TB1-5	DC GND	
TB1-6	DC GND	
TB1-7	DC GND	
TB1-8	SPARE	NA
TB1-9	SPARE	NA
TB1-10	SPARE	NA
TB1-11	SPARE	NA
TB1-12	CURR. MONITOR 1	CAB. HARNESS #5
TB1-13	CURR. MONITOR 1	CAB. HARNESS #5
TB1-14	CURR. MONITOR 2	CAB. HARNESS #5
TB1-15	CURR. MONITOR 2	CAB. HARNESS #5
TB1-16	CURR. MONITOR 3	CAB. HARNESS #5
TB1-17	CURR. MONITOR 3	CAB. HARNESS #5
TB1-18	CURR. MONITOR 4	CAB. HARNESS #5
TB1-19	CURR. MONITOR 4	CAB. HARNESS #5
TB1-20	CURR. SEN. MON.	CAB. HARNESS #5
TB1-21	CURR. SEN. MON.	CAB. HARNESS #5
TB1-22	C1 PIN 10	CIA CONTROL 4
TB1-23	C1 PIN 18	NA
TB1-24	C1 PIN 63	NA
TB1-25	C1 PIN 64	NA
TB1-26	C1 PIN 65	POL. CONTROL SW.
TB1-27	C1 PIN 66	POL. LIGHTS SW.
TB1-28	C1 PIN 77	NA
TB1-29	SPARE	CAB. HARNESS #5
TB1-30	SPARE	CAB. HARNESS #5

INPUT PANEL #3
TERMINAL BLOCK (TB #2) ASSIGNMENT DETAIL

POS	A	B	POS	A	B
TB2-1	I-1D		TB2-36	EQ. GND	
TB2-2	I-1E		TB2-39	I-8J	
TB2-3	EQ. GND		TB2-40	I-8K	
TB2-4	I-1J		TB2-41	I-9D	
TB2-5	I-1K		TB2-42	I-9E	
TB2-6	I-2D		TB2-43	EQ. GND	
TB2-7	I-2E		TB2-44	I-9J	
TB2-8	EQ. GND		TB2-45	I-9K	
TB2-9	I-2J		TB2-46	I-10D	
TB2-10	I-2K		TB2-47	I-10E	
TB2-11	I-3D		TB2-48	EQ. GND	
TB2-12	I-3E		TB2-49	I-10J	
TB2-13	EQ. GND		TB2-50	I-10K	
TB2-14	I-3J		TB2-51	I-11D	
TB2-15	I-3K		TB2-52	I-11E	
TB2-16	I-4D		TB2-53	EQ. GND	
TB2-17	I-4E		TB2-54	I-11J	
TB2-18	EQ. GND		TB2-55	I-11K	
TB2-19	I-4J		TB2-56	I-12D	
TB2-20	I-4K		TB2-57	I-12E	
TB2-21	I-5D		TB2-58	EQ. GND	
TB2-22	I-5E		TB2-59	I-12J	
TB2-23	EQ. GND		TB2-60	I-12K	
TB2-24	I-5J		TB2-61	I-13D	
TB2-25	I-5K		TB2-62	I-13E	
TB2-26	I-6D		TB2-63	EQ. GND	
TB2-27	I-6E		TB2-64	I-13J	
TB2-28	EQ. GND		TB2-65	I-13K	
TB2-29	I-6J		TB2-66	I-14D	
TB2-30	I-6K		TB2-67	I-14E	
TB2-31	I-7D		TB2-68	EQ. GND	
TB2-32	I-7E		TB2-69	I-14J	
TB2-33	EQ. GND		TB2-70	I-14K	
TB2-34	I-7J		TB2-71	SPARE	
TB1-35	I-7K		TB1-72	SPARE	
TB1-36	I-8D		TB1-73	EQ. GND	
TB2-37	I-8E				

TITLE:

SIDE PANEL DETAILS
SHEET 4 OF 4

NO SCALE

TEES 2009

A6-24

C1 HARNESS #1 WIRING LIST

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC GND	DC GND BUS	-	53	I2-7	IFI-11W	SPARE #1
2	O1-1	C4-1	SWPK 4P-RED	54	I2-8	IFJ-11W	SPARE #2
3	O1-2	C4-2	SWPK 4P-GRN	55	I3-1	IFJ-1F&W	5 CE
4	O1-3	C4-3	SWPK 4-RED	56	I3-2	IFI-1F&W	1 CE
5	O1-4	C4-4	SWPK 4-YEL	57	I3-3	IFJ-5F&W	7 CE
6	O1-5	C4-5	SWPK 4-GRN	58	I3-4	IFI-5F&W	3 CE
7	O1-6	C4-6	SWPK 3-RED	59	I3-5	IFJ-9F	5 CE
8	O1-7	C4-7	SWPK 3-YEL	60	I3-6	IFI-9F	1 CE
9	O1-8	C4-8	SWPK 3-GRN	61	I3-7	IFJ-9W	7 CE
10	O2-1	C4-9	SWPK 2P-RED	62	I3-8	IFI-9W	3 CE
11	O2-2	C4-10	SWPK 2P-GRN	63	I4-5	IFI-3F	2 CE
12	O2-3	C4-11	SWPK 2-RED	64	I4-6	IFJ-3F	6 CE
13	O2-4	C4-12	SWPK 2-YEL	65	I4-7	IFI-7F	4 CE
14	DC GND	IFI-15-4	INPUT DC GND	66	I4-8	IFJ-7F	8 CE
15	O2-5	C4-13	SWPK 2-GRN	67	I5-1	IFI-12F	2 PED
16	O2-6	C4-14	SWPK 1-RED	68	I5-2	IFI-13F	6 PED
17	O2-7	C4-15	SWPK 1-YEL	69	I5-3	IFI-12W	4 PED
18	O2-8	C4-16	SWPK 1-GRN	70	I5-4	IFI-13W	8 PED
19	O3-1	C4-17	SWPK 8P-RED	71	I5-5	IFJ-12F	EVA PREEMPT
20	O3-2	C4-18	SWPK 8P-GRN	72	I5-6	IFJ-13F	EVB PREEMPT
21	O3-3	C4-19	SWPK 8-RED	73	I5-7	IFJ-12W	EVC PREEMPT
22	O3-4	C4-20	SWPK 8-YEL	74	I5-8	IFJ-13W	EVD PREEMPT
23	O3-5	C4-21	SWPK 8-GRN	75	I6-1	IFJ-11W	SPARE #3
24	O3-6	C4-22	SWPK 7-RED	76	I6-2	IFI-3W	2 CE
25	O3-7	C4-23	SWPK 7-YEL	77	I6-3	IFJ-3W	6 CE
26	O3-8	C4-24	SWPK 7-GRN	78	I6-4	IFI-7W	4 CE
27	O4-1	C4-25	SWPK 6P-RED	79	I6-5	IFJ-7W	8 CE
28	O4-2	C4-26	SWPK 6P-GRN	80	I6-6	IFI-11F	ADVANCE
29	O4-3	C4-27	SWPK 6-RED	81	I6-7	IFI-14F	FLASH SENSE
30	O4-4	C4-28	SWPK 6-YEL	82	I6-8	IFI-14W	STOP TIME
31	O4-5	C4-29	SWPK 6-GRN	83	O6-1	C5-1	SWPK 14-RED
32	O4-6	C4-30	SWPK 5-RED	84	O6-2	C5-2	SWPK 14-GRN
33	O4-7	C4-31	SWPK 5-YEL	85	O6-3	C5-3	SWPK 13-RED
34	O4-8	C4-32	SWPK 5-GRN	86	O6-4	C5-4	SWPK 13-YEL
35	O5-1	C4-33	SWPK 2P-YEL	87	O6-5	C5-5	SWPK 13-GRN
36	O5-2	C4-34	SWPK 6P-YEL	88	O6-6	C5-6	SWPK 12-RED
37	O5-3	C4-35	SWPK 4P-YEL	89	O6-7	C5-7	SWPK 12-YEL
38	O5-4	C4-36	SWPK 8P-YEL	90	O6-8	C5-8	SWPK 12-GRN
39	I1-1	IFI-2F	2 CE	91	O7-1	C5-9	SWPK 11-RED
40	I1-2	IFJ-2F	6 CE	92	DC GND	DC GND BUS	-
41	I1-3	IFI-6F	4 CE	93	O7-2	C5-10	SWPK 11-GRN
42	I1-4	IFJ-6F	8 CE	94	O7-3	C5-11	SWPK 10-RED
43	I1-5	IFI-2W	2 CE	95	O7-4	C5-12	SWPK 10-YEL
44	I1-6	IFJ-2W	6 CE	96	O7-5	C5-13	SWPK 10-GRN
45	I1-7	IFI-6W	4 CE	97	O7-6	C5-14	SWPK 9-RED
46	I1-8	IFJ-6W	8 CE	98	O7-7	C5-15	SWPK 9-YEL
47	I2-1	IFI-4F&W	2 CALL	99	O7-8	C5-16	SWPK 9-GRN
48	I2-2	IFJ-4F&W	6 CALL	100	O5-5	C5-17	SWPK 14-YEL
49	I2-3	IFI-8F&W	4 CALL	101	O5-6	C5-18	SWPK 11-YEL
50	I2-4	IFJ-8F&W	8 CALL	102	O5-7	IFI&J-15-3	DETECTOR RESET
51	I2-5	IFJ-14F	RR1 PREEMPT	103	O5-8	C4-37	WDT-MU
52	I2-6	IFJ-14W	RR2 PREEMPT	104	DC GND	IFJ-15-4	INPUT DC GND

TITLE:

HARNESS WIRING DETAILS
SHEET 1 OF 5

NO SCALE

TEES 2009

A6-25

C1 HARNESS #2 WIRING LIST

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC GND	TB1/3-7	DC GND BUS	53	I2-7	IFI-11F	RATE CODE 2
2	O1-1	C6-1	SWPK 1-RED	54	I2-8	IFI-11W	RATE CODE 1
3	O1-2	C6-2	SWPK 1-GRN	55	I3-1	IFI-4F	MAIN 9
4	O1-3	C6-3	SWPK 2-RED	56	I3-2	IFI-4W	MAIN 10
5	O1-4	C6-4	SWPK 2-YEL	57	I3-3	IFI-6F	MAIN 3
6	O1-5	C6-5	SWPK 2-GRN	58	I3-4	IFI-6W	MAIN 4
7	O1-6	C6-6	SWPK 3-RED	59	I3-5	IFI-7F	MAIN 5
8	O1-7	C6-7	SWPK 3-YEL	60	I3-6	IFI-7W	MAIN 6
9	O1-8	C6-8	SWPK 3-GRN	61	I3-7	IFI-8F	MAIN 11
10	O2-1	TB1/22	CIA CONTROL 4	62	I3-8	IFI-8W	MAIN 12
11	O2-2	C7-25	CMS CLOCK	63	I4-5	TB1/24	MAIN 17
12	O2-3	C7-26	CMS ENABLE	64	I4-6	TB1/25	MAIN 18
13	O2-4	C7-27	CMS CLEAR	65	I4-7	TB1/26	POL. CONTR'L SW.
14	DC GND	IFI-15-4	INPUT DC GND	66	I4-8	TB1/27	POL. LIGHTS SW.
15	O2-5	C7-28	CMS DIM LEVEL 1	67	I5-1	C7-16	CIA SENSE 1
16	O2-6	C7-29	CMS DIM LEVEL 2	68	I5-2	C7-31	CIA SENSE 2
17	O2-7	C7-30	CMS DIM LEVEL 3	69	I5-3	C7-32	CIA SENSE 3
18	O2-8	TB1/23	-	70	I5-4	C7-33	CIA SENSE 4
19	O3-1	C7-9	CMS ADDRESS 1	71	I5-5	C7-34	CIA SENSE 5
20	O3-2	C7-10	CMS ADDRESS 2	72	I5-6	C7-35	CIA SENSE 6
21	O3-3	C7-11	CMS ADDRESS 3	73	I5-7	C7-36	CIA SENSE 7
22	O3-4	C7-12	CMS ADDRESS 4	74	I5-8	C7-37	CIA SENSE 8
23	O3-5	C7-13	CMS ADDRESS 5	75	I6-1	C7-5	CMS LATCH
24	O3-6	C7-14	CMS ADDRESS 6	76	I6-2	C7-6	PHASE FIRE
25	O3-7	C7-15	CMS ADDRESS 7	77	I6-3	TB1/29	MAIN 19
26	O3-8	C7-4	CIA CONTROL 5	78	I6-4	C7-8	CMS TEST REQ.
27	O4-1	C7-17	CMS DATA 1	79	I6-5	IFI-10F	MAIN 15
28	O4-2	C7-18	CMS DATA 2	80	I6-6	IFI-9W	MAIN 14
29	O4-3	C7-19	CMS DATA 3	81	I6-7	IFI-9F	MAIN 13
30	O4-4	C7-20	CMS DATA 4	82	I6-8	IFI-10W	MAIN 16
31	O4-5	C7-21	CMS DATA 5	83	O6-1	C5-1	SWPK 14-RED
32	O4-6	C7-22	CMS DATA 6	84	O6-2	C5-2	SWPK 14-GRN
33	O4-7	C7-23	CMS DATA 7	85	O6-3	C5-3	SWPK 13-RED
34	O4-8	C7-24	CMS DATA 8	86	O6-4	C5-4	SWPK 13-YEL
35	O5-1	C7-1	CIA CONTROL 1	87	O6-5	C5-5	SWPK 13-GRN
36	O5-2	C7-2	CIA CONTROL 2	88	O6-6	C5-6	SWPK 12-RED
37	O5-3	C6-9	SWPK 1-YEL	89	O6-7	C5-7	SWPK 12-YEL
38	O5-4	C7-3	CIA CONTROL 3	90	O6-8	C5-8	SWPK 12-GRN
39	I1-1	IFI-1W	PASSAGE 1	91	O7-1	C5-9	SWPK 11-RED
40	I1-2	IFI-12W	PASSAGE 2	92	DC GND	TB1/3-7	-
41	I1-3	IFI-12F	DEMAND 2	93	O7-2	C5-10	SWPK 11-GRN
42	I1-4	IFI-13W	OFF RAMP 2	94	O7-3	C5-11	SWPK 10-RED
43	I1-5	IFI-13F	QUE 2	95	O7-4	C5-12	SWPK 10-YEL
44	I1-6	IFI-14W	PASSAGE 3	96	O7-5	C5-13	SWPK 10-GRN
45	I1-7	IFI-14F	DEMAND 3	97	O7-6	C5-14	SWPK 9-RED
46	I1-8	IFI-1F	DEMAND 1	98	O7-7	C5-15	SWPK 9-YEL
47	I2-1	IFI-2W	OFF RAMP 1	99	O7-8	C5-16	SWPK 9-GRN
48	I2-2	IFI-3W	MAIN 7	100	O5-5	C5-17	SWPK 14-YEL
49	I2-3	IFI-3F	MAIN 8	101	O5-6	C5-18	SWPK 11-YEL
50	I2-4	IFI-2F	QUE 1	102	O5-7	IFI-15-3	DETECTOR RESET
51	I2-5	IFI-5F	MAIN 1	103	O5-8	C6-10	WDT
52	I2-6	IFI-5W	MAIN 2	104	DC GND	TB1/3-7	DC GND BUS

TITLE:		HARNESS WIRING DETAILS SHEET 2 OF 5
NO SCALE	A6-26	
TEES 2009		

C1 HARNESS #3 WIRING LIST

PIN	SOURCE	DESTINATION	FUNCTION	PIN	SOURCE	DESTINATION	FUNCTION
1	DC GND	DC GND BUS		53	I2-7	TB2-5	SPARE #1
2	O1-1	C4-1	SWPK 4P-RED	54	I2-8	TB2-6	SPARE #2
3	O1-2	C4-2	SWPK 4P-GRN	55	I3-1	IFI-5F	5 CE
4	O1-3	C4-3	SWPK 4-RED	56	I3-2	IFI-1F	1 CE
5	O1-4	C4-4	SWPK 4-YEL	57	I3-3	IFI-7F	7 CE
6	O1-5	C4-5	SWPK 4-GRN	58	I3-4	IFI-3F	3 CE
7	O1-6	C4-6	SWPK 3-RED	59	I3-5	IFI-1SP	-
8	O1-7	C4-7	SWPK 3-YEL	60	I3-6	IFI-2SP	-
9	O1-8	C4-8	SWPK 3-GRN	61	I3-7	IFI-3SP	-
10	O2-1	C4-9	SWPK 2P-RED	62	I3-8	IFI-4SP	-
11	O2-2	C4-10	SWPK 2P-GRN	63	I4-5	IFI-5SP	-
12	O2-3	C4-11	SWPK 2-RED	64	I4-6	IFI-6SP	-
13	O2-4	C4-12	SWPK 2-YEL	65	I4-7	IFI-7SP	-
14	DC GND	IFI-15-4	INPUT DC GND	66	I4-8	IFI-8SP	-
15	O2-5	C4-13	SWPK 2-GRN	67	I5-1	IFI-12F	2 PED
16	O2-6	C4-14	SWPK 1-RED	68	I5-2	IFI-13F	6 PED
17	O2-7	C4-15	SWPK 1-YEL	69	I5-3	IFI-12W	4 PED
18	O2-8	C4-16	SWPK 1-GRN	70	I5-4	IFI-13W	8 PED
19	O3-1	C4-17	SWPK 8P-RED	71	I5-5	IFI-10F	EVA PREEMPT
20	O3-2	C4-18	SWPK 8P-GRN	72	I5-6	IFI-11F	EVB PREEMPT
21	O3-3	C4-19	SWPK 8-RED	73	I5-7	IFI-10W	EVC PREEMPT
22	O3-4	C4-20	SWPK 8-YEL	74	I5-8	IFI-11W	EVD PREEMPT
23	O3-5	C4-21	SWPK 8-GRN	75	I6-1	IFI-9SP	SPARE #3
24	O3-6	C4-22	SWPK 7-RED	76	I6-2	IFI-10SP	2 CE
25	O3-7	C4-23	SWPK 7-YEL	77	I6-3	IFI-11SP	6 CE
26	O3-8	C4-24	SWPK 7-GRN	78	I6-4	IFI-12SP	4 CE
27	O4-1	C4-25	SWPK 6P-RED	79	I6-5	IFI-13SP	8 CE
28	O4-2	C4-26	SWPK 6P-GRN	80	I6-6	IFI-14SP	ADVANCE
29	O4-3	C4-27	SWPK 6-RED	81	I6-7	IFI-14F	FLASH SENSE
30	O4-4	C4-28	SWPK 6-YEL	82	I6-8	IFI-14W	STOP TIME
31	O4-5	C4-29	SWPK 6-GRN	83	O6-1	NA	-
32	O4-6	C4-30	SWPK 5-RED	84	O6-2	NA	-
33	O4-7	C4-31	SWPK 5-YEL	85	O6-3	NA	-
34	O4-8	C4-32	SWPK 5-GRN	86	O6-4	NA	-
35	O5-1	C4-33	SWPK 2P-YEL	87	O6-5	NA	-
36	O5-2	C4-34	SWPK 6P-YEL	88	O6-6	NA	-
37	O5-3	C4-35	SWPK 4P-YEL	89	O6-7	NA	-
38	O5-4	C4-36	SWPK 8P-YEL	90	O6-8	NA	-
39	I1-1	IFI-2F	2 CE	91	O7-1	NA	-
40	I1-2	IFI-6F	6 CE	92	DC GND	DC GND BUS	-
41	I1-3	IFI-4F	4 CE	93	O7-2	NA	-
42	I1-4	IFI-8F	8 CE	94	O7-3	NA	-
43	I1-5	IFI-2W	2 CE	95	O7-4	NA	-
44	I1-6	IFI-6W	6 CE	96	O7-5	NA	-
45	I1-7	IFI-4W	4 CE	97	O7-6	NA	-
46	I1-8	IFI-8W	8 CE	98	O7-7	NA	-
47	I2-1	IFI-1W	2 CALL	99	O7-8	NA	-
48	I2-2	IFI-5W	6 CALL	100	O5-5	NA	-
49	I2-3	IFI-3W	4 CALL	101	O5-6	NA	-
50	I2-4	IFI-7W	8 CALL	102	O5-7	IFI-15-3	DETECTOR RESET
51	I2-5	IFI-9F	RR1 PREEMPT	103	O5-8	C4-37	WDT-MU
52	I2-6	IFI-9W	RR2 PREEMPT	104	DC GND	IFJ-15-4	-

TITLE:

HARNESS WIRING DETAILS
SHEET 3 OF 5

NO SCALE

TEES 2009

A6-27

C4 HARNESS #1 AND #3 WIRING LIST

PIN	SOURCE	DESTINATION
1	C1-2	SWPK 4P-RED
2	C1-3	SWPK 4P-GRN
3	C1-4	SWPK 4-RED
4	C1-5	SWPK 4-YEL
5	C1-6	SWPK 4-GRN
6	C1-7	SWPK 3-RED
7	C1-8	SWPK 3-YEL
8	C1-9	SWPK 3-GRN
9	C1-10	SWPK 2P-RED
10	C1-11	SWPK 2P-GRN
11	C1-12	SWPK 2-RED
12	C1-13	SWPK 2-YEL
13	C1-15	SWPK 2-GRN
14	C1-16	SWPK 1-RED
15	C1-17	SWPK 1-YEL
16	C1-18	SWPK 1-GRN
17	C1-19	SWPK 8P-RED
18	C1-20	SWPK 8P-GRN
19	C1-21	SWPK 8-YEL
20	C1-22	SWPK 8-YEL
21	C1-23	SWPK 8-GRN
22	C1-24	SWPK 7-RED
23	C1-25	SWPK 7-YEL
24	C1-26	SWPK 7-GRN
25	C1-27	SWPK 6P-RED
26	C1-28	SWPK 6P-GRN
27	C1-29	SWPK 6-RED
28	C1-30	SWPK 6-YEL
29	C1-31	SWPK 6-GRN
30	C1-32	SWPK 5-RED
31	C1-33	SWPK 5-YEL
32	C1-34	SWPK 5-GRN
33	C1-35	SWPK 2P-YEL
34	C1-36	SWPK 6P-YEL
35	C1-37	SWPK 4P-YEL
36	C1-38	SWPK 8P-YEL
37	C1-103	SWPK WDT-MU

C5 HARNESS #1 AND #2 WIRING LIST

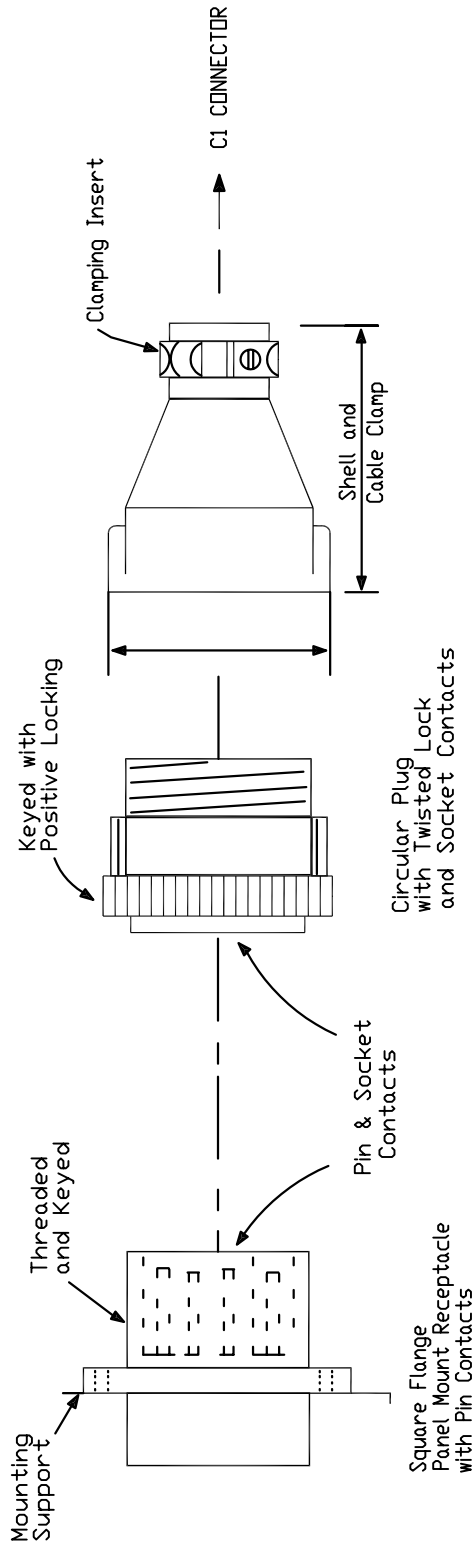
PIN	SOURCE	DESTINATION
1	C1-83	SWPK 14-RED
2	C1-84	SWPK 14-GRN
3	C1-85	SWPK 13-RED
4	C1-86	SWPK 13-YEL
5	C1-87	SWPK 13-GRN
6	C1-77	SWPK 12-RED
7	C1-89	SWPK 12-YEL
8	C1-90	SWPK 12-GRN
9	C1-91	SWPK 11-RED
10	C1-93	SWPK 11-GRN
11	C1-94	SWPK 10-RED
12	C1-95	SWPK 10-YEL
13	C1-96	SWPK 10-GRN
14	C1-97	SWPK 9-RED
15	C1-98	SWPK 9-YEL
16	C1-99	SWPK 9-GRN
17	C1-100	SWPK 14-YEL
18	C1-101	SWPK 11-YEL
19	NA	NA
20	NA	NA
21	NA	NA
22	NA	NA
23	NA	NA
24	+24 VDC	PIN 9, ALL SOCKETS

C6 HARNESS #2 WIRING LIST

PIN	SOURCE	DESTINATION
1	C1-2	SWPK 1-RED
2	C1-3	SWPK 1-GRN
3	C1-4	SWPK 2-RED
4	C1-5	SWPK 2-YEL
5	C1-6	SWPK 2-GRN
6	C1-7	SWPK 3-RED
7	C1-8	SWPK 3-YEL
8	C1-9	SWPK 3-GRN
9	C1-37	SWPK 1-YEL
10	C1-103	WDT
11	NA	NA
12	NA	NA
13	NA	NA
14	NA	NA
15	NA	NA
16	NA	NA
17	NA	NA
18	NA	NA
19	NA	NA
20	NA	NA
21	NA	NA
22	NA	NA
23	NA	NA
24	+24 VDC	PIN 9, ALL SOCKETS

TITLE:		HARNESS WIRING DETAILS SHEET 4 OF 5
NO SCALE		A6-28
TEES 2009		

CONNECTORS C4, C5 AND C6



NOTE: (FOR DETAILS A6-25 to A6-29)

1. Sheet definitions:

C1-2	= CONNECTOR C1, PIN 2
EVA	= EMERGENCY VEHICLE A
I1-1	= INPUT PORT 5001, BIT 1
IF1-2F, SP	= INPUT FILE 1, TERMINAL BLOCK 2, TERMINAL DESIGNATION F (CHANNEL 1 OUTPUT), SPARE
IFJ-6W	= INPUT FILE J, TERMINAL BLOCK 6, TERMINAL DESIGNATION W (CHANNEL 2 OUTPUT)
O1-1	= OUTPUT PORT 5001, BIT 1
TB1/26	= TERMINAL BLOCK 1 POSITION 26
RR1	= RAILROAD 1
SWPK 2P-GRN	= SWITCHPACK 2 PEDESTRIAN, GREEN
WDT-MU	= WATCHDOG TIMER, MONITOR UNIT
2 CE	= PHASE 2 COUNT & EXTENSION

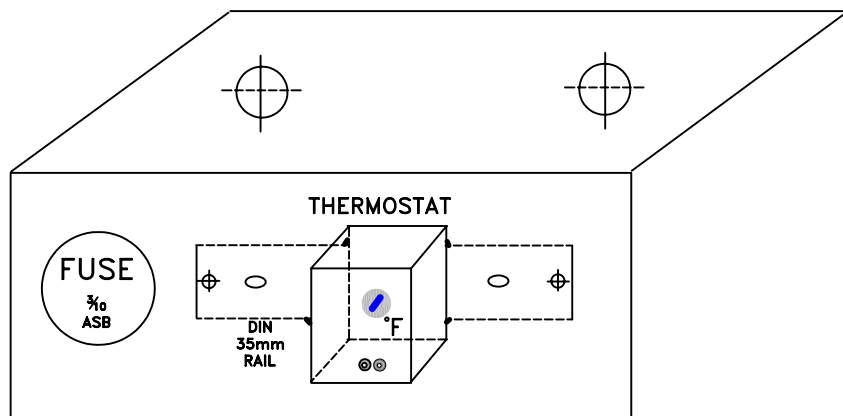
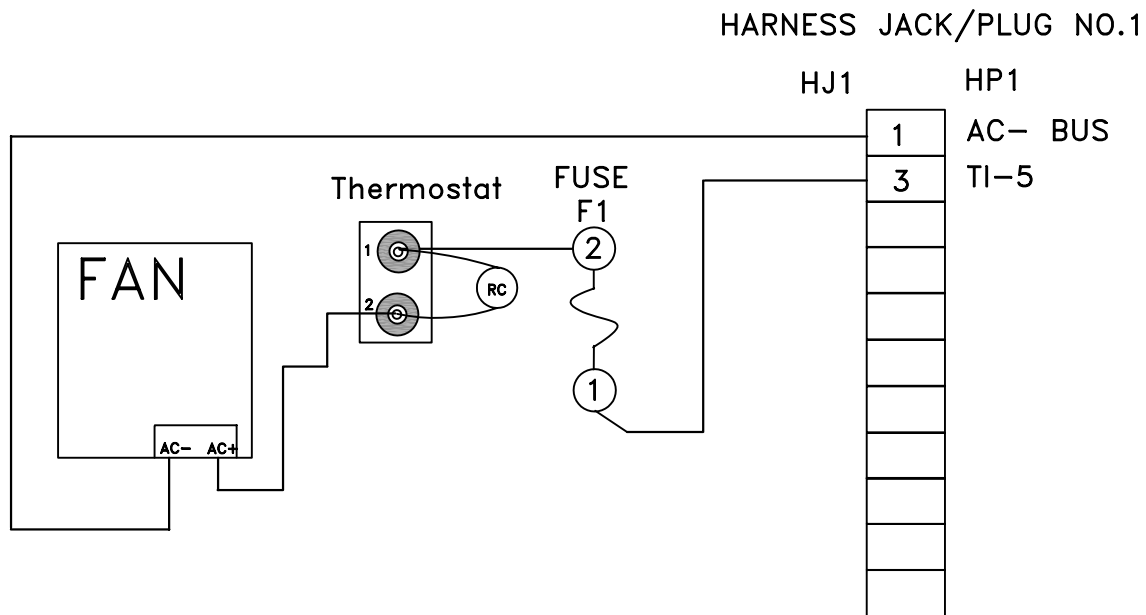
TITLE:

HARNESS WIRING DETAILS
SHEET 5 OF 5

NO SCALE

TEES 2009

A6-29



THERMOSTAT MOUNTING DETAILS

TITLE:

FAN AND THERMOSTAT DETAILS

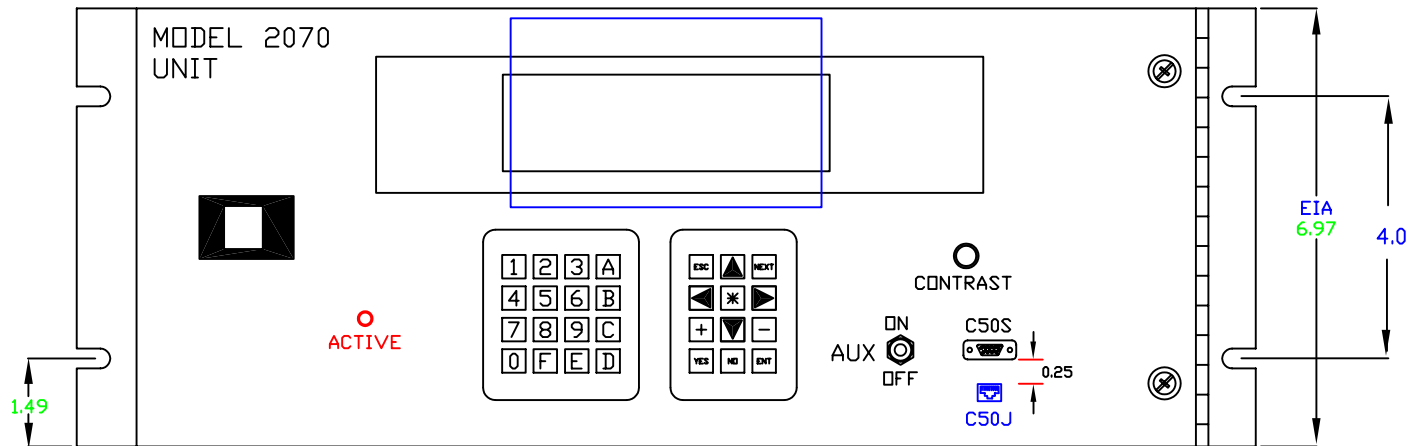
NO SCALE

TEES 2009

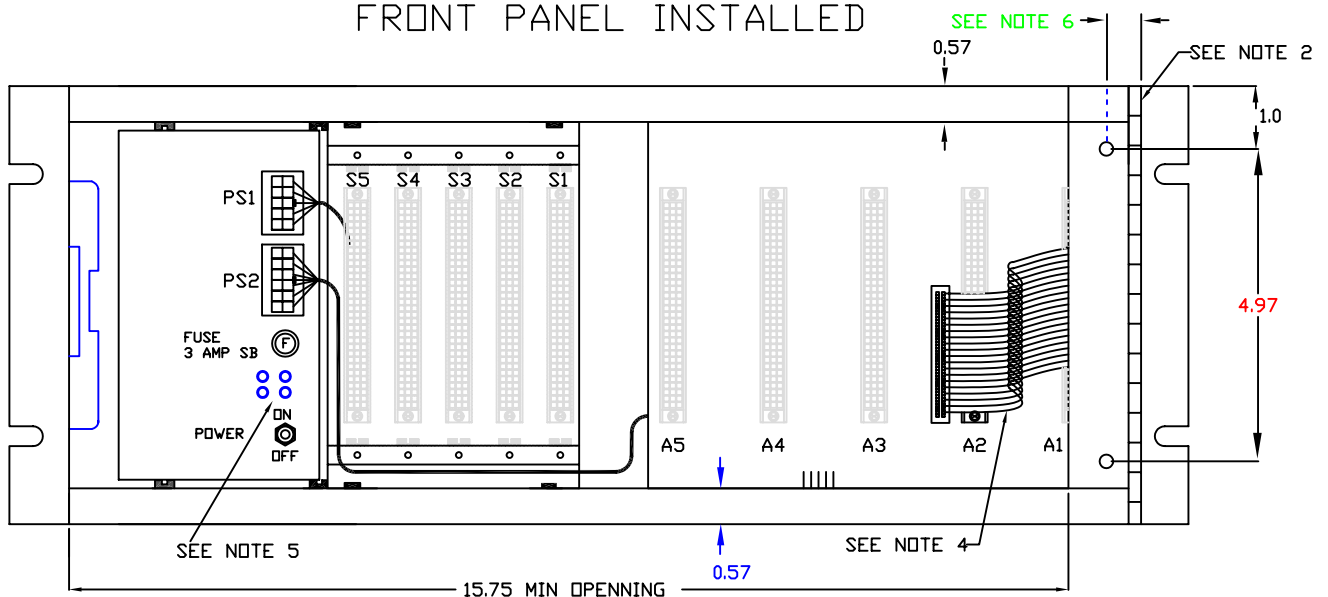
A6-30

**APPENDIX A9
CHAPTER 9 DETAILS**

Model 2070 - Chassis Front View	A9-1
Model 2070 - Chassis Rear View	A9-2
Model 2070 - Chassis Top View	A9-3
Model 2070 - Chassis Motherboard	A9-4
Model 2070 - Motherboard A1-A5 Connector Pinouts	A9-5
Model 2070 - System PCB Modules, General	A9-6
Model 2070 – 1E CPU Modules & Serial Port / SDLC Protocol	A9-7
Model 2070 – 2, Field I/O Module	A9-8
Model 2070 – 2A Field I/O Module, C1 & C11 Connectors	A9-9
Model 2070 – 3A, 3B & 3D Front Panel Assembly	A9-10
Model 2070 – 3 Front Panel Assembly, Key Codes	A9-11
Model 2070 – 3 Front Panel Assembly, Display Key Codes	A9-12
Model 2070 – 4 Power Supply Module	A9-13
Model 2070 – 5 VME Cage Assembly	A9-14
Model 2070 – 1C CPU Module	A9-15
Model 2070 – Serial Port Descriptors Defaults	A9-16
Model 2070 – Power Failure Reaction	A9-17



FRONT PANEL INSTALLED

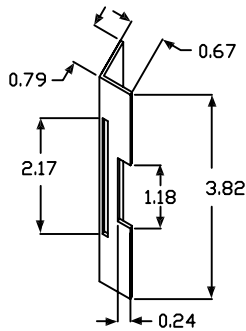
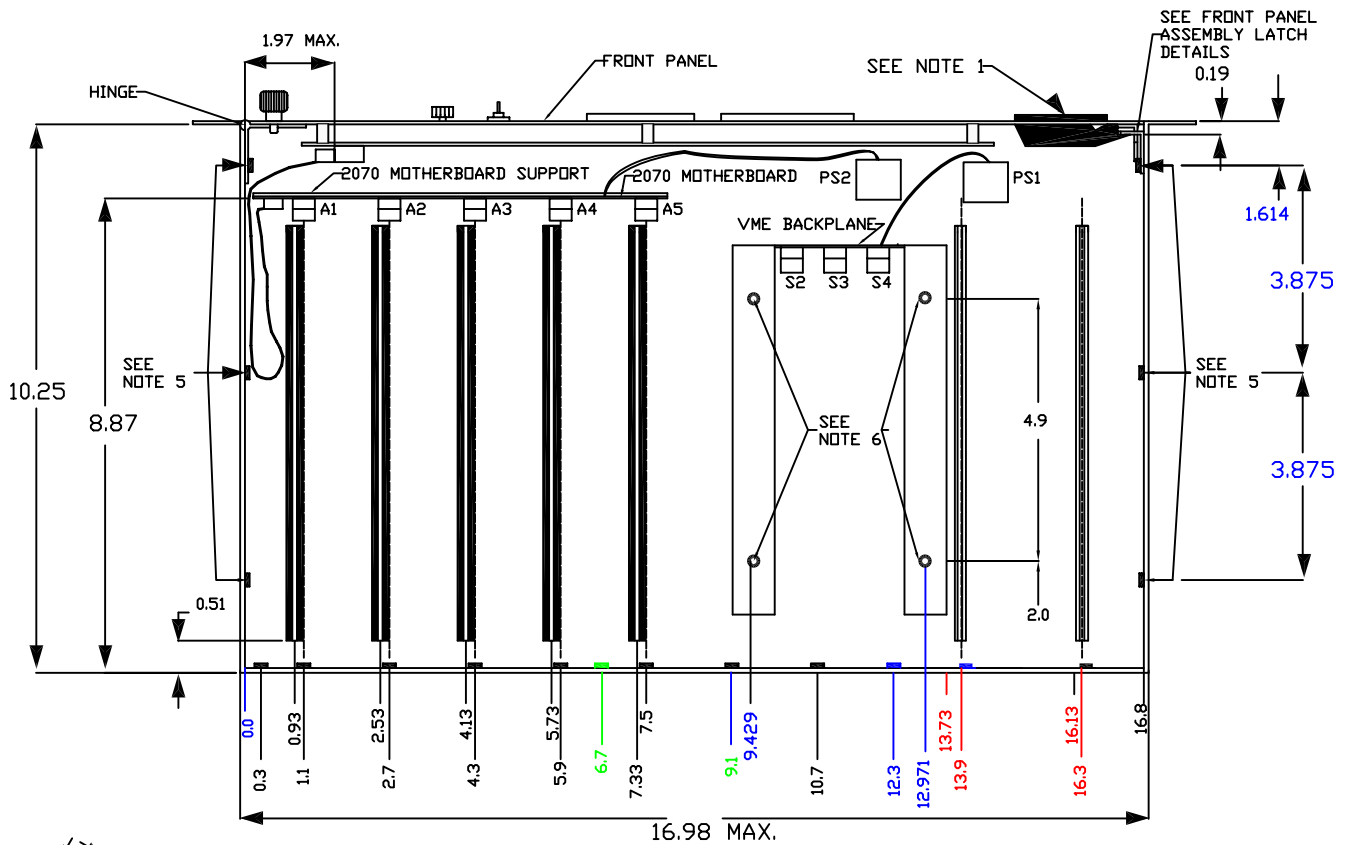


FRONT PANEL REMOVED

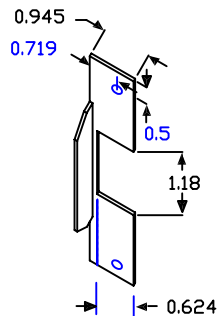
NOTES: (FOR THIS DETAIL)

1. The unit shall be capable of mounting to a Standard EIA-310B Rack using 4U open end mounting slots.
2. Continuous stainless steel hinge (0.157in maximum hinge barrel) that attaches to the Front Panel by two TSD #1 Thumbscrew devices.
3. Actual location of ACTIVE light, AUX switch, C50S, C50J and contrast control shall be limited to ACTIVE light on the left side of the panel; AUX switch, C50S, C50J and the contrast control on the right side. They shall be located greater than 1 in from the edge of each other, other devices, connector or latch. C50J only needs to be 0.25in minimum from C50S.
4. The length of the Front Panel Harness shall be 5in + 2% and it shall be removeable.
5. LED indicators for each DC voltage shall be provided.
6. With the hinge installed, the distance between the TSD hole center and the CHASSIS Right Side (inside plane) shall be 0.55in.
7. All dimensions shown are in inches.

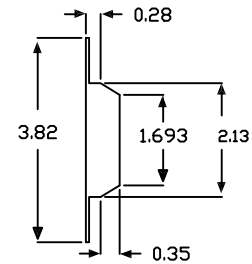
TITLE:		MODEL 2070-CHASSIS FRONT VIEW
NO SCALE		A9-1
TEES 2009		



CHASSIS BRACKET
(Thickness Is 0.06)



FRONT PANEL BRACKET



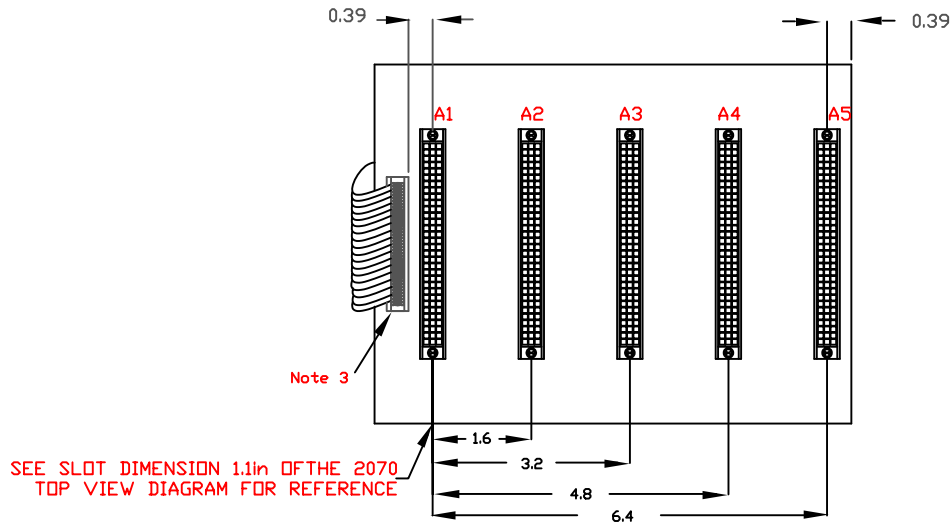
SIDE VIEW

FRONT PANEL ASSEMBLY LATCH DETAILS

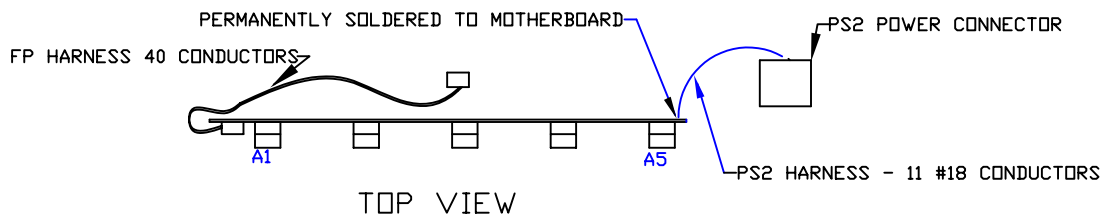
NOTES: (FOR THIS DETAIL)

1. Front Panel Assembly Latch mating with and rigidly held in place by Chassis Guide Latch/member shall be provided.
2. Nylon card guides, SAE 1800F (OR EQUAL), shall be provided (top and bottom) for Mother Slot/Connectors A1 to A5. The Guides shall begin 0.51 inch from the Backplane **outside** surface.
3. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes located on Backplane Surface.
4. All harnesses shall have a minimum slack of **1 inch** when connected.
5. M3 PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the TSD #3 Thumbscrew Devices on the Model 2070-8 Module. Fastener centers shall be 0.25 inch above unit baseline.
6. Eight 6-32 Phillips head counter-sunk screws, 4 top and 4 bottom, shall be used to mount the cage assembly to the 2070 Chassis.
7. The 2070 chassis top & bottom sections shall be constructed with a continuous 0.571 inch folded lip along the front perpendicular to the 2070 top and bottom sections. The top and bottom sections of the 2070 chassis shall be recessed **0.71 inch** as measured from the front surface of the front panel.
8. Chassis side plates shall be 0.090in thick.
9. All dimensions shown are in inches.

TITLE: MODEL 2070-CHASSIS TOP VIEW	
NO SCALE	A9-3
TEES 2009	



CONNECTOR VIEW



TOP VIEW

FP HARNESS PIN/WIRING ASSIGNMENT			
PIN	CONNECTOR ROW A	PIN	CONNECTOR ROW B
1	SP4TXD+	2	SP4TXD-
3	SP4RXD+	4	SP4RXD-
5	SP6TXD+	6	SP6TXD-
7	SP6RXD+	8	SP6RXD-
9	NA	10	NA
11	NA	12	NA
13	NA	14	NA
15	NA	16	NA
17	NA	18	NA
19	NA	20	NA
21	DCG #1	22	DCG #1
23	+12 VDC SER	24	-12 VDC SER
25	DCG #1	26	DCG #1
27	CPU LED	28	DCG #1
29	CPURESET	30	DCG #1
31	DCG #1	32	C50 ENABLE
33	DCG #1	34	+5 VDC
35	+5 VDC	36	+5 VDC
37	+5 VDC	38	+5 VDC
39	NA	40	NA

PS2 HARNESS PIN/WIRING ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISD +12 VDC
7	DCG #2 (ISD +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

NOTES: (FOR THIS DETAIL)

1. The Motherboard shall be a 0.125 inch minimum thickness pcb mechanically mounted in a vertical position.
2. A1 to A5 receptacle connectors shall be 96 socket contact DIN 41612 connectors (ROBINSON NUGENT #DIN 96RSC or ELCO Series 8477 Three Row Inverted Socket OR EQUAL).
3. The FP Harness shall be connected to the motherboard via a header connector. Pin 1 shall be in the lower right hand corner.
4. Front Panel Harness Connector shall intermate with AMP 102-160-9 or equal located on Front Panel PCB.
5. All dimensions shown are in inches.

TITLE: MODEL 2070 CHASSIS MOTHERBOARD	
NO SCALE	A9-4
TEES 2009	

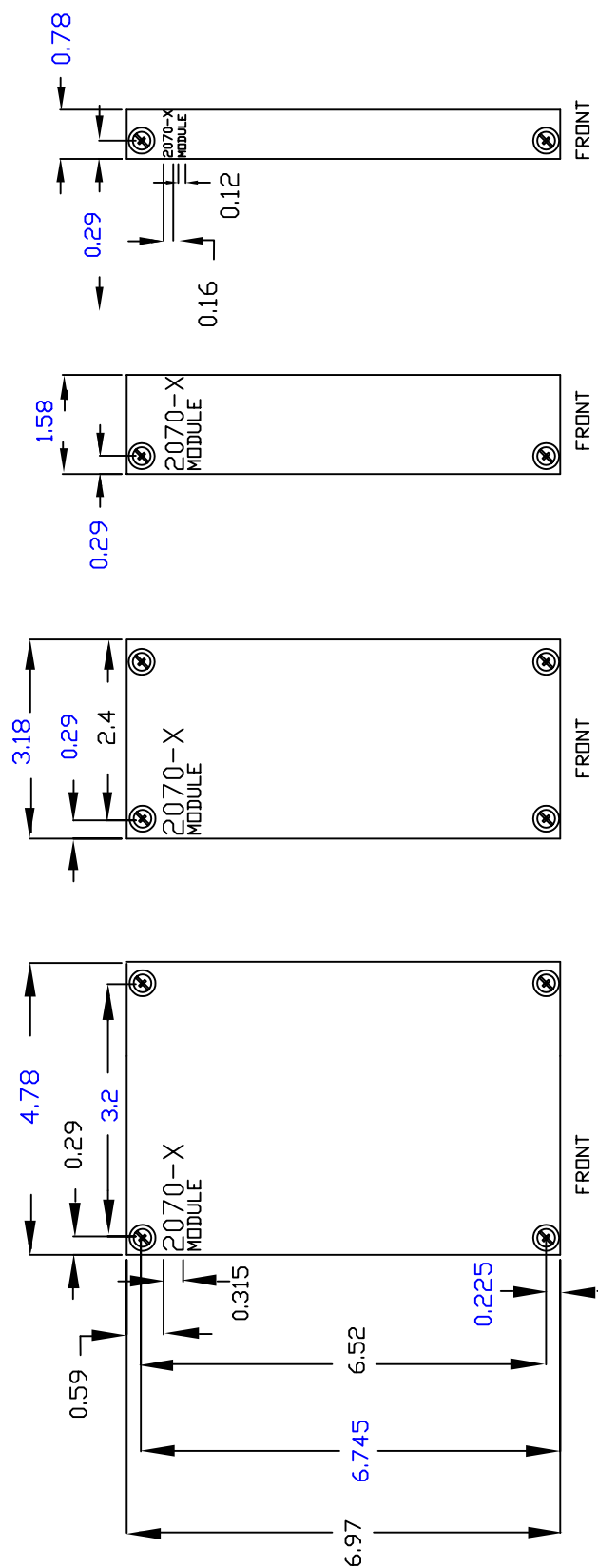
A1 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP3TXD+	SP6TXD+	SP5TXD+
2	SP3TXD-	SP6TXD-	SP5TXD-
3	SP3RXD+	SP6RXD+	SP5TXC+
4	SP3RXD-	SP6RXD-	SP5TXC-
5	SP3RTS+	SP3TXC0+	SP5RXD+
6	SP3RTS-	SP3TXC0-	SP5RXD-
7	SP3CTS+	SP3TXCI+	SP5RXC+
8	SP3CTS-	SP3TXCI-	SP5RXC-
9	SP3DCD+	SP3RXC+	SP3TXD+
10	SP3DCD-	SP3RXC-	SP3TXD-
11	SP4TXD+	SP4TXD+	SP3RXD+
12	SP4TXD-	SP4TXD-	SP3RXD-
13	SP4RXD+	SP4RXD+	SP3RTS+
14	SP4RXD-	SP4RXD-	SP3RTS-
15	NA	NA	SP3CTS+
16	NA	NA	SP3CTS-
17	NA	NA	SP3DCD+
18	NA	NA	SP3DCD-
19	NA	NA	SP3TXC0+
20	NA	NA	SP3TXC0-
21	DCG #1	C50 ENABLE	SP3TXCI+
22	NetP5 (TX+)	NA	SP3TXCI-
23	NetP5 (TX-)	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NetP5 (RX+)	POWERUP	CPURESET
26	NetP5 (RX-)	POWERDOWN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

A2 TO A5 CONNECTOR PIN OUT			
PIN	A	B	C
1	SP1TXD+	SP6TXD+	SP5TXD+
2	SP1TXD-	SP6TXD-	SP5TXD-
3	SP1RXD+	SP6RXD+	SP5TXC+
4	SP1RXD-	SP6RXD-	SP5TXC-
5	SP1RTS+	SP1TXC0+	SP5RXD+
6	SP1RTS-	SP1TXC0-	SP5RXD-
7	SP1CTS+	SP1TXCI+	SP5RXC+
8	SP1CTS-	SP1TXCI-	SP5RXC-
9	SP1DCD+	SP1RXC+	SP3TXD+
10	SP1DCD-	SP1RXC-	SP3TXD-
11	SP2TXD+	SP4TXD+	SP3RXD+
12	SP2TXD-	SP4TXD-	SP3RXD-
13	SP2RXD+	SP4RXD+	SP3RTS+
14	SP2RXD-	SP4RXD-	SP3RTS-
15	SP2RTS+	SP2TXC0+	SP3CTS+
16	SP2RTS-	SP2TXC0-	SP3CTS-
17	SP2CTS+	SP2TXCI+	SP3DCD+
18	SP2CTS-	SP2TXCI-	SP3DCD-
19	SP2DCD+	SP2RXC+	SP3TXC0+
20	SP2DCD-	SP2RXC-	SP3TXC0-
21	DCG #1	NA	SP3TXCI+
22	NetP5 (TX+)	NA	SP3TXCI-
23	NetP5 (TX-)	NA	SP3RXC+
24	NA	LINESYNC	SP3RXC-
25	NetP5 (RX+)	POWERUP	CPURESET
26	NetP5 (RX-)	POWERDOWN	CPU LED
27	DCG #1	DCG #1	DCG #1
28	+12 VDC SER	-12 VDC SER	+5 Standby
29	+5 VDC	+5 VDC	+5 VDC
30	DCG #1	DCG #1	DCG #1
31	ISO +12 VDC	ISO +12 VDC	ISO +12 VDC
32	DCG #2	DCG #2	DCG #2

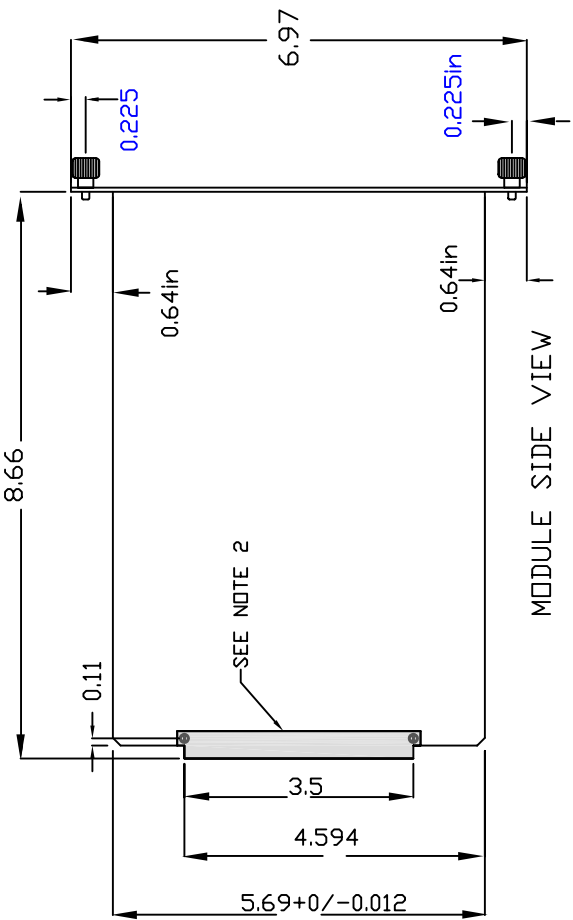
NOTES: (FOR THIS DETAIL)

- Functions are referenced to the CPU.
- DCG #1 for +5VDC and +/-12VDC SER.
DCG #2 for ISO +12 VDC.
- A1 Connector is the furthest A Connector to the left when viewed from the unit back.
- Connector A2 to A4, pins B21 and B22 shall read "NA".
Connector A2, pins B23 shall read "A2 Installed".
Connector A3, pins B23 shall read "A3 Installed".
Connector A4, pins B23 shall read "NA".
Connector A5, pins B21 shall read "A2 Installed".
Connector A5, pins B22 shall read "DCG #1".
Connector A5, pins B23 shall read "A3 Installed".
- Pin A24 (NA) is reserved for network protection only, ie., "Ethernet Shield".
- Module installed in slot A2 enables SP1 & SP2 on 2070-1x modules.
- Module installed in slot A3 enables SP5, on 2070-1x modules.
- SP3 and SP6 are always enabled.
- "C50 ENABLE" Active (e.g. DCG #1) is used by module installed in slot A1 to disable its channel 2 (i.e. SP4).
- NetP5 signals TX+, TX-, RX+, RX- respectively.

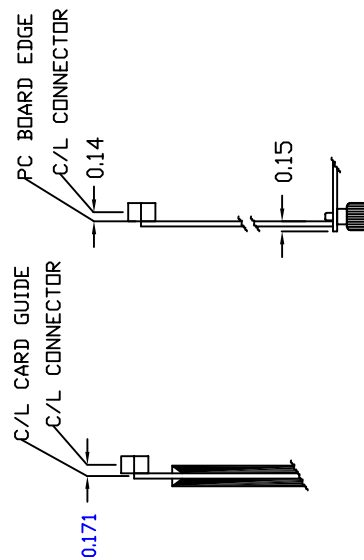
TITLE: MODEL 2070-MOTHERBOARD A1-A5 CONNECTOR PIN OUT	
NO SCALE	A9-5
TEES 2009	



FRONT FRONT FRONT FRONT
6X WIDE MODULE 4X WIDE MODULE 2X WIDE MODULE 1X WIDE MODULE



MODULE SIDE VIEW



TOP VIEW DETAILS

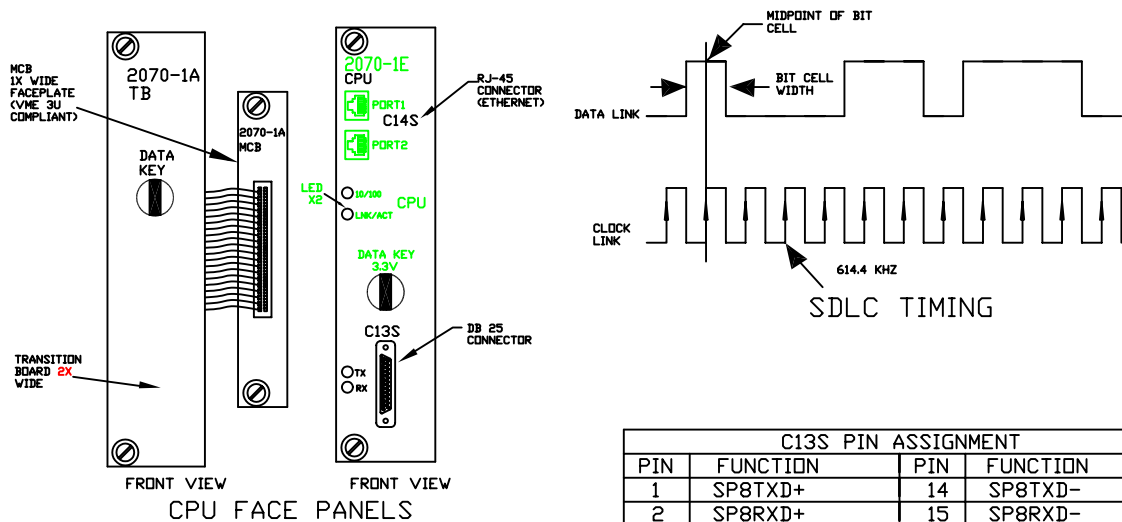
NOTES: (FOR THIS DETAIL)

1. All Thumbscrew devices on modules described in this drawing shall be TSD#3 or equal.
2. 96 pin DIN connector ELCO # 00 8272 96 000 013 or equal.
3. All dimensions shown are in inches.

TITLE: MODEL 2070-SYSTEM PCB MODULES GENERAL	
NO SCALE	A9-6
TEES 2009	

SERIAL PORT REQUIREMENTS			
LOGICAL PORT		RATE KBITS	PROTOCOL
SP1		1.2, NOTE 1	ASYNC
SP1S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP2		1.2, NOTE 1	ASYNC
SP2S		19.2, NOTE 2	SYNC, HDLC, SDLC
SP3		1.2, NOTE 1	ASYNC
SP3S		614.4, NOTE 3	SYNC, HDLC, SDLC
SP4		9.6, NOTE 1	ASYNC
SP5		1.2, NOTE 1	ASYNC
SP5S		614.4	SYNC, HDLC, SDLC
SP6		38.4, NOTE 1	ASYNC
SP8**	NOTE 4	9.6, NOTE 1	ASYNC
SP8S**	NOTE 4	153.6, NOTE 3	SYNC, HDLC, SDLC

SDLC FRAME LAYOUT					
OPENING FLAG	ADDR	CONTROL	INFORMATION	CRC	CLOSING FLAG
0111 1110	8 BITS	1000 0011	VARIABLE LENGTH	16 BITS	0111 1110



C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8TXD+	14	SP8TXD-
2	SP8RXD+	15	SP8RXD-
3	SP8TXC+	16	SP8TXC-
4	SP8RXC+	17	SP8RXC-
5	SP8RTS+	18	SP8RTS-
6	SP8CTS+	19	SP8CTS-
7	SP8DCD+	20	SP8DCD-
8	NA	21	NA
9	LINESYNC+	22	LINESYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

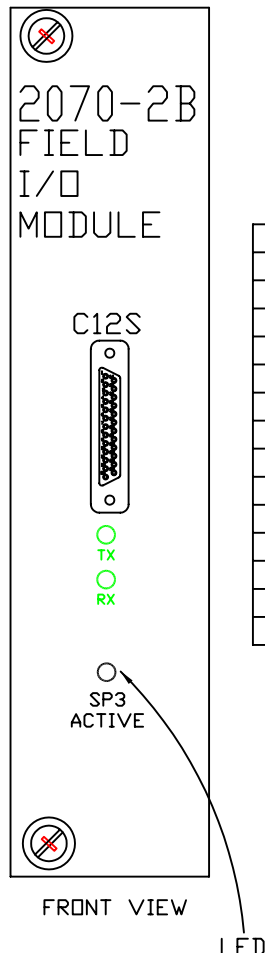
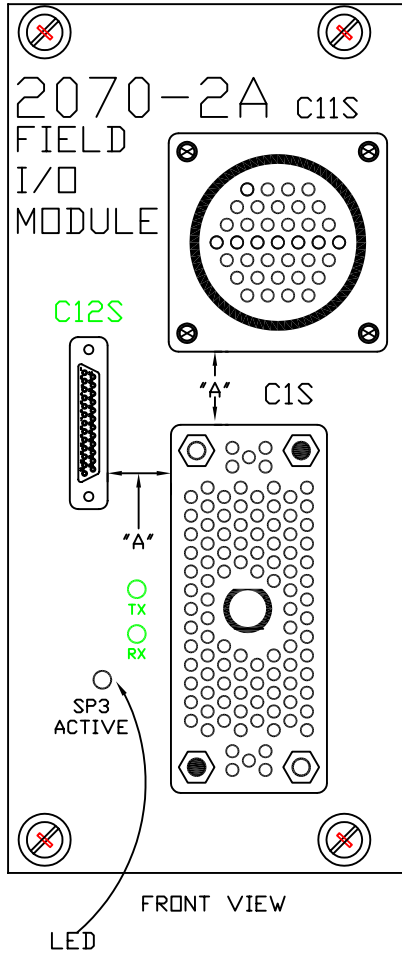
C14S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NOTES: (FOR THIS DETAIL)

- Additional rates 1.2, 2.4, 4.8, 9.6, 19.2, 38.4.
- Additional descriptors for other rates:
SPxSa = 19.2, SPxSb = 38.4, SPxSc = 57.6
SPxSd = 76.8, SPxSg = 64.0, SPxSe = 153.6.
- Additional descriptors for other rates:
SPxSe = 153.6, SPxSf = 614.4.
- On 2070-1A, SP1 is assigned to 68360 SCC1.
On 2070-1E, SP1 and SP8 are assigned to the dual SCC, and ETHERNET is assigned to 68EN360 SCC1.
- A Post Header (ROBINSON NUGENT IDA-XX OR EQUAL) Connector with strain relief shall be provided on the MCB Front Plate and the Transition Board for mating with the interface harness. The harness shall be shielded and straight through wired.
- BIAS +5VDC (50mA maximum) refers to voltage required for a Line Terminator device and is derived from the ISO +12VDC Power Supply.
- EG (Equipment Ground) pin is electrically connected to the faceplate.

** 2070-1E only.

TITLE:	MODEL 2070-1E CPU MODULES AND SERIAL PORT/SDLC PROTOCOL
NO SCALE	A9-7
TEES 2009	



FIELD I/O FACE PANELS

C12S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP5TXD+	14	SP5TXD-
2	SP5RXD+	15	SP5RXD-
3	SP5TXC+	16	SP5TXC-
4	SP5RXC+	17	SP5RXC-
5	SP3TXD+	18	SP3TXD-
6	SP3RXD+	19	SP3RXD-
7	SP3TXC+	20	SP3TXC-
8	SP3RXC+	21	SP3RXC-
9	LINE SYNC+	22	LINE SYNC-
10	NRESET+	23	NRESET-
11	POWERDOWN+	24	POWERDOWN-
12	BIAS +5 VDC	25	EG
13	DCG #2		

NOTES: (FOR THIS DETAIL)

- 2070-2A Faceplate shall be 4X wide. 2070-2B Faceplate shall be 2X wide.
(SEE SYSTEM PCB MODULE, GENERAL DETAILS.)
- Dark Circles in the C1S Connector denote guide pin locations and opencircles denote guide socket locations.
- Dimension "A" shall be a minimum of 0.5in.
- C1S - M104 Type. C11S - 37-Pin Circular Plastic Type.
C12S - 25-Pin DB Socket Type
- C12S pin 12 (BIAS +5VDC) at 50mA maximum is derived from the ISO +12 VDC Power Supply.
BIAS +5VDC refers to voltage required for a Line Terminator device.
- EG (Equipment Ground) pin is electrically connected to the faceplate.
- LED indicators Tx & Rx for SP3 shall be provided (field side).
- C1 connector shall be bolted to the front plate.

TITLE:		MODEL 2070-2 FIELD I/O MODULES
NO SCALE	A9-8	
TEES 2009		

C1S PIN ASSIGNMENT

PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME
1	DCG #2	27	Q24	53	I14	79	I44
2	Q0	28	Q25	54	I15	80	I45
3	Q1	29	Q26	55	I16	81	I46
4	Q2	30	Q27	56	I17	82	I47
5	Q3	31	Q28	57	I18	83	Q40
6	Q4	32	Q29	58	I19	84	Q41
7	Q5	33	Q30	59	I20	85	Q42
8	Q6	34	Q31	60	I21	86	Q43
9	Q7	35	Q32	61	I22	87	Q44
10	Q8	36	Q33	62	I23	88	Q45
11	Q9	37	Q34	63	I28	89	Q46
12	Q10	38	Q35	64	I29	90	Q47
13	Q11	39	I0	65	I30	91	Q48
14	DCG #2	40	I1	66	I31	92	DCG #2
15	Q12	41	I2	67	I32	93	Q49
16	Q13	42	I3	68	I33	94	Q50
17	Q14	43	I4	69	I34	95	Q51
18	Q15	44	I5	70	I35	96	Q52
19	Q16	45	I6	71	I36	97	Q53
20	Q17	46	I7	72	I37	98	Q54
21	Q18	47	I8	73	I38	99	Q55
22	Q19	48	I9	74	I39	100	Q36
23	Q20	49	I10	75	I40	101	Q37
24	Q21	50	I11	76	I41	102	Q38 DET RES
25	Q22	51	I12	77	I42	103	Q39 WDT
26	Q23	52	I13	78	I43	104	DCG #2

C11S PIN ASSIGNMENT

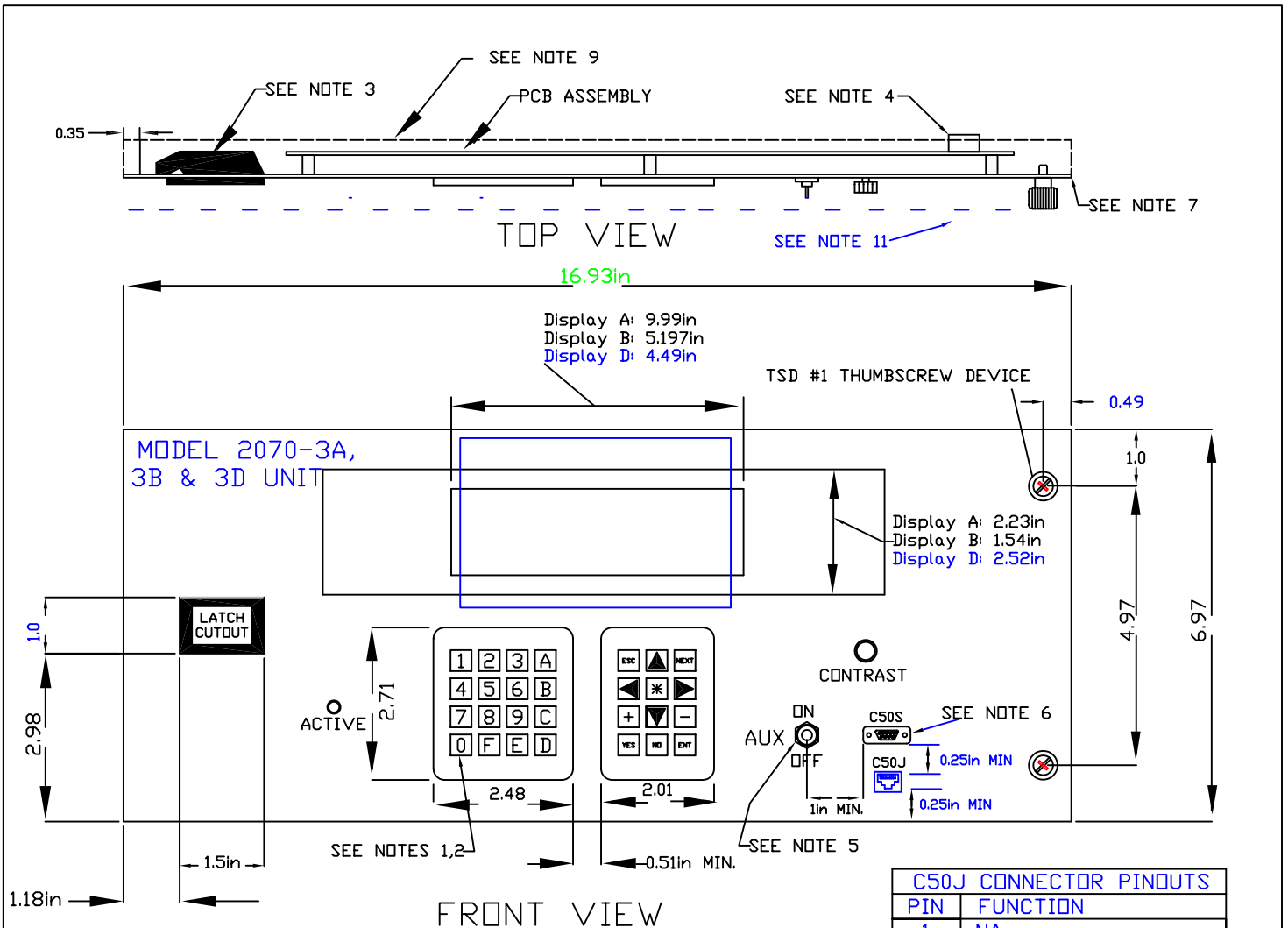
PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME	PIN	FUNCTION NAME
1	Q56	11	I25	21	I54	31	DCG #2
2	Q57	12	I26	22	I55	32	NA
3	Q58	13	I27	23	I56	33	NA
4	Q59	14	DCG #2	24	I57	34	NA
5	Q60	15	I48	25	I58	35	NA
6	Q61	16	I49	26	I59	36	NA
7	Q62	17	I50	27	I60	37	DCG #2
8	Q63	18	I51	28	I61		
9	DCG #2	19	I52	29	I62		
10	I24	20	I53	30	I63		

TITLE: MODEL 2070-2A
FIELD I/O MODULE
C1S & C11S CONNECTORS

NO SCALE

TEES 2009

A9-9



C50J CONNECTOR PINDS	
PIN	FUNCTION
1	NA
2	SP4RXD
3	C50 ENABLE
4	NA
5	SP4TXD
6	DCG #1
7	NA
8	NA

C50S CONNECTOR PINDS	
PIN	C50S FUNCTION
1	C50 ENABLE
2	SP4RXD
3	SP4TXD
4	NA
5	DCG #1
6	NA
7	NA
8	NA
9	NA

C60P CONNECTOR PINDS	
PIN	FUNCTION
1	B Box Power, Note 10
2	SP6RXD
3	SP6TXD
4	NA
5	DCG #3
6	NA
7	CPURESET
8	NA
9	CPU LED

NOTES: (FOR THIS DETAIL)

- Key size shall be (0.3x0.3)in.
- Key center to center spacing shall be 0.5in.
- Slide latch shall be a SOUTHCO flush style A3-40-625-12 (OR EQUAL).
- The 40 contact connector shall be similar to AMP 102160-9 or equal & compatible to the FP harness in type and pin assignments. Center of the FP harness connector shall be vertically positioned (3.54+/-0.197)in as measured from the top of the FPA. The connector shall be a right angle connector with pin 1 located on the lower right hand corner.
- Two position LOGIC switch mounted vertically.
- "C50S" connector shall be a DE-9 socket contact connector. "C50J" shall be a RJ-45 8-position jack. "C60P" connector shall be a DE-9 plug contact connector.
- Front panel sheet metal thickness shall be (0.06±0.005) in.
- The FPA shall be provided with a continuous top and bottom 0.63in (inside dimension) lip bent 90 degrees to the front plate and shall extend the full length of the FPA.
- C60P B Box Power is +5VDC, 350mA max. All signals on C60 P are referenced to isolated interface ground DCG#3.
- Components shall not protrude beyond the height of the thumbscrews when tightened.
- See 9.4.1 for components required.
- All dimensions shown are in inches.

TITLE: MODEL 2070-3A, 3B & 3D FRONT PANEL ASSEMBLY	
NO SCALE	A9-10
TEES 2009	

MODEL 2070-3 AUX SWITCH CODES		
SWITCH POSITION	ASCII DATA (TEXT)	ASCII DATA (HEX)
ON	ESC O T	1B 4F 54
OFF	ESC O U	1B 4F 55

MODEL 2070-3 KEY CODES		
KEY	ASCII DATA (TEXT)	ASCII DATA (HEX)
0	0	30
1	1	31
2	2	32
3	3	33
4	4	34
5	5	35
6	6	36
7	7	37
8	8	38
9	9	39
A	A	41
B	B	42
C	C	43
D	D	44
E	E	45
F	F	46
<UP ARROW>	ESC [A	1B 5B 41
<DOWN ARROW>	ESC [B	1B 5B 42
<RIGHT ARROW>	ESC [C	1B 5B 43
<LEFT ARROW>	ESC [D	1B 5B 44
ESC	ESC O S	1B 4F 53
NEXT	ESC O P	1B 4F 50
YES	ESC O Q	1B 4F 51
NO	ESC O R	1B 4F 52
*	*	2A
+	+	2B
-	-	2D
ENTER	CR	OD

TITLE: MODEL 2070-3 FRONT PANEL ASSEMBLY KEY CODES	
NO SCALE	A9-11
TEES 2009	

CONFIGURATION COMMAND CODES

ASCII REPRESENTATION	HEX VALUE	FUNCTION
HT	09	Move cursor to next tab stop
CR	0D	Position cursor at first position on current line
LF	0A	(Line Feed) Move cursor down one line
BS	08	(Backspace) Move cursor one position to the left and write space
ESC [Py j Px f	1B 5B Py 3B Px 66	Position cursor at (Px, Py)
ESC [Pn C	1B 5B Pn 43	Position cursor Pn positions to right
ESC [Pn D	1B 5B Pn 44	Position cursor Pn positions to left
ESC [Pn A	1B 5B Pn 41	Position cursor Pn positions up
ESC [Pn B	1B 5B Pn 42	Position cursor Pn positions down
ESC [H	1B 5B 48	Home cursor (move to 1,1)
ESC [2 J	1B 5B 32 4A	Clear screen with spaces without moving cursor
ESC c	1B 63	Soft reset
ESC P P1 [Pn j Pn...f	1B 50 P1 5B Pn 3B...Pn 66	Compose special character number Pn (1-8) at current cursor position
ESC [< Pn V	1B 5B 3C Pn 56	Display special character number Pn (1-8) at current cursor position
ESC [25 h	1B 5B 32 35 68	Turn Character blink on
ESC [25 l	1B 5B 32 35 6C	Turn character blink off
ESC [< 5 h	1B 5B 3C 35 68	Illuminate Backlight
ESC [< 5 l	1B 5B 3C 35 6C	Extinguish Backlight
ESC [33 h	1B 5B 33 33 68	Cursor blink on
ESC [33 l	1B 5B 33 33 6C	Cursor blink off
ESC [27 h	1B 5B 32 37 68	Reverse video on -Note 2
ESC [27 l	1B 5B 32 37 6C	Reverse video off -Note 2
ESC [24 h	1B 5B 32 34 68	Underline on -Note 2
ESC [24 l	1B 5B 32 34 6C	Underline off -Note 2
ESC [0 m	1B 5B 30 6D	All attributes off
ESC H	1B 48	Set tab stop at current cursor position
ESC [Pn g	1B 5B Pn 67	Pn = 0 : Clear Tab at Current Position, Pn = 3 : Clear All Tabs
ESC [? 7 h	1B 5B 3F 37 68	Auto-wrap on
ESC [? 7 l	1B 5B 3F 37 6C	Auto-wrap off
ESC [? 8 h	1B 5B 3F 38 68	Auto-repeat on
ESC [? 8 l	1B 5B 3F 38 6C	Auto-repeat off
ESC [? 12 h	1B 5B 3F 31 32 68	Heater on
ESC [? 12 l	1B 5B 3F 31 32 6C	Heater off
ESC [? 25 h	1B 5B 3F 32 35 68	Cursor on
ESC [? 25 l	1B 5B 3F 32 35 6C	Cursor off
ESC [< 47 h	1B 5B 3C 34 37 68	Auto-scroll on
ESC [< 47 l	1B 5B 3C 34 37 6C	Auto-scroll off
ESC [< Pn S	1B 5B 3C Pn 53	Set Backlight timeout value to Pn (0-63)
ESC [PU	1B 5B 50 55	String sent to CPU when FPA power up

NOTES:

- Numerical values have one ASCII character per digit without leading zero.
- Reverse Video & Underline NOT required for Front Panel Assembly Option 3A 3B & 3D.
Command codes shall be available for Option 3C (C60P).

INQUIRY COMMAND-RESPONSE CODES

COMMAND CPU Module to Front Panel Module		RESPONSE Front Panel Module to CPU Module		FUNCTION
ASCII Representation	HEX Value	ASCII Representation	HEX Value	
ESC [6 n	1B 5B 36 6E	ESC [Pyj Px R	1B 5B Py 3B Px 52	Inquire Cursor Position
ESC [B n	1B 5B 42 6E	ESC [P1;P2;.....P6 R	1B 5B P1 3B P2 3B...P6 52	Status Cursor Position P1: Auto-wrap (h,l) P2: Auto-scroll (h,l) P3: Auto-repeat (h,l) P4: Backlight (h,l) P5: Backlight timeout P6: AUX Switch (h,l)
ESC [A n	1B 5B 41 6E	ESC [P1 R	1B 5B P1 52	P1: AUX Switch (h,l)
ESC [h n	1B 5B 68 6E	ESC [P1 R	1B 5B P1 52	P1: Heater (h,l)
ESC [c	1B 5B 63	ESC [P1 R	1B 5B P1 52	P1: Type (A,B,D)

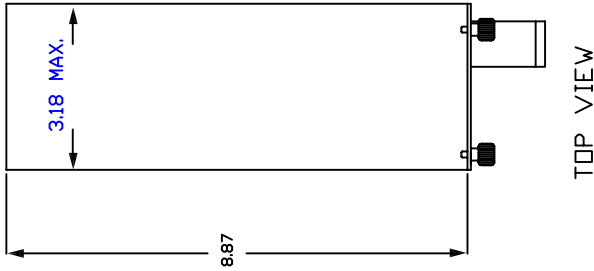
TITLE:

MODEL 2070-3
FRONT PANEL ASSEMBLY
DISPLAY KEY CODES

NO SCALE

TEES 2009

A9-12

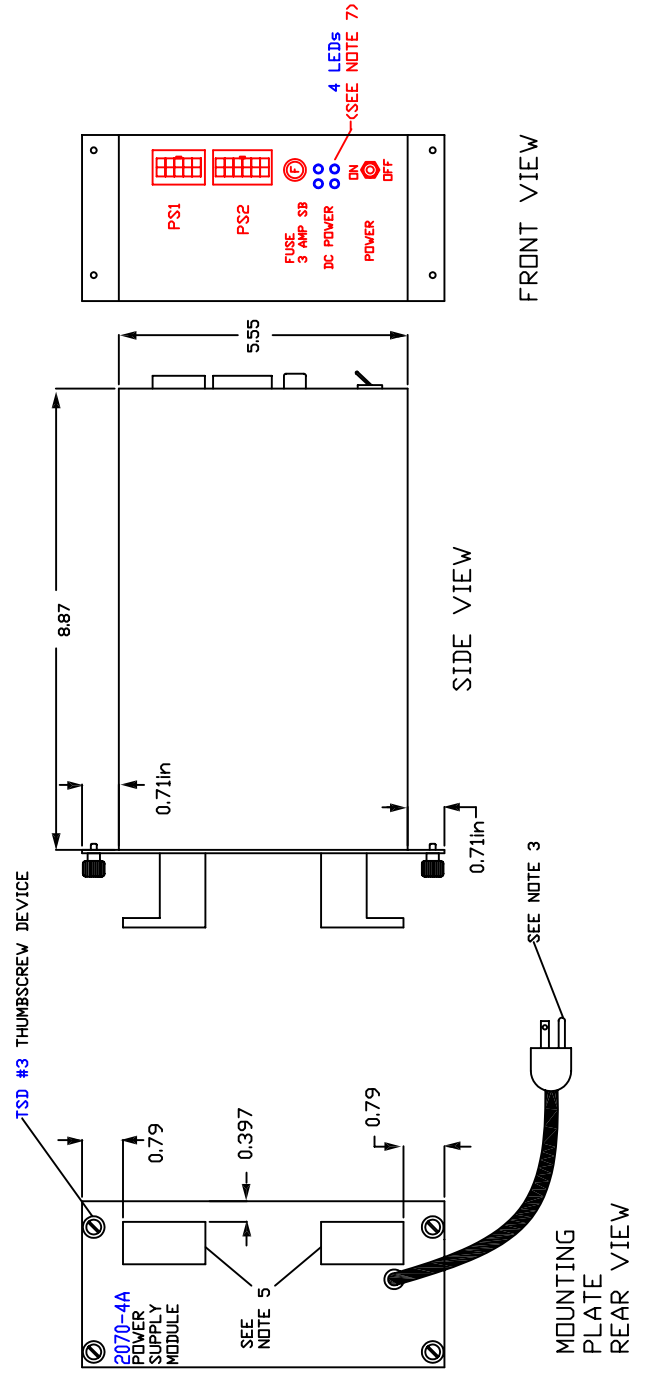


PS1 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	+5 VDC SENSE
7	DCG #1 SENSE
8	AC FAIL
9	SYSRESET
10	NA

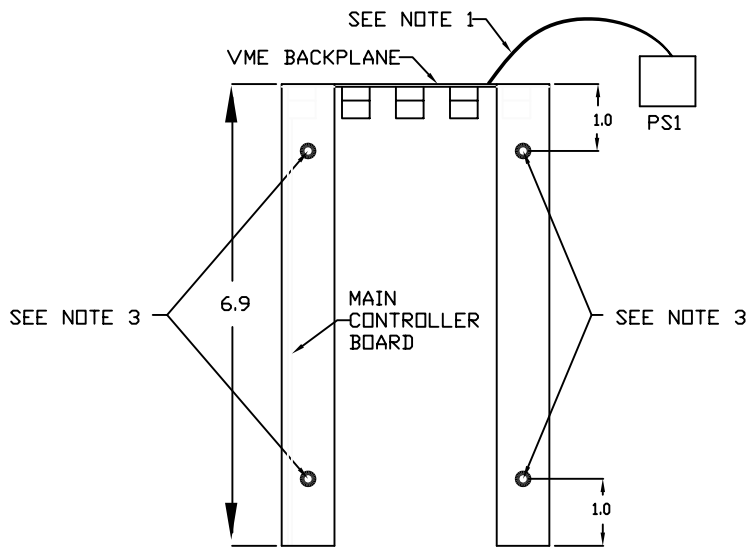
PS2 CONNECTOR PINOUT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & 12 SER)
5	+5 VDC Standby
6	ISO +12 VDC
7	DCG #2 (ISO +12 VDC ONLY)
8	POWERDOWN
9	POWERUP
10	EG (EQUIPMENT GROUND)
11	LINESYNC
12	NA

NOTES: (FOR THIS DETAIL)

1. Power switch shall be mounted vertically. Power On shall be in the up position.
2. Fuse shall be a replaceable 3AG Slow Blow type resident in a fuse holder. Fuse label shall indicate rating.
3. Three conductor #16 power cable, 40 inch minimum length and permanency attached to the Module with strain relief. The end plug connector shall be a three blade NEMA 5-15P grounding plug type.
4. PS1 and PSS2 Receptacle Connectors shall be AMP Mini-Universal Double row **MATE-N-LOK 2 CAP** Connectors with locking latch devices (OR EQUAL).
5. PS1 connector shall be a 10 position PLUG connector. PS2 connector shall be a 12 position PLUG connector.
6. Buckeye Cord-Wrap PP-40055 device with PP-40058 Extension (OR EQUAL).
6. Mounting Plate shall conform to the 4X Wide Module dimensions.
7. A LED indicator shall be provided for each DC power source (+5, ISO +12, +12 SER, -12 SER).
8. Power Supply shall be marked as 2070-4A.
9. All dimensions shown are in inches.

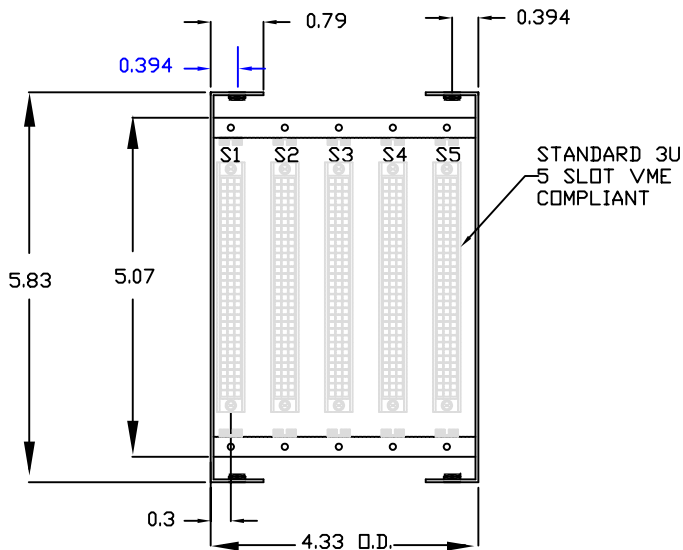


TITLE:		MODEL 2070-4 POWER SUPPLY MODULE
NO SCALE	A9-13	
TEES 2009		



TOP VIEW

PS1 CONNECTOR PIN ASSIGNMENT	
PIN	FUNCTION
1	+5 VDC
2	+12 VDC SER
3	-12 VDC SER
4	DCG #1 (+5 VDC & ±12 SER)
5	+5 VDC Standby
6	+5 VDC SENSE
7	DCG #1 SENSE
8	AC FAIL
9	SYSRESET
10	NA

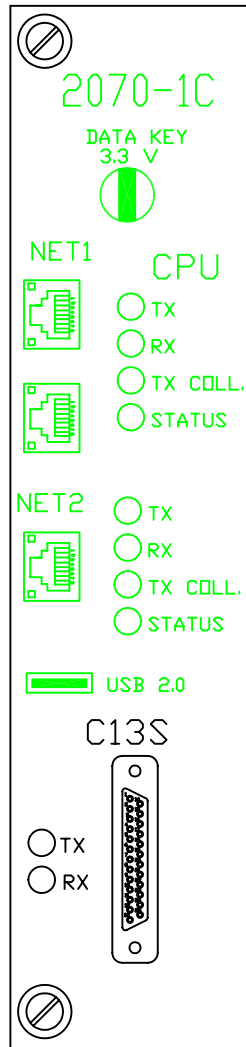


FRONT VIEW

NOTES: (FOR THIS DETAIL)

1. PS1 Harness interfaces between the Model 2070-4 Power Supply Module and the 2070-5 VME Cage Assembly. The harness shall be permanently attached to the Cage Assembly by solder, **FastOn** or Power Bugs. The Harness wiring shall be 8 #18 conductors for power and 2 #22 conductors for others.
2. The plate shall cover the open area & attach to the Chassis Backplane mounting surface via **TSD #3 thumbscrews**. The screws shall mate with the PEM nuts as specified in the Model 2070 Chassis Top View Detail.
3. **6-32** PEM Self-clinching Miniature Fasteners (OR EQUAL) shall be used for mounting holes to match the 6-32 screws on the top and bottom of the Model 2070 chassis.
4. All dimensions shown are in inches.

TITLE:		MODEL 2070-5 VME CAGE ASSEMBLY
NO SCALE		A9-14
TEES 2009		



Note (2)

USB 2.0 PIN ASSIGNMENT	
PIN	FUNCTION
1	VCC
2	DATA-
3	DATA+
4	GND

NET1 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

NET2 PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

C13S PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	SP8 TX +	14	SP8 TX -
2	SP8 RX +	15	SP8 RX -
3	SP8 TXC +	16	SP8 TXC -
4	SP8 RXC +	17	SP8 RXC -
5	SP8 RTS +	18	SP8 RTS -
6	SP8 CTS +	19	SP8 CTS -
7	SP8 DCD +	20	SP8 DCD -
8	NA	21	NA
9	LINESYNC +	22	LINESYNC -
10	NRESET +	23	NRESET -
11	PWRDWN +	24	PWRDWN -
12	BIAS +5 VDC	25	EQUIP GND
13	DC GND #2		

NOTES: (FOR THIS DETAIL)

- BIAS +5VDC refers to voltage required for a Line Terminator device.
- NET1, NET2, USB & C13S should be placed within the area as shown.

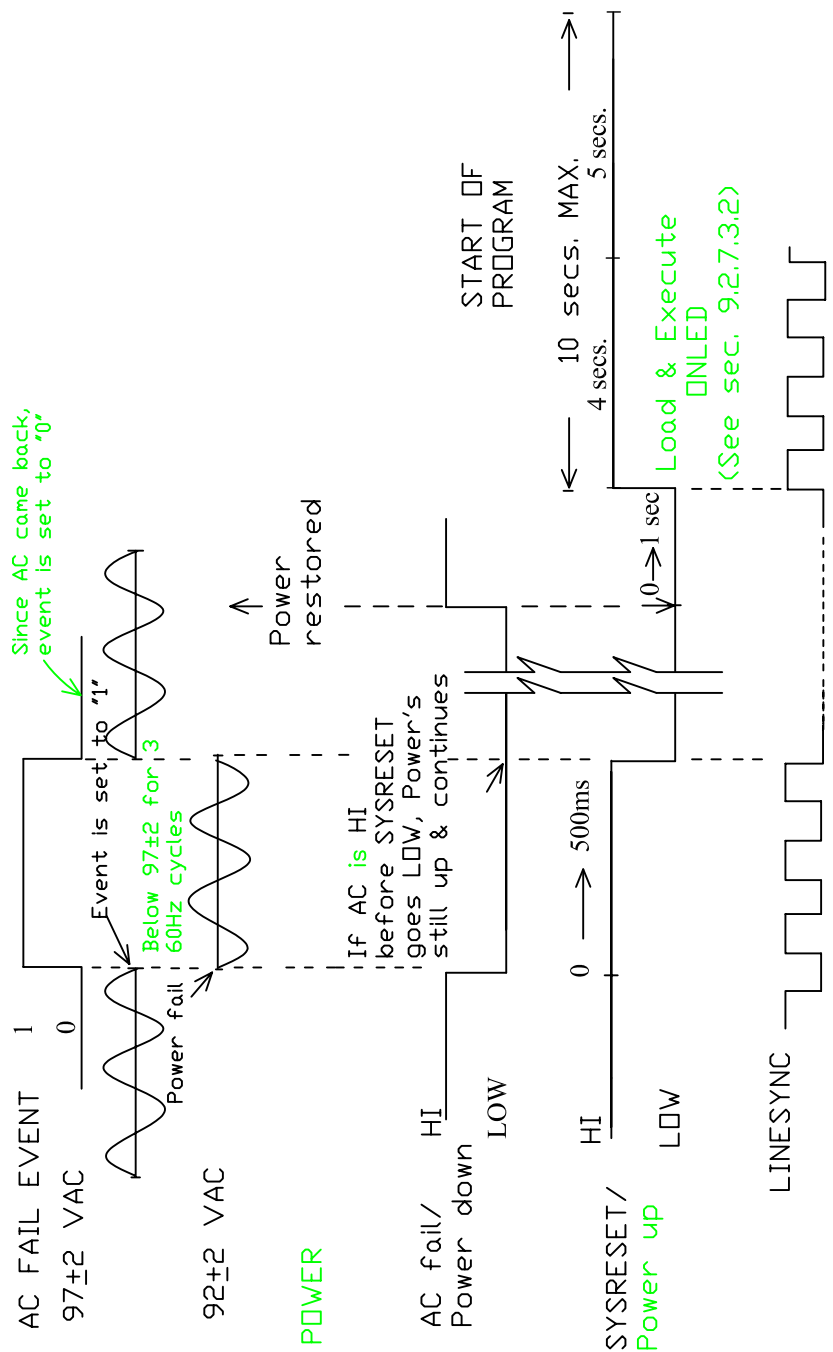
TITLE:		MODEL 2070-1C CPU
NO SCALE	A9-15	
TEES 2009		

SERIAL PORT DESCRIPTORS DEFAULTS			
SP1, SP2, SP3 and SP5	SP4	SP6	SP8
noupc	noupc	noupc	noupc
bsb	bsb	bsb	bsb
bsl	bsl	bsl	bsl
noecho	echo	echo	noecho
lf	lf	lf	lf
null=0	null=0	null=0	null=0
nopause	nopause	nopause	nopause
page=24	page=24	page=24	page=24
bsb=08	bsb=08	bsb=08	bsb=08
dell=18	dell=18	dell=18	dell=18
eor=0D	eor=0D	eor=0D	eor=0D
eof= 1B	eof= 1B	eof= 1B	eof= 1B
reprint=04	reprint=04	reprint=04	reprint=04
dup=01	dup=01	dup=01	dup=01
psc=17	psc=17	psc=17	psc=17
abort=03	abort=03	abort=03	abort=03
quit=05	quit=05	quit=05	quit=05
bse=08	bse=08	bse=08	bse=08
bell=07	bell=07	bell=07	bell=07
type=00	type=00	type=00	type=00
baud=1200	baud=9600	baud=38400	baud=9600
xon=11	xon=00	xon=11	xon=11
xoff=13	xoff=00	xoff=13	xoff=13
tabc=09	tabc=09	tabc=09	tabc=09
tabs=4	tabs=4	tabs=04	tabs=04

NOTES: (FOR THIS DETAIL)

1. All serial port descriptors shall be set with 8 Bit Word, 1 Stop & no Parity.
2. Model 2070-1C sp4 shall be set to 38.4 Kbps.
3. sp3s & sp5s shall be set to 614.4 Kbps.

TITLE:		SERIAL PORT DESCRIPTORS DEFAULTS
NO SCALE	A9-16	
TEES 2009		



NOTES:

Power Failure: A Power Failure is said to have occurred when the incoming line voltage falls below 92+/-2 VAC for 50ms. See Power Conditions.

Power Restoration: Power is said to be restored when the incoming line voltage equals or exceeds 97+/-2 VAC for 50ms. See Power Conditions.

Power Conditions: A 16.7 ms (one 60 Hz cycle) reaction period is allowed to be included in the 50 ms timing or added to (60 ms duration). The hysteresis between power failure and power restoration voltage settings shall be a min. of 5 VAC with a threshold drift of no more than 0.2 VAC.

TITLE:		MODEL 2070 POWER FAILURE REACTION
NO SCALE	A9-17	
TEES 2009		

**APPENDIX A10
CHAPTER DETAILS**

Model 2070-6 ASYNC / Modem Serial Communication Module	A10-1
Model 2070-7 ASYNC / SYNC Serial Communication Module	A10-2
Model 2070-6D Fiber Optics Communication Module	A10-3
Model 2070-Fx Fiber Optics Network Communication Module	A10-4
Model 2070-6W Wireless Modem Communication Module	A10-5
Model 2070-9 FSK / Dial Up Modem Communication Module	A10-6
Model 2070 - 6E Serial 2 Network Communication Module	A10-7
Model 2070 - 9D Dial-Up Modem Communication Module	A10-8

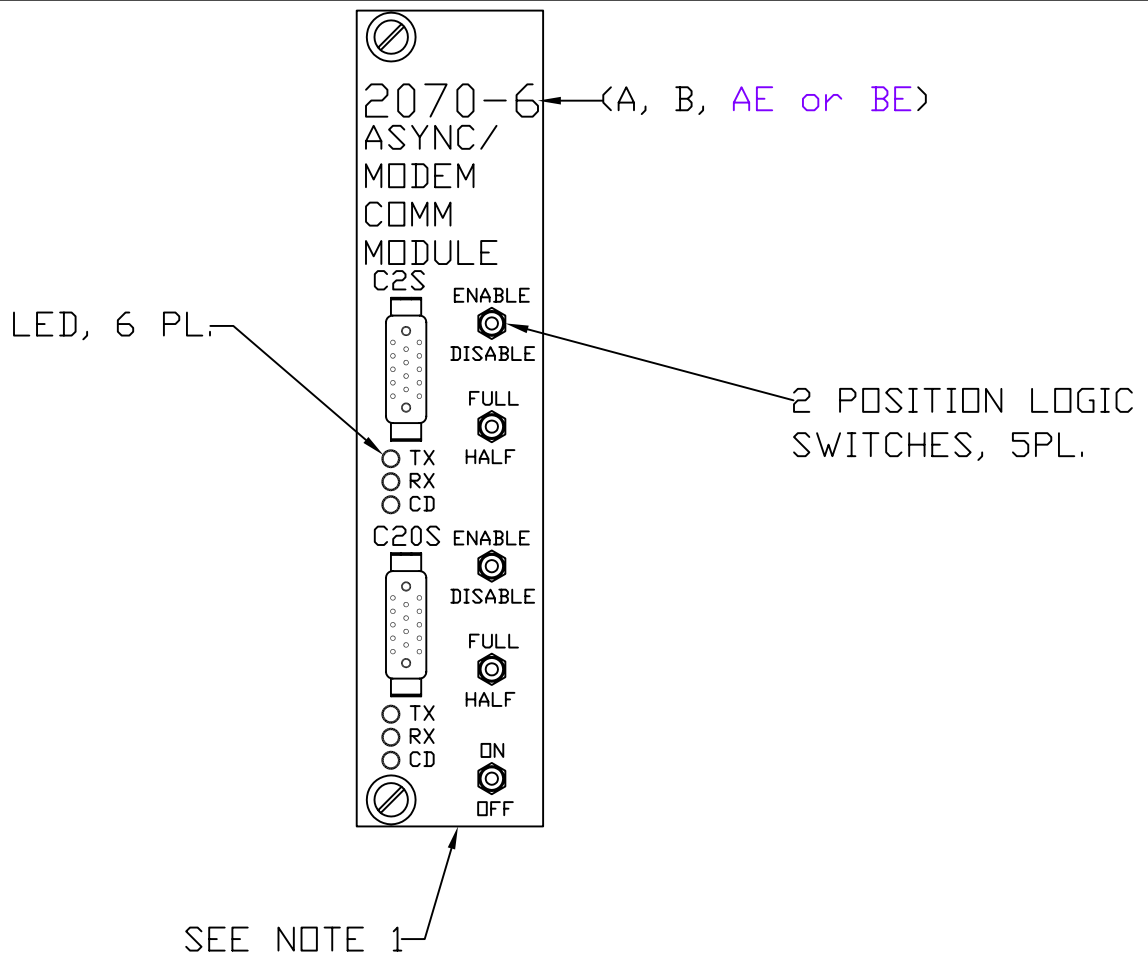
GENERAL NOTES

The 2070-6x and 2070-7x modules shall provide circuitry to disable its Channel 2 and EIA 232 control lines when a ground-true state is presented at Connector A1 Pin B21 (C50 Enable). **C50 Enable shall disable channel 2 via disabling the RS-485 signals to and from the motherboard.** The Disable line shall be pulled up on the module.

Line drivers/receivers shall be socket or surface mounted.

Isolation circuitry shall be opto- or capacitive-coupled isolation technologies. Each module's circuit shall be capable of reliably passing a minimum of 1.0 Mbps.

The Comm modules shall be "Hot" swappable without damage to circuitry or operations.

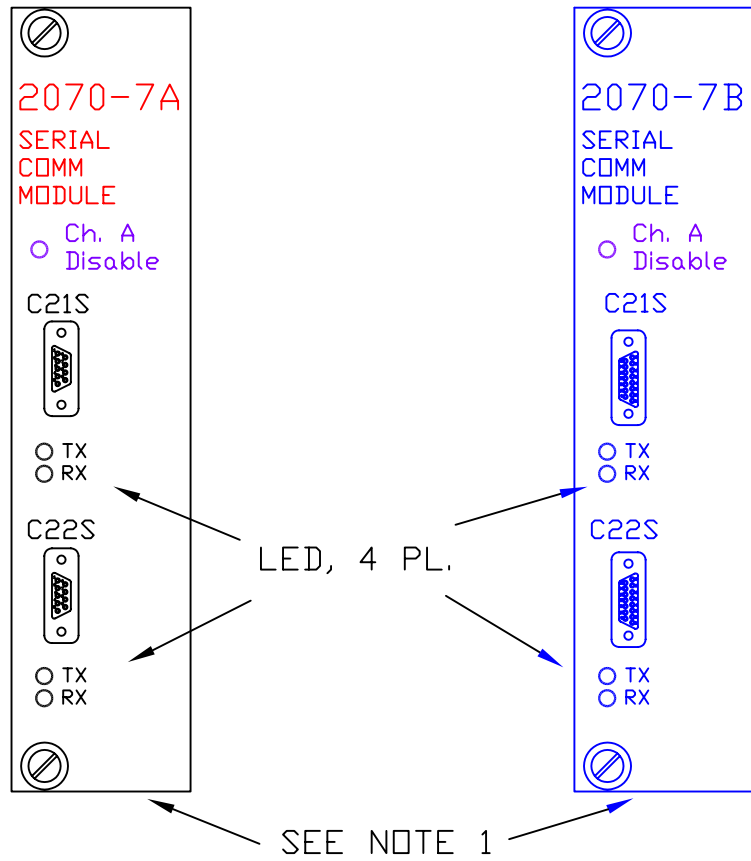


C2S & C20S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	RXD
C	AUDIO OUT	L	TXD
D	IFC +5 VDC	M	CTS
E	AUDIO OUT	N	IFC GND
F	NA	P	NA
H	DCD	R	NA

NOTES: (FOR THIS DETAIL)

- 2X Faceplate
(See 2070 System PCB Module, Detail A9-6).
- Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.
- IFC (Interface) Power and Ground is isolated from the internal ground system & is the voltage reference for the EIA-232 signals also.

TITLE: MODEL 2070-6A, 6B, 6AE, 6BE ASYNC/MODEM SERIAL COMMUNICATION MODULE	
NO SCALE	A10-1
TEES 2009	



2070-7A (DE-9S)	
C21S & C22S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

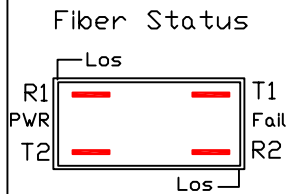
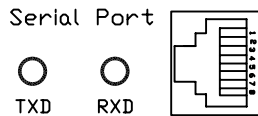
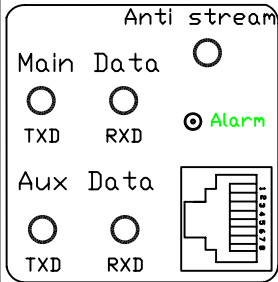
2070-7B (DA-15S)			
C21S & C22S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
1	TXD+	9	TXD-
2	IFC GND	10	IFC GND
3	TXC+	11	TXC-
4	IFC GND	12	IFC GND
5	RXD+	13	RXD-
6	IFC GND	14	IFC GND
7	RXC+	15	RXC-
8	NA		

- NOTES: (FOR THIS DETAIL)
- 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
 - Connectors 21 & 22 are DE 9S for Module 7A & DA 15S for Module 7B.
 - IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.
 - On 2070-7B, SPxRTS shall enable/disable TXD+/- & TXCO+/-
 - TXC is jumper selectable to be either TXCO or TXCI.
 - Channel A denotes C21S and Channel B denotes C22S.

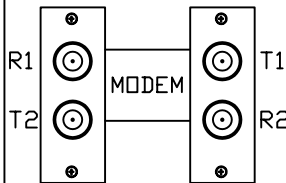
TITLE: MODEL 2070-7A, 7B ASYNC/SYNC SERIAL COMMUNICATION MODULE	
NO SCALE	A10-2
TEES 2009	



2070-6D



Warning
Do not look into
Fiber Ports



AUX. PORT PIN OUT ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	N/C	5	RXD
2	DCD/KOD	6	TXD
3	N/C	7	CTS
4	GND	8	RTS

SERIAL PORT PIN OUT ASSIGNMENTS			
PIN	FUNCTION	PIN	FUNCTION
1	+5 VDC	5	RXD
2	DCD	6	TXD
3	N/C	7	CTS
4	GND	8	RTS

TITLE: MODEL 2070 6D FIBER OPTICS MODEM COMMUNICATION MODULE	
NO SCALE	A10-3
TEES 2009	

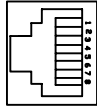


2070-Fx

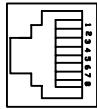
PORT 1

- 10/100 CPU
- Activity
- DUP
- ADD

PORT 2



PORT 3



PORT 4

- Rx1 Tx1

PORT 5

- Rx2 Tx2

100-Fx



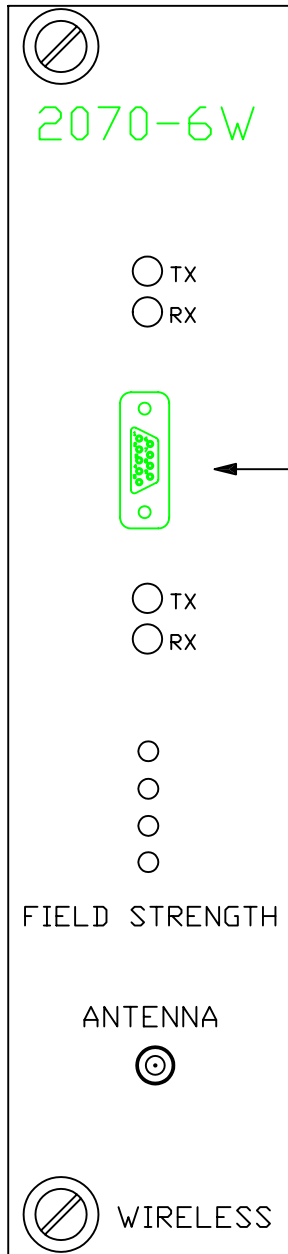
PORT 2 & 3 RJ45 PIN ASSIGNMENTS

PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	RX -
3	RX +	7	NA
4	NA	8	NA

TITLE: MODEL 2070-Fx FIBER OPTICS NETWORK COMMUNICATION MODULE

NO SCALE
TEES 2009

A10-4



COM 1

COM 2

DB-9

FIELD STRENGTH

ANTENNA

WIRELESS

2070-9W (DB-9)	
C21S CONNECTOR PINOUT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.

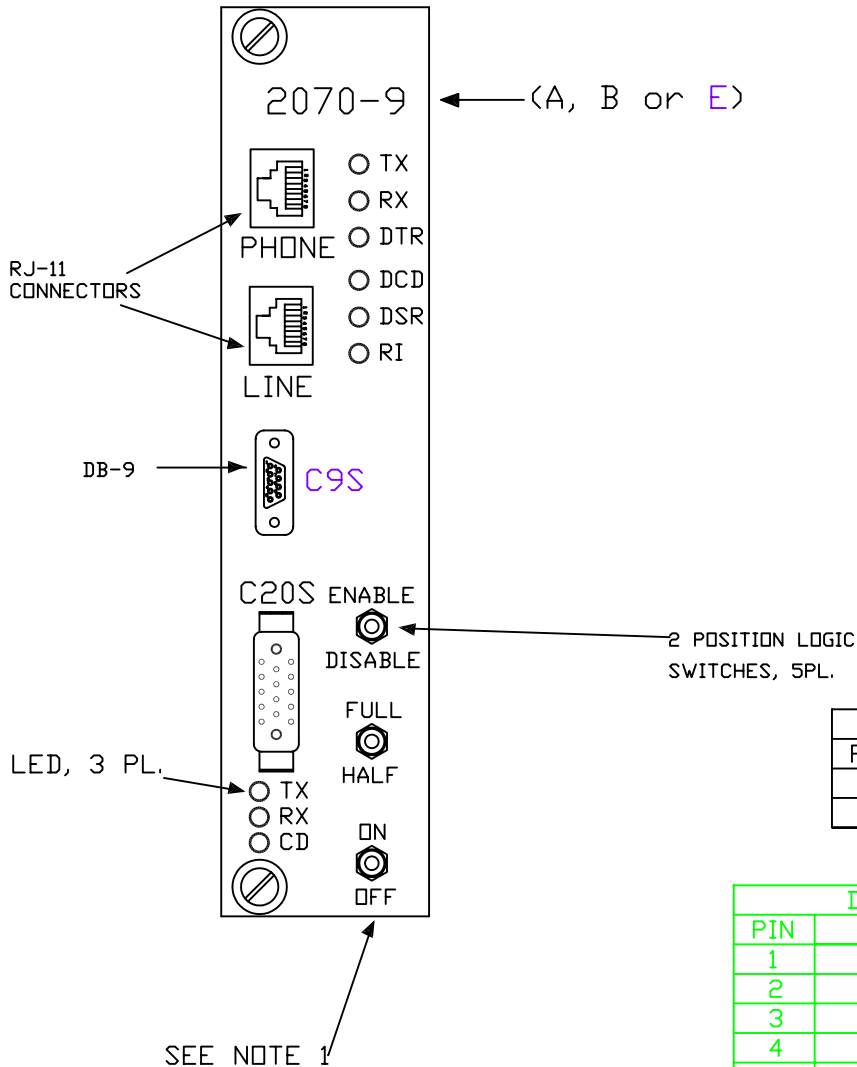
TITLE:

MODEL 2070-6W WIRELESS MODEM
COMMUNICATION MODULE

NO SCALE

TEES 2009

A10-5



RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

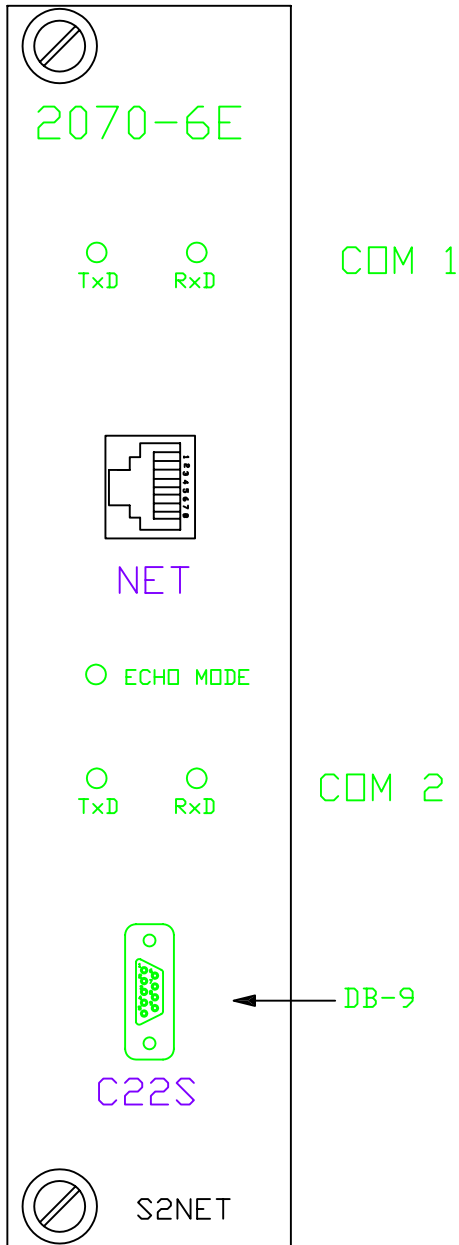
DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

C20S CONNECTOR PINOUT			
PIN	FUNCTION	PIN	FUNCTION
A	AUDIO IN	J	RTS
B	AUDIO IN	K	RXD
C	AUDIO OUT	L	TXD
D	IFC +5 VDC	M	CTS
E	AUDIO OUT	N	IFC GND
F	NA	P	NA
H	DCD	R	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. Connectors C2S & C20S shall be mounted on the front plate and shall be M14 AMP with Spring Latch supports or equal.
3. IFC (Interface) Power and Ground is isolated from the internal ground system and is the voltage reference for the EIA-232 signals also.

TITLE: MODEL 2070-9A, 9B, 9E FSK/DIAL UP MODEM COMMUNICATION MODULE	
NO SCALE	A10-6
TEES 2009	



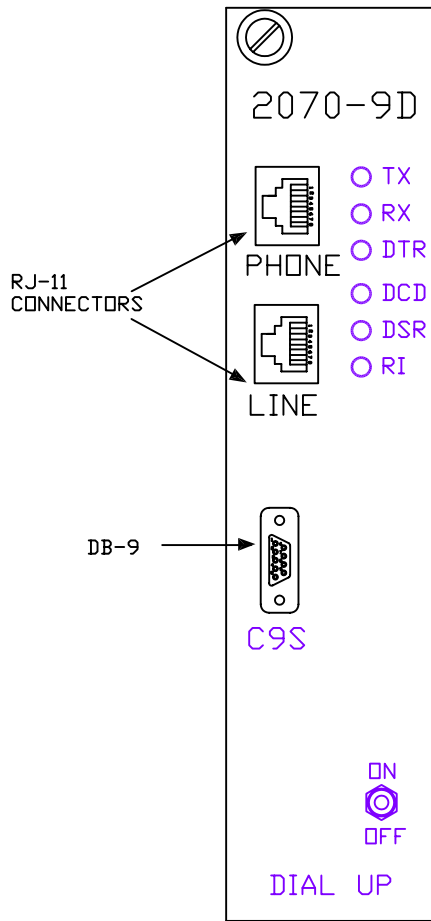
DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

RJ45 ETHERNET PIN ASSIGNMENT			
PIN	FUNCTION	PIN	FUNCTION
1	TX +	5	NA
2	TX -	6	NA
3	RX +	7	NA
4	RX-	8	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. IFC GND is isolated from the internal ground system & is the voltage reference for the EIA-232 & EIA-485 signals.

TITLE:		MODEL 2070-6E SERIAL 2 NETWORK COMMUNICATION MODULE
NO SCALE	A10-7	
TEES 2009		



SEE NOTE 1

RJ-11 PIN-OUT	
PIN	FUNCTION
2	TIP TERMINAL
3	RING TERMINAL

DB9-PIN ASSIGNMENT	
PIN	FUNCTION
1	DCD
2	RXD
3	TXD
4	NA
5	IFC GND
6	NA
7	RTS
8	CTS
9	NA

NOTES: (FOR THIS DETAIL)

1. 2X Faceplate (See 2070 System PCB Module, Detail A9-6).
2. IFC (Interface) Power and Ground is isolated from the internal ground system & is the voltage reference for the EIA-232 signals also.

TITLE:

MODEL 2070-9D
DIAL UP MODEM
COMMUNICATION MODULE

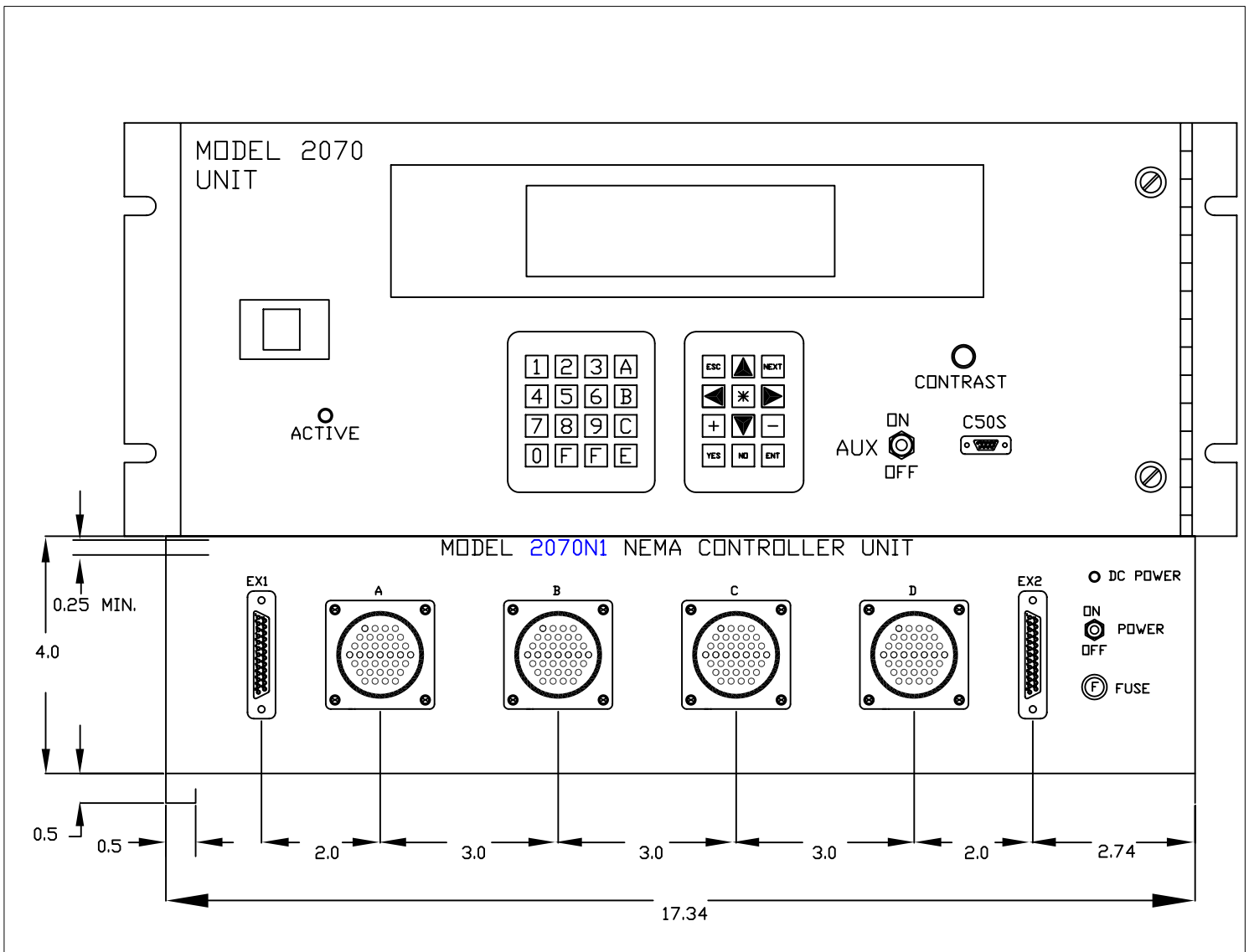
NO SCALE

TEES 2009

A10-8

APPENDIX A11
CHAPTER 11 DETAILS

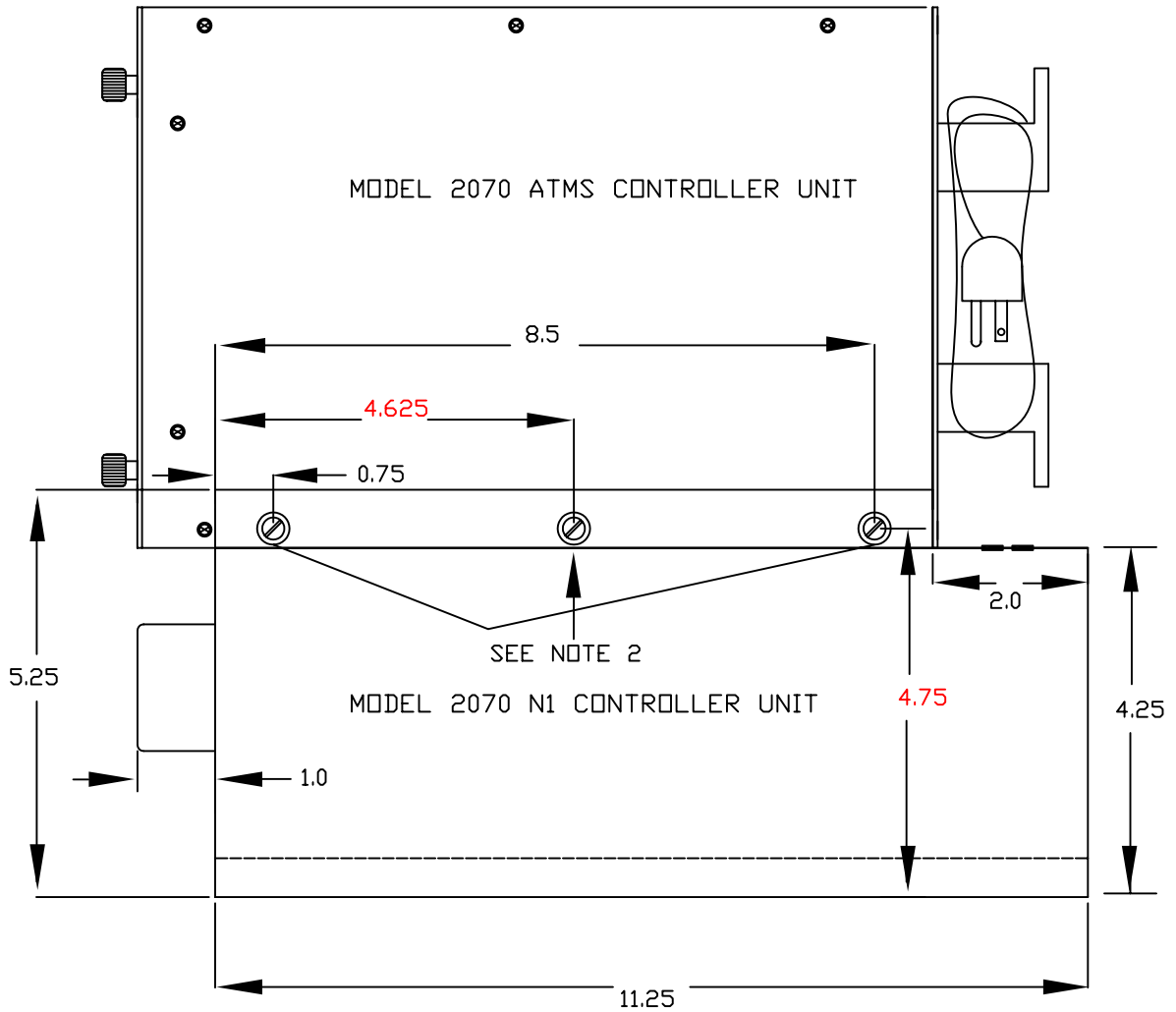
2070 (V or L) N1 Controller Unit - Front View	A11-1
2070 (V or L) N1 Controller Unit - Side View	A11-2
2070 (V or L) N1 Controller Unit - ISO View	A11-3
2070-8 Field I/O Module, Connector A & B	A11-4
2070-8 Field I/O Module, Connector C & D	A11-5
2070-8 Field I/O Module, EX1 & EX2 Connectors	A11-6
2070-2N Field I/O Module	A11-7



NOTES: (FOR THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.
2. The bottom supports shall be double flanged.
3. A = Connector A (MS-3112-22-55P Type)
 B = Connector B (MS-3112-22-55S Type)
 C = Connector C (MS-3112-24-61S Type)
 D = Connector D (MS-3112-24-61P Type)
 EX1 = Connector EX1 (DB-25S Type)
 EX2 = Connector EX2 (DB-25S Type)
4. All dimensions shown are in inches.

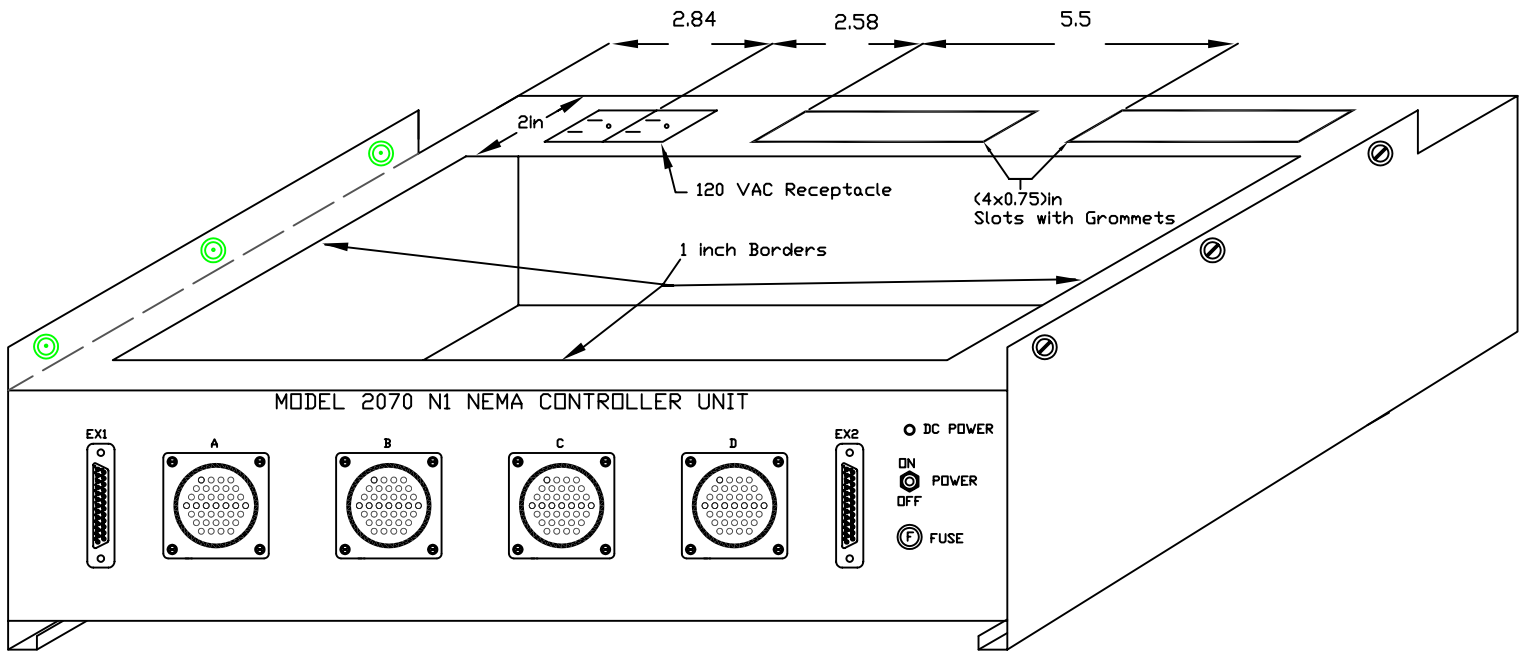
TITLE: 2070 (V or L) N1 CONTROLLER UNIT FRONT VIEW	
NO SCALE	A11-1
TEES 2009	



NOTES: (FOR THIS DETAIL)

1. The Model 2070 Controller Unit is shown only for reference.
2. TDS #3 Thumbscrew Devices. Module shall provide mating nuts permanently mounted on the module.
3. All dimensions shown are in inches.

TITLE:		2070 (V or L) N1 CONTROLLER UNIT SIDE VIEW
NO SCALE	A11-2	
TEES 2009		



NOTES: (FOR THIS DETAIL)

1. The module housing bottom shall be slot vented. The top shall be open.
2. All dimensions shown are in inches.

TITLE: 2070 (V or L) N1 CONTROLLER UNIT ISO VIEW	
NO SCALE	A11-3
TEES 2009	

CONNECTOR A			CONNECTOR B		
PIN	FUNCTION		FUNCTION		PORT
	NAME	PORT	NAME	PORT	
A	Fault Monitor	---	Phase 1 Next	08-1	
B	+24 VDC External	---	Reserved	I9-5	
C	Voltage Monitor	---	Phase 2 Next	08-2	
D	Phase 1 Red	01-1	Phase 3 Green	03-3	
E	Phase 1 Don't Walk	04-1	Phase 3 Yellow	02-3	
F	Phase 2 Red	01-2	Phase 3 Red	01-3	
G	Phase 2 Don't Walk	04-2	Phase 4 Red	01-4	
H	Phase 2 Ped Clear	05-2	Phase 4 Ped Clear	05-4	
J	Phase 2 Walk	06-2	Phase 4 Don't Walk	04-4	
K	Phase 2 Vehicle Detector	I1-2	Phase 4 Check	07-4	
L	Phase 2 Pedestrian Detector	I2-2	Phase 4 Vehicle Detector	I1-4	
M	Phase 2 Hold	I3-2	Phase 4 Pedestrian Detector	I2-4	
N	Stop Timing (Ring 1)	I6-2	Phase 3 Vehicle Detector	I1-3	
P	Inh Max Term (Ring 1)	I6-3	Phase 3 Pedestrian Detector	I2-3	
R	External Start	I8-1	Phase 3 0mit	I5-3	
S	Interval Advance	I8-2	Phase 2 0mit	I5-2	
T	Indicator Lamp Control	I8-3	Phase 5 Ped 0mit	I4-5	
U	AC Neutral	---	Phase 1 0mit	I5-1	
V	Chassis Ground	---	Ped Recycle (Ring 2)	I7-5	
W	2070N DC Ground	---	Reserved	I9-6	
X	Flashing Logic Out	011-7	Reserved	I9-7	
Y	Coded Status Bit C (Ring 1)	012-3	Phase 3 Walk	06-3	
Z	Phase 1 Yellow	02-1	Phase 3 Ped Clear	05-3	
a	Phase 1 Ped Clear	05-1	Phase 3 Don't Walk	04-3	
b	Phase 2 Yellow	02-2	Phase 4 Green	03-4	
c	Phase 2 Green	03-2	Phase 4 Yellow	02-4	
d	Phase 2 Check	07-2	Phase 4 Walk	06-4	
e	Phase 2 0n	09-2	Phase 4 0n	09-4	
f	Phase 1 Vehicle Detector	I1-1	Phase 4 Next	08-4	
g	Phase 1 Pedestrian Detector	I2-1	Phase 4 0mit	I5-4	
h	Phase 1 Hold	I3-1	Phase 4 Hold	I3-4	
i	Force 0ff (Ring 1)	I6-1	Phase 3 Hold	I3-3	
j	Min Recall All Phases	I8-4	Phase 3 Ped 0mit	I4-3	
k	Manual Control Enable	I8-5	Phase 6 Ped 0mit	I4-6	
m	Call To Non-Actuated I	I6-8	Phase 7 Ped 0mit	I4-7	
n	Test Input A	I9-1	Phase 8 Ped 0mit	I4-8	
p	AC Power	---	Overlap A Yellow	010-2	
q	I/O Mode Bit A	I8-6	Overlap A Red	010-3	
r	Coded Status Bit B (Ring 1)	012-2	Phase 3 Check	07-3	
s	Phase 1 Green	03-1	Phase 3 0n	09-3	
t	Phase 1 Walk	06-1	Phase 3 Next	08-3	
u	Phase 1 Check	07-1	Overlap D Red	011-6	
v	Phase 2 Ped 0mit	I4-2	Reserved	I9-8	
w	0mit All-Red Clear (Phase 1)	I6-7	Overlap D Green	011-4	
x	Red Rest Mode (Ring 1)	I6-4	Phase 4 Ped 0mit	I4-4	
y	I/O Mode Bit B	I8-7	Not Assigned	---	
z	Call To Non-Actuated II	I7-8	Max II Selection (Ring 2)	I7-6	
AA	Test Input B	I9-2	Overlap A Green	010-1	
BB	Walk Rest Modifier	I9-4	Overlap B Yellow	010-5	
CC	Coded Status Bit A (Ring 1)	012-1	Overlap B Red	010-6	
DD	Phase 1 0n	09-1	Overlap C Red	011-3	
EE	Phase 1 Ped 0mit	I4-1	Overlap D Yellow	011-5	
FF	Pedestrian Recycle (Ring 1)	I6-5	Overlap C Green	011-1	
GG	Max II Selection (Ring 1)	I6-6	Overlap B Green	010-4	
HH	I/O Mode Bit C	I8-8	Overlap C Yellow	011-2	

TITLE: 2070-8 FIELD I/O MODULE
CONNECTOR A & B

NO SCALE

TEES 2009

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CONNECTOR C			CONNECTOR D	
PIN	FUNCTION		FUNCTION	
	NAME	PORT	NAME	PORT
A	Coded Status Bit A (Ring 2)	012-4	Detector 9	I10-1
B	Coded Status Bit B (Ring 2)	012-5	Detector 10	I10-2
C	Phase 8 Don't Walk	04-8	Detector 11	I10-3
D	Phase 8 Red	01-8	Detector 12	I10-4
E	Phase 7 Yellow	02-7	Detector 13	I10-5
F	Phase 7 Red	01-7	Detector 14	I10-6
G	Phase 6 Red	01-6	Detector 15	I10-7
H	Phase 5 Red	01-5	Detector 16	I10-8
J	Phase 5 Yellow	02-5	Detector 17	I11-1
K	Phase 5 Ped Clear	05-5	Detector 18	I11-2
L	Phase 5 Don't Walk	04-5	Detector 19	I11-3
M	Phase 5 Next	08-5	Detector 20	I11-4
N	Phase 5 Dn	09-5	Detector 21	I11-5
P	Phase 5 Vehicle Detector	I1-5	Detector 22	I11-6
R	Phase 5 Pedestrian Detector	I2-5	Detector 23	I11-7
S	Phase 6 Vehicle Detector	I1-6	Detector 24	I11-8
T	Phase 6 Pedestrian Detector	I2-6	Clock Update	I12-1
U	Phase 7 Pedestrian Detector	I2-7	Hardware Control	I12-2
V	Phase 7 Vehicle Detector	I1-7	Cycle Advance	I12-3
W	Phase 8 Pedestrian Detector	I2-8	Max 3 Selection	I12-4
X	Phase 8 Hold	I3-8	Max 4 Selection	I12-5
Y	Force Off (Ring 2)	I7-1	Free	I12-6
Z	Stop Timing (Ring 2)	I7-2	Not Assigned	I12-7
a	Inhibit Max Timing (Ring 2)	I7-3	Not Assigned	I12-8
b	Test Input C	I9-3	Alarm 1	I13-1
c	Coded Status Bit C (Ring 2)	012-6	Alarm 2	I13-2
d	Phase 8 Walk	06-8	Alarm 3	I13-3
e	Phase 8 Yellow	02-8	Alarm 4	I13-4
f	Phase 7 Green	03-7	Alarm 5	I13-5
g	Phase 6 Green	03-6	Flash In	I13-6
h	Phase 6 Yellow	02-6	Conflict Monitor Status	I13-7
i	Phase 5 Green	03-5	Door Ajar	I13-8
j	Phase 5 Walk	06-5	Special Function 1	I14-1
k	Phase 5 Check	07-5	Special Function 2	I14-2
m	Phase 5 Hold	I3-5	Special Function 3	I14-3
n	Phase 5 Dnit	I5-5	Special Function 4	I14-4
p	Phase 6 Hold	I3-6	Special Function 5	I14-5
q	Phase 6 Dnit	I5-6	Special Function 6	I14-6
r	Phase 7 Dnit	I5-7	Special Function 7	I14-7
s	Phase 8 Dnit	I5-8	Special Function 8	I14-8
t	Phase 8 Vehicle Detector	I1-8	Preempt 1 In	I15-1
u	Red Rest Mode (Ring 2)	I7-4	Preempt 2 In	I15-2
v	Dnit All Red (Ring 2)	I7-7	Preempt 3 In	I15-3
w	Phase 8 Ped Clear	05-8	Preempt 4 In	I15-4
x	Phase 8 Green	03-8	Preempt 5 In	I15-5
y	Phase 7 Don't Walk	04-7	Preempt 6 In	I15-6
z	Phase 6 Don't Walk	04-6	Alarm 1 Out	012-7
AA	Phase 6 Ped Clear	05-6	Alarm 2 Out	012-8
BB	Phase 6 Check	07-6	Special Function 1 Out	013-1
CC	Phase 6 Dn	09-6	Special Function 2 Out	013-2
DD	Phase 6 Next	08-6	Special Function 3 Out	013-3
EE	Phase 7 Hold	I3-7	Special Function 4 Out	013-4
FF	Phase 8 Check	07-8	Special Function 5 Out	013-5
GG	Phase 8 Dn	09-8	Special Function 6 Out	013-6
HH	Phase 8 Next	08-8	Special Function 7 Out	013-7
JJ	Phase 7 Walk	06-7	Special Function 8 Out	013-8
KK	Phase 7 Ped Clear	05-7	Not Assigned	---
LL	Phase 6 Walk	06-6	Detector Reset	011-8
MM	Phase 7 Check	07-7	Not Assigned	---
NN	Phase 7 Dn	09-7	+24 VDC	---
PP	Phase 7 Next	08-7	2070N DC Gnd	---

TITLE: 2070-8 FILED I/O MODULE
CONNECTOR C & D

NO SCALE

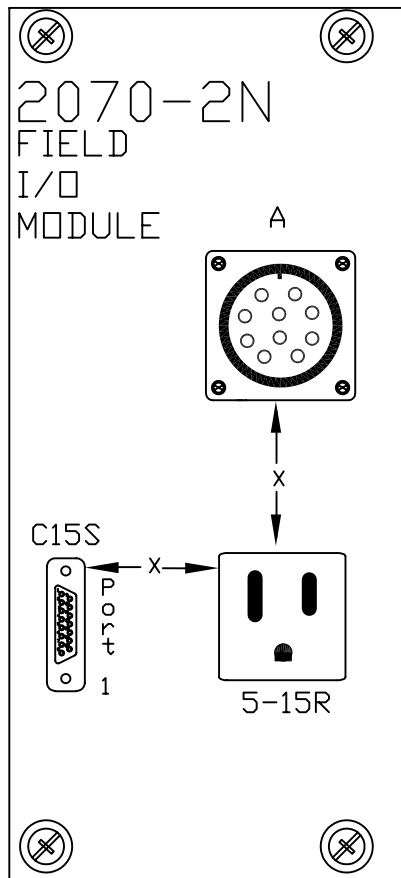
TEES 2009

A11-5

EX1 CONNECTOR PINOUT	
PIN	FUNCTION
1	EQ GND
2	TXD (FCU)
3	RXD (FCU)
4	RTS (FCU)
5	CTS (FCU)
6	NA
7	2070-8 DC GND
8	DCD (FCU)
9	2070-8 DC GND
10	SP3TXD+
11	SP3TXD-
12	SP3TXC+
13	SP3TXC-
14	2070-8 DC GND
15	SP3RXD+
16	SP3RXD-
17	2070-8 DC GND
18	SP3RXC+
19	SP3RXC-
20	NA
21	NA
22	NA
23	NA
24	NA
25	NA

EX2 CONNECTOR PINOUT	
PIN	FUNCTION
1	EG (Equipment Ground)
2	TXD (Channel 1)
3	RXD (Channel 1)
4	RTS (Channel 1)
5	CTS (Channel 1)
6	NA
7	IFC GND
8	DCD (Channel 1)
9	AUDIO IN (Channel 1)
10	AUDIO IN (Channel 1)
11	AUDIO OUT (Channel 1)
12	AUDIO OUT (Channel 1)
13	NA
14	EG (Equipment Ground)
15	TXD (Channel 2)
16	RXD (Channel 2)
17	RTS (Channel 2)
18	CTS (Channel 2)
19	NA
20	IFC GND
21	DCD (Channel 2)
22	AUDIO IN (Channel 2)
23	AUDIO IN (Channel 2)
24	AUDIO OUT (Channel 2)
25	AUDIO OUT (Channel 2)

TITLE:		2070-8 FIELD I/O MODULE EX1 & EX2 CONNECTOR
NO SCALE		A11-6
TEES 2009		



FRONT VIEW

2070-2N FIELD I/O FACE PANEL

A PIN ASSIGNMENT	
PIN	FUNCTION
A	AC Neutral
B	NA
C	AC Line
D	NA
E	NA
F	Fault Monitor
G	DCG #2
H	EG
I	NA
J	NA

C15S PIN ASSIGNMENT	
PIN	FUNCTION
1	SP3TXD+
2	DCG #2
3	SP3TXC+
4	DCG #2
5	SP3RXD+
6	DCG #2
7	SP3RXC+
8	DCG #2
9	SP3TXD-
10	Port 1 Disable
11	SP3TXC-
12	EG
13	SP3RXD-
14	Reserved
15	SP3RXC-

NOTES: (FOR THIS DETAIL)

1. 2070N Faceplate shall be 4X wide.
2. RS-485 Termination Resistors (120 Ohms) provided external to module.
3. Dimension "X" shall be minimum of 1.00 in.
4. A - Intermate with MS3106()-18-1S.
C15S - 15-Pin DB Socket Type.
5. EG (Equipment Ground) pin is electrically connected to the faceplate.
6. Port 1 Disable: 0VDC = Disable.

TITLE:

MODEL 2070-2N
FIELD I/O MODULE

NO SCALE

TEES 2009

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